

Press release: European Processor Initiative Successfully Concluded

Paris, July 15, 2026

On July 1 and 2, 2026, the European Processor Initiative (funded by the EuroHPC Joint Undertaking under Framework Partnership Agreement No 800928 and Specific Grant Agreement No 101036168 – EPI SGA2) held its final review in Luxembourg.

After four years of SGA2, the project successfully concluded its second stage, with highlights of outstanding achievements coming from both the EuroHPC JU's staff and the reviewers. The project's original purpose - helping to pave way towards strengthening Europe's technological sovereignty - has been achieved.

Part of the review was also demonstrating the unique technologies and chips developed within both stages of the project to the reviewers as well as EuroHPC JU's staff.

Rhea1 Demo

The meeting was opened with a world premiere of Rhea1 chip demonstration. It showcased the first Rhea1 silicon running a complete HPC software stack shortly after first silicon was back from foundry and packaging. This highlights the effectiveness of SiPearl's extensive pre-silicon bring-up preparation. The system booted on a test board, with a standard Linux distribution running with high speed HBM memories and their associated hardware performance monitoring counters. It successfully executed the HPL and STREAM benchmarks demonstrating the readiness of the complete Rhea1 hardware and software ecosystem for HPC workloads to power Exascale systems.

EPI accelerators and EPAC Demo

Five live demonstrations were presented, together telling one story: the RISC-V accelerator technology built in EPI is no longer just individual blocks - it now runs a full software stack, from real hardware up to real applications and tools that a normal user can actually take advantage of.

The five demos were:

Demo 1 - A full HPC cluster on the VEC accelerator. This showed the latest RTL (out-of-order RISC-V core by Semidynamics, improved vector unit by Barcelona Supercomputing Center) mapped onto a multi-FPGA system built on the MEEP FPGA infrastructure. A real scientific application was run (Mini-Fall3D, dust

diffusion in the atmosphere, from ChEESE CoE) parallelized with OpenMP + MPI, compiled with the EPI LLVM toolchain, and profiled with standard HPC tools (PAPI, Extrae/Paraver). The runs showed scalability showing execution time of scalar, vector, +OpenMP, +MPI across nodes. The key message: not just one benchmark, but the complete HPC stack coupled with scientific applications, including user-driven performance analysis.

Demo 2 - EPAC 1.5 test chip as an accelerator. This used the real taped-out EPAC 1.5 chip as a RISC-V accelerator attached to an Arm host over PCI Express. The project's compiler generates a single binary containing both Arm and RISC-V code; the RISC-V part is carried over PCIe via DMA, dynamically loaded, executed, and the results copied back. It demonstrates the original EPI compute node idea: a heterogeneous system, Arm CPU + RISC-V accelerator - different ISAs and different operating systems - working efficiently together on real hardware.

Demo 3 - Kalray K VX use case (hardware/software co-design). Kalray showed optimized FFT kernels running on their K VX accelerator, using FFT bottleneck analysis to guide ISA changes together with the hardware teams. The new KV4-1 core outperforms the previous KV3-2 by about 16%, thanks to new instructions and microarchitectural improvements. It also runs in a RISC-V mode), pointing to the next steps.

Demo 4 — Menta EDA tool (Origami)

Menta demonstrated the optimization work done on their European EDA tool for large eFPGAs. They identified placement as the main bottleneck and parallelized the simulated-annealing placement with multi-threading, reaching roughly 9× speedup on 8 threads and fitting the design flow into the project schedule.

Demo 5 — ZeroPoint memory compression (DenseMem) on EPAC 1.5. The live demo generated traffic at different compression ratios and showed the resulting reduction in memory traffic in real time.

The Way Ahead

After three years of SGA1, and now four years of SGA2, the Initiative is proud to announce these outcomes. The way ahead towards European sovereignty in digital technologies lies in furthering these results. The project's scientific partners will make sure of that through publishing the results of the project's extensive research, while the industrial partners will continue to further develop IPs garnered through this project.

*“EPI has evolved from a project into a recognized brand, proving what is possible when Europe's research and industrial communities join forces around a common ARM and RISC-V vision. Together, we haven't only delivered outstanding scientific and technological achievements, but we also strengthened Europe's technological sovereignty and global competitiveness through the development of European processors and accelerators designed to power the next generations of supercomputers”, explains **Eric Monchalín**, chair of the EPI Board.*

“EPI started with a bold ambition: to prove that Europe could build the critical processor technologies needed to achieve leadership in high-performance computing. Today, thanks to the commitment and expertise of all consortium partners, that ambition has become a reality.

Yes, we showed we can. We have laid the technological foundations for a new generation of European HPC and AI processors and opened the path toward seeing a Top-5 supercomputer powered by European-designed chips in the near future.

*As EPI concludes, we are passing the baton to next pioneering initiatives such as EUPEX, EUPILLOT, and DARE, which will carry this momentum forward, transform EPI's achievements into operational systems, and help secure Europe's technological position”, said **Etienne Walter**, General Manager of EPI SGA2 project.*

*“The European Processor Initiative has transformed Europe's processor landscape, delivering unprecedented technological achievements and laying the foundations for European digital sovereignty. The successful demonstration of the fully operational 80-core Rhea1 processor, the most complex processor ever designed in Europe, alongside a portfolio of HPC accelerator chips, marks a defining milestone in Europe's pursuit of technological leadership and digital sovereignty. Equally important, EPI has evolved beyond a research project into a globally recognized brand and a symbol of European technological ambition, establishing itself as both a strategic asset and a landmark initiative in Europe's digital history”, added **Mario Kovač**, EPI SGA2 Chief Communication Officer.*

“Incubated within the EPI consortium, SiPearl is the result of a strong commitment of the European Union to bring to market a CPU that marks the return to Europe of technologies and expertise in high-performance, energy-efficient processors to meet the demands of exascale computing. With Rhea1, we have fulfilled our mission: in a few months' time, our CPU will power JUPITER, Europe's first exascale supercomputer, operated by Jülich and owned by EuroHPC. Next, it will be Rhea2 that powers our continent's second exascale supercomputer, Alice Recoque. Beyond that, SiPearl's next generations of CPUs will power AI gigafactories, data

centres and our defence systems. In this way, SiPearl will contribute to Europe's technological sovereignty and independence", explained **Philippe Notton**, CEO and founder of SiPearl.

"EPI proves that Europe can turn open standards into real silicon. Taking RISC-V from IP blocks to a full HPC software stack, and giving those results back to the community and to follow-on projects, is a lasting contribution to the open-hardware ecosystem", BSC Mobile and embedded-based HPC Group leader and RISC-V Stream activity leader within EPI SGA2, **Filippo Mantovani** said.

Anders Jensen, Executive Director of the EuroHPC Joint Undertaking, stated: *"The European Processor Initiative (EPI) project has brought together leading European expertise from research and industry to advance processor and accelerator technologies for the next generation of HPC. The final demonstrations showcased a fully functional European Processor, as well as the integration of hardware, software and scientific applications on real platforms, highlighting the value of European collaboration and contributing to the continued development of Europe's HPC capabilities."*

About EPI

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