HERAKLION CODESIGN WORKSHOP

DAY 1 – SEP 10

TIME	TOPIC	SPEAKER
09:30	Welcome	(FORTH)
09:50	Welcome & Agenda outline	(EPI-PMO)
10:00	Keynote: “Co-design in AI times: Looking at GPUs from EPI”	(Jesus Labarta - BSC)
11:00	“Experiences and learnings with the EPAC test-chip"	(Filippo Mantovani - BSC)
11:40	<coffee break: 20'>	
12:00	“SiPearl: Overview and roadmap of Rhea processors”	(SiPEARL) - TBC
12:30	“Semidynamics: Overview and roadmap of RISC-V IP cores”	(José María Arnau – SMD)
13:00	<lunch break: 60'>	
14:00	“European RISC-V chips: Experiences and perspectives from the EUPILOT project”	(Carlos Puchol – BSC)
14:30	"Codesign Experiences and perspectives from the EUPEX project”	(Matteo Turisini - CINECA)
15:00	<coffee break: 20'>	
15:20	"Silent Data Corruptions: Demystifying the Unmeasurable"	(Dimitris Gizopoulos – U. Athens)
15:50	“RAS Concerns for RISC-V Systems”	(Daniele Rossi – UNIPI)
16:20	Panel: "European Chips: Technology Challenges & Opportunities"	(position statements & moderated discussion)
17:30	Expected end of day-1 workshop	
20:30	Social dinner	

DAY2 – SEP 11

TIME	TOPIC	SPEAKER
09:45	Welcome & Agenda outline	(EPI-PMO)
10:00	Keynote: “Chiplets and Interposers: Architectural Trends, Integration Technologies, and Strategic Opportunities for Europe”	(Denis Dutoit - CEA)
11:00	<coffee break: 20'>	
11:20	“Experiences from initiating an Arm HPC ecosystem in Europe”	(Jean-Pierre Panziera, Eviden & ETP4HPC)
11:55	“Perspective on Arm processors and GPU acceleration in HPC”	(Filippo Spiga, NVIDIA)
12:25	“Advancing European Sovereignty in HPC with RISC-V: Overview of the DARE project”	(Paul Carpenter - BSC)
13:00	<lunch break: 60'>	
14:00	“Co-Design in the EU HPC Ecosystem: Some examples”	(Matteo Mascagni - EuroHPC JU)
14:35	“Experiences and perspective from European RISC-V chip projects”	(Lluc Alvarez – BSC & Zettascale Lab)
15:10	“Retrospective on the design and validation of the memory hierarchy in RISC-V prototypes”	(Vassilis Papaefstathiou - FORTH)
15:40	<coffee break: 20'>	
16:00	“FAUST - Advanced configurable pipelined RISC-V floating point unit”	(Mario Kovač UNIZG-FER)
16:20	“The EPI Common Platform”	(presentation and discussion)
16:50	Panel: "Codesign to meet future needs of the European HPC ecosystem” (position statements & discussion)	(incl. positions by Pilot and CoE projects - MaX, SPACE, ChEESE, ESiWACE3)
18:00	Expected end of day-2 workshop	

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