

EPI Forum

Barcelona, 9–10.10.2024.





European Processor Initiative

Framework Partnership Agreement In European Low-power Microprocessor Technologies

AGENDA

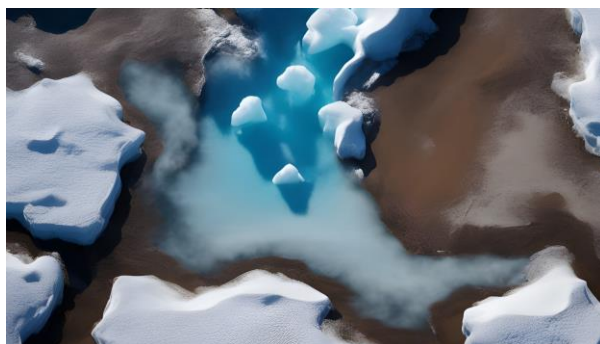


- Why EPI
- Where are we?
- Perspectives

WHY EPI

HPC, THE LEADING EDGE FOR A BRILLIANT PHYGITAL FUTURE

Anticipate climate changes



Study earthquakes



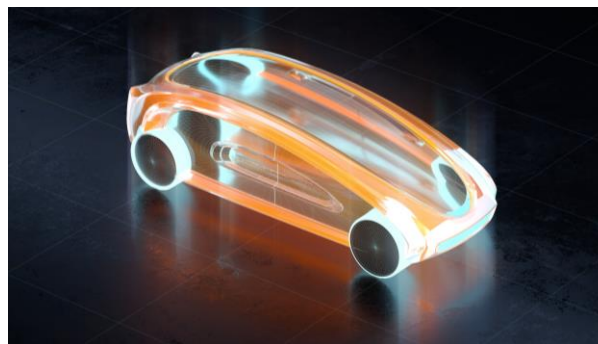
Control epidemics



Care for aging population



Innovate without limit



Secure energy resources



ACHIEVE AUTONOMY IN STRATEGIC PROCESSING TECHNOLOGIES

20%

Production (worldwide value) in Europe of cutting-edge and sustainable semiconductors including processors (instead of 10%)

5 to
2nm

Manufacturing capacity

x10

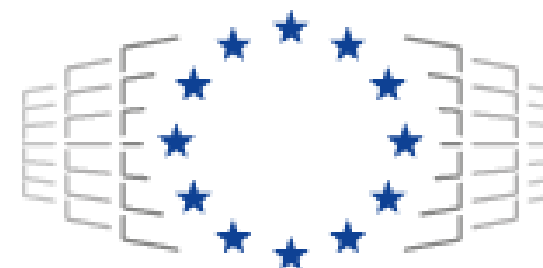
Energy efficiency improvement from 2020



TWO PILLARS TO MAKE EUROPEAN AMBITION A REALITY



Empowering Europe's
Semiconductor Future, uniting
innovation and driving Progress



EuroHPC
Joint Undertaking

Leading the way in European
Supercomputing, developing a World
Class Supercomputing Ecosystem

EU BACK IN THE RACE WITH EUROHPC JU



EuroHPC
Joint Undertaking

Deploy

Develop, deploy, extend & maintain a **world-leading supercomputing, quantum computing, service & data infrastructure ecosystem** in Europe

Innovate

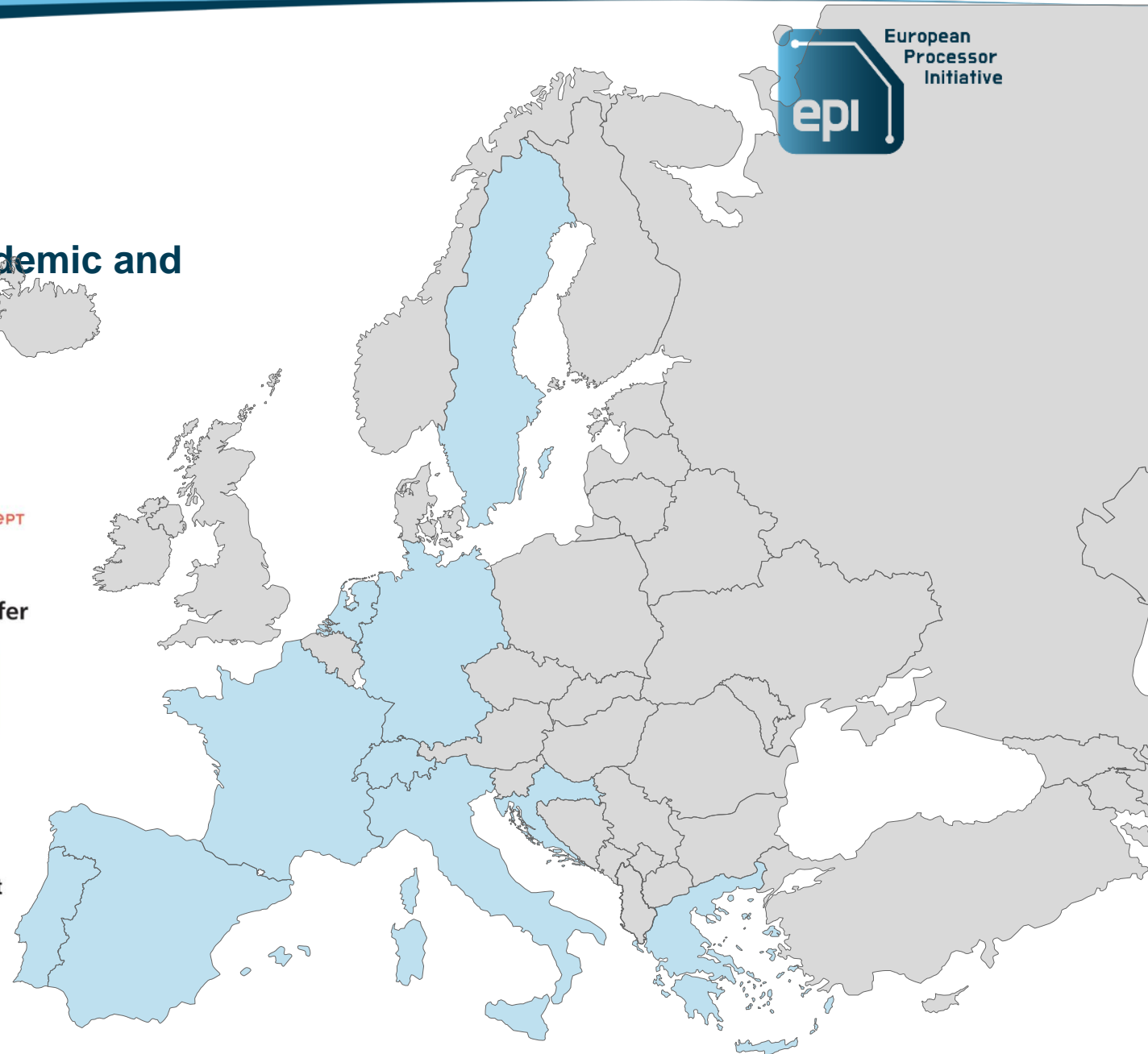
Support the development of **innovative supercomputing components, technologies, knowledge & applications** to underpin a **competitive European supply chain**

Value

Widen the **use of HPC & quantum infrastructures** to a large number of public & private users wherever they are located in Europe and supporting the **development of key HPC skills** for European science and industry

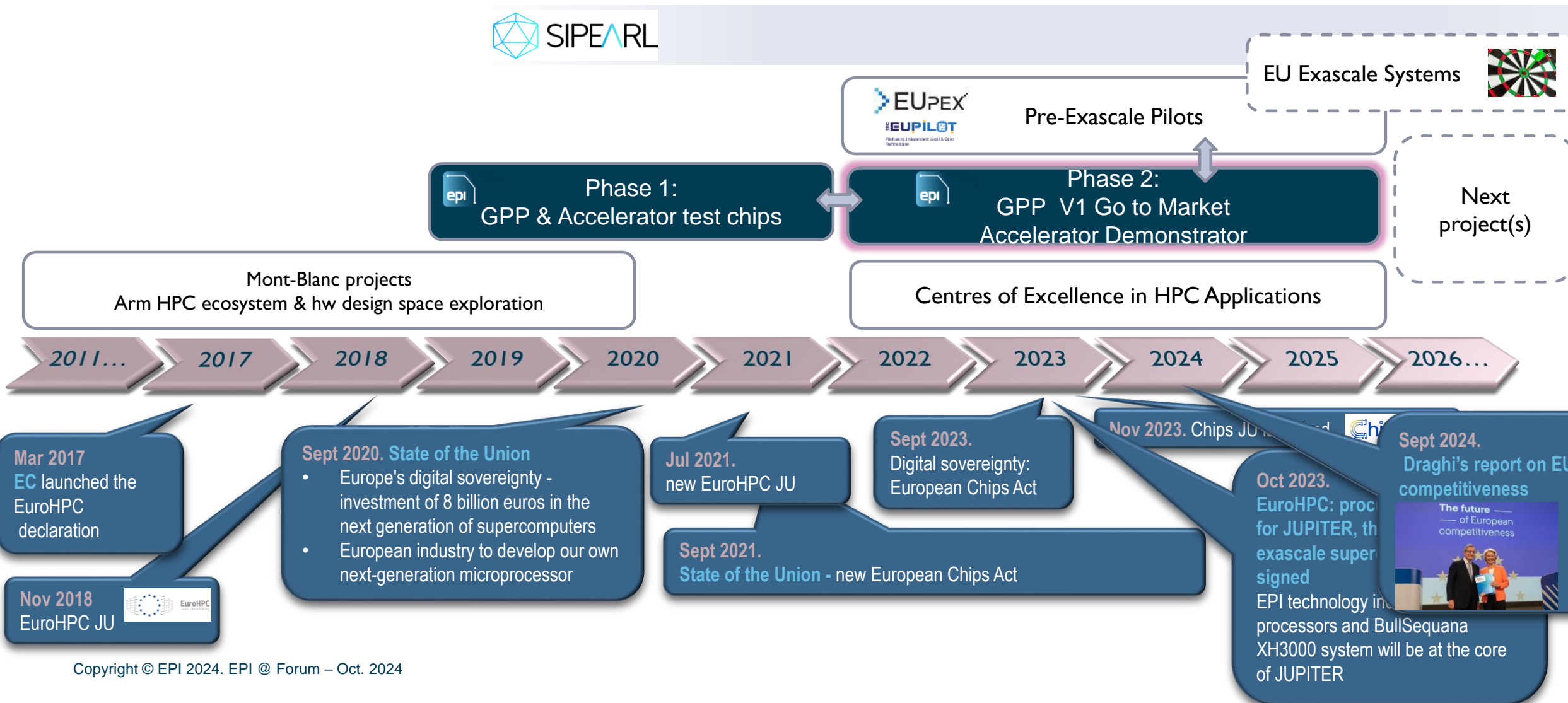
EPI CONSORTIUM

- 27^(*) strategically chosen key European academic and industrial partners
- 10 EU countries



(*) For EPI SGA2 action

EPI MEETS THE EU TIMELINE





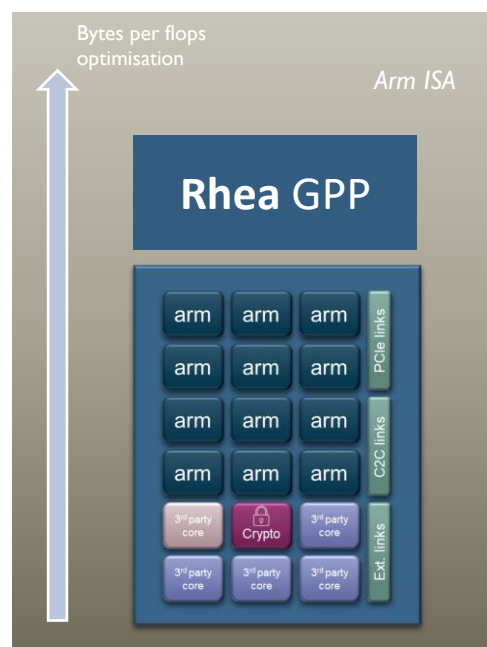
WHERE ARE WE?

EPI & PILOTS : MAIN OBJECTIVES

EU chips fit for HPC usage - at Exascale level

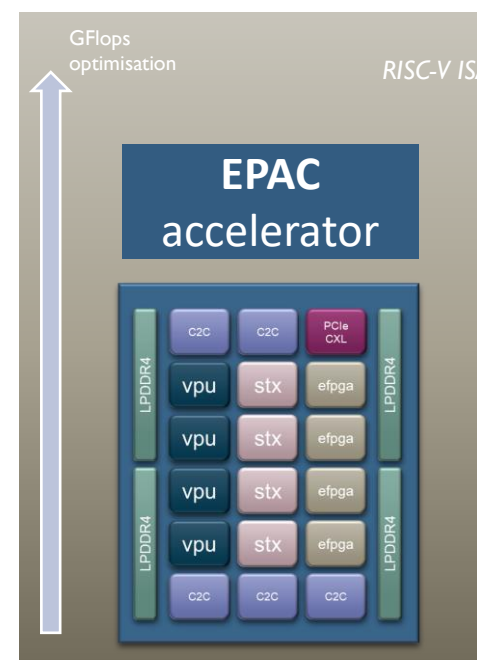
arm

General Purpose Processors:
Legacy & programmability



Accelerators:
Computing force

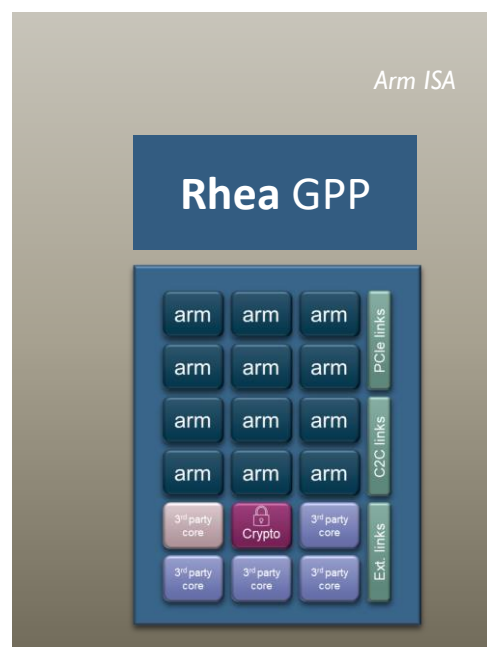
RISC-V®



TWO PROCESSOR FAMILIES : RHEA

arm

General Purpose Processors:
Legacy & programmability

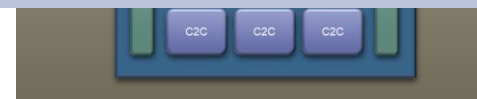


Accelerators:
Computing force

RISC-V

Rhea General Purpose family:

- Arm Neoverse V1 cores
- Arm NoC
- Dedicated crypto IP



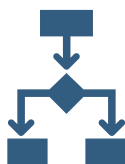
RHEA DEVELOPMENT STATUS



SiPearl Serie A
funding completion



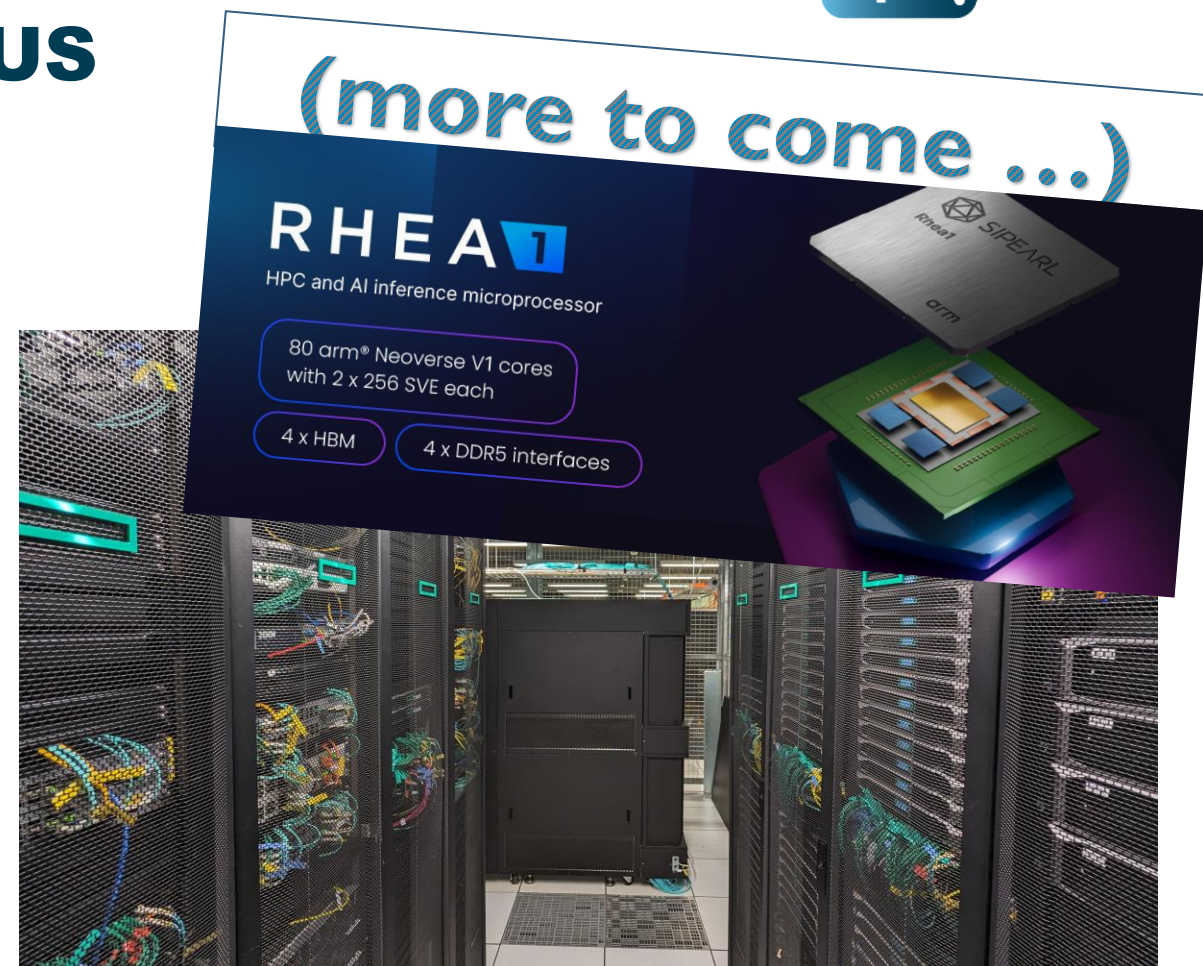
Chip announced
@ ISC



Rhea1 Design
finished



Tests & full
emulation running
well



TWO PROCESSOR FAMILIES - EPAC

arm

General Purpose Processors:
Legacy & programmability

- EPAC accelerator family :
- vpu – Vector Processing Unit
 - Stx – Stencil/Tensor accelerator

Accelerators:
Computing force

RISC-V®



EPAC DEVELOPMENT STATUS



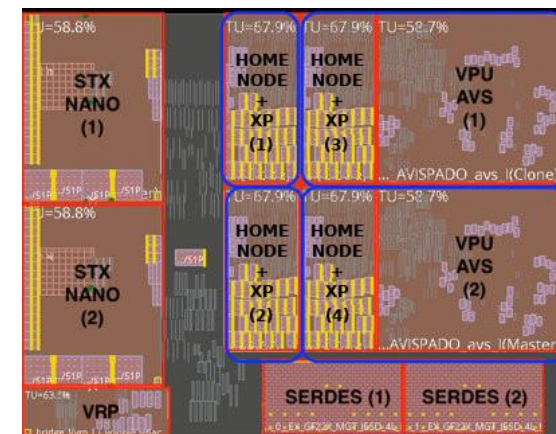
EPAC 1.5 test chip
back, brought-up and
running well



Software
Development Vehicle :
trainings performed



Preparing IPs reuse

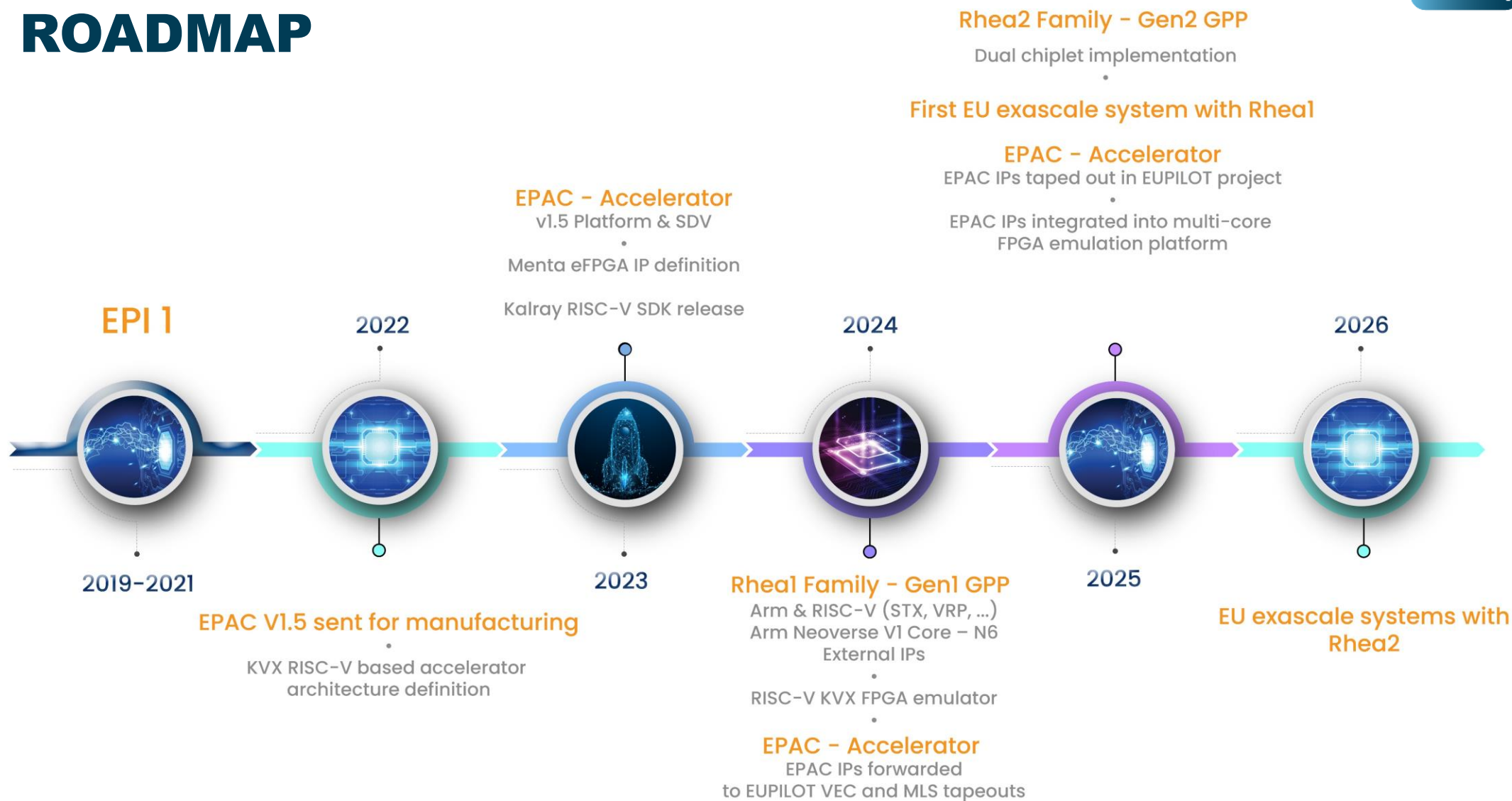


(more to come ...)



OUR PERSPECTIVE

ROADMAP



CLOSING OUR TARGETS TO MAKE UE BACK IN THE RACE



Exascale Systems



Pre-Exascale Pilots



EPI:

GPP & Accelerator test chips



EPI2:

GPP V1 Go to Market
Accelerator Demonstrator

Next project(s):
GPP V2 Go to Market
Risc-V xPUs Go to Market (DARE)

2019 – 2021

2022 - 2025

2025 -

A FOUNDATION FOR EU DIGITAL ROADMAP

European silicon
proven IP

Flexible chiplets

Ready for state of
the art AI

Deployment-ready
through pilots

First IPs (2024-2026):

- Build on EPI efforts on ARM & RISC-V-based processors
- From test chips to TRL 9
- EuroHPC exascale systems as first customer

New architectures (2026-2028)

- Stand-alone competitive processors & accelerators
- Building on EU R&D in low power, security,...
- EuroHPC post-exascale system as first customer

Post-exascale(2028-)

- ARM/RISC-V systems based on EU R&D and IPs



THANK YOU

EPI – A FOUNDATION FOR EU SOVEREIGNTY

EPI FORUM



EuroHPC
Joint Undertaking

PLATINUM SPONSORS



EVIDEN



GOLD SPONSORS

