European Processor Initiative announces the successful bring-up of the EPAC1.5 acceleration chip

Barcelona, 8. Nov 2023.

The European Processor Initiative (EPI) https://www.european-processor-initiative.eu/, a project with 30 partners from 10 European countries, with the goal of achieving Europe's independence in HPC chip technologies and infrastructure, is proud to announce the successful Manufacturing and Silicon Demonstration of its EPAC Accelerator chip version 1.5, marking a significant milestone in high-performance computing.

EPAC1.5 is a collection of RISC-V based accelerators designed to push the boundaries of acceleration technologies. This innovative test-chip showcases three distinct approaches to acceleration:

1. General purpose CPU with dedicated vector unit (VPU)
2. Many-core stencil/machine learning accelerator (STX)
3. General Purpose CPU supporting variable precision (VRP)

The EPAC 1.5 design (Figure 1) contains vector processing micro-tiles (VPU) composed of the Avispado RISC-V core designed by SemiDynamics and a vector processing unit designed by Barcelona Supercomputing Center and the University of Zagreb.
Additional micro-tiles contain distributed Home Nodes (HN) and L2 cache slices (L2), designed respectively by Chalmers and FORTH-ICS, that provide a coherent view of the shared memory subsystem.
The chip also includes the Stencil and Tensor accelerator (STX) designed by ETH Zürich and Fraunhofer IIS and the variable precision processor (VRP) designed by CEA.
All accelerators are interconnected with a very high-speed network on chip with multiple crosspoints (XP) and an off-chip link using SERDES technology from EXTOLL.

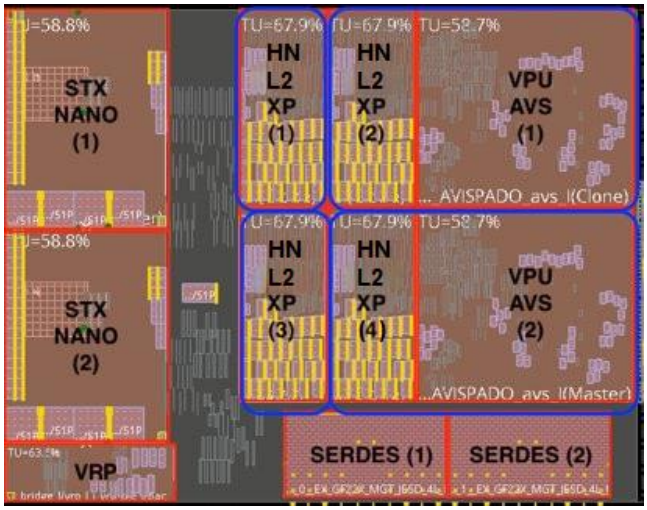

Figure 1: EPAC 1.5 chip floorplan illustrating the major blocks

The physical design was performed by Fraunhofer IIS using GLOBALFOUNDRIES 22FDX low-power technology. The chip is 27mm^2 with 0.3 billion transistors and is hosted on a daughtercard designed by E4 (Figure 2).
The complex bring-up and Linux boot process was carried out at FORTH-ICS, Heraklion, Crete, Greece, and EXTOLL, Mannheim, Germany.

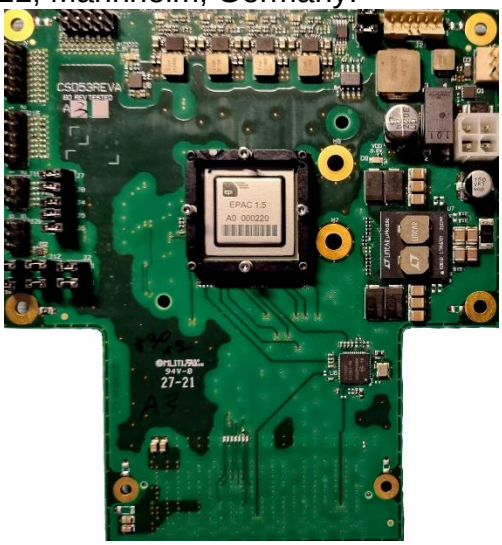

Figure 2: EPAC 1.5 chip on daughtercard

The EPI team demonstrated Linux boot (Ubuntu 22.04 LTS) in both command-line and graphical user interface modes (Figure 3). This demonstration seamlessly integrated the execution of High-Performance Computing (HPC) kernels, harnessing the impressive power of the vector processing unit within the vector accelerator.

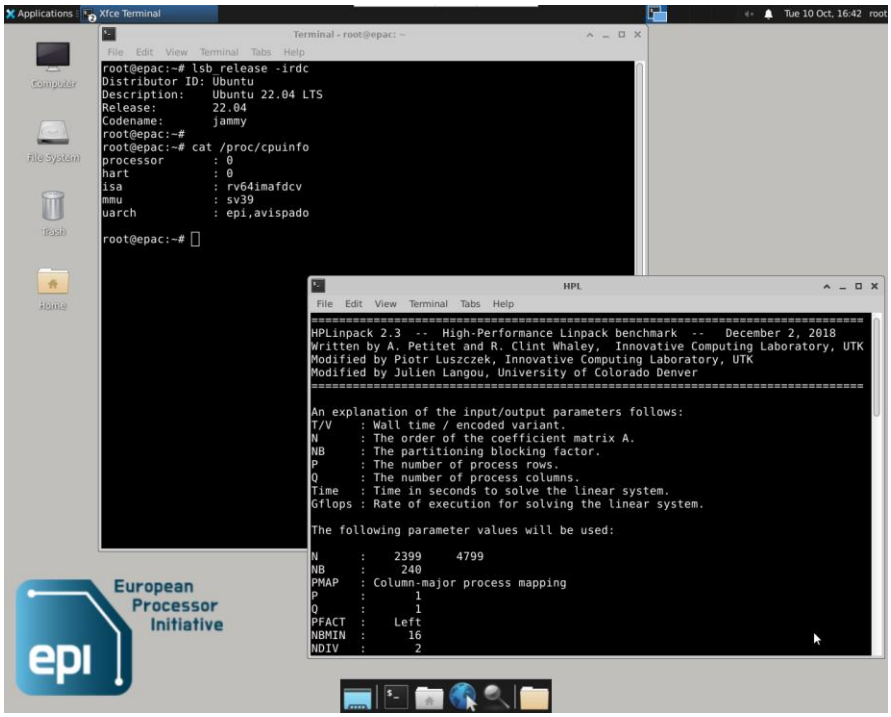

Figure 3: EPAC 1.5 running Ubuntu 22.04 with GUI

"Seeing a standard Linux distribution's GUI boot on a chip developed through collaborative efforts within the European Union consortium has been nothing short of thrilling," declared Filippo Mantovani, the coordinator of the EPAC effort at BSC.

Roger Espasa, founder and CEO of Semidynamics, shared his enthusiasm, stating, "The Avispado core by Semidynamics is an integral part of EPAC, and we take immense pride in our role within this successful EU endeavor. Semidynamics' development of Avispado has been advanced by EPI funding, propelling the EPAC architecture forward over the past four years."

Vassilis Papaefstathiou, Head of the bring-up team at FORTH-ICS, added: “It has been an incredible journey for our team from the very early stages of EPAC 1.5 bring-up to booting Linux and running demanding benchmarks. We are extremely proud to be part of the EPI team and contribute to this success.”

The successful bring-up of EPAC 1.5 is a major step in the development of the EPI common platform, showcasing the variety of accelerators that can be integrated in future European supercomputers to efficiently address a wide range of compute problems.

For more comprehensive details about EPAC, please visit EPI website http://www.european-processor-initiative.eu/accelerator/.

About EPI

The European Processor Initiative (EPI) is a project whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications.

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