EPI - European Processor Initiative

European Processor Initiative Yearly Public Report (2022)

Deliverable 28.3

Version N°1.0

Dissemination level: PUBLIC

http://www.european-processor-initiative.eu/

EuroHPC Joint Undertaking

This project has received funding from the European High Performance Computing Joint Undertaking (JU) under Framework Partnership Agreement No 800928 and Specific Grant Agreement No101036168 EPI SGA2. The JU receives support from the European Union's Horizon 2020 research and innovation programme and from Croatia, France, Germany, Greece, Italy, Netherlands, Portugal, Spain, Sweden, and Switzerland.

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ACKNOWLEDGEMENTS

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Please see http://www.european-processor-initiative.eu/ for more information.

The partners in the project are Bull SAS (Atos), Barcelona Supercomputing Center / Centro Nacional de Supercomputación (BSC), Infineon Technologies AG (IFAG), Semidynamics Technology Services S.L. (SMD), Commissariat à l'Énergie Atomique et aux Énergies Alternatives (CEA), Chalmers Tekniska Högskola AB (Chalmers), Eidegenoessische Technische Hochschule Zürich (ETHZ), Foundation for Research and Technoloy Hellas / Ίδρυμα Τεχνολογίας και Έρευνας (Forth), Grand Équipement National de Calcul Intensif (GENCI), Instituto Superior Técnico (IST), Forschungzentrum Jülich GmbH (FZJ), Alma Mater Studiorum - Università di Bologna (UniBO), Sveučilište u Zagrebu Fakultet Elektrotehnike i Računarstva (UniZG), Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V. (FHG), STMicroelectronics S.r.l. (ST-I), E4 Computer Engineering S.p.A. (E4), Università di Pisa (UniPI), Surf B.V. (SURF), Kalray S.A. (Kalray), EXTOLL GmbH (Extoll), CINECA Consorzio universitario (CINECA), Bayerische Motoren Werke AG (BMW GROUP), Elektrobit Automotive GmbH (ELEKTROBIT), ProvenRun S.A.S. (P&R), Karlsruher Institut für Technologie (KIT), Menta S.A.S. (MENTA), SiPearl S.A.S. (SiPearl), Kernkonzept GmbH (KRNKZPT), Leonardo S.p.A. (LEO), ZeroPoint Technologies AB (ZPT). The content of this document is the result of extensive discussions within the EPI © Consortium as a whole.

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Executive Summary

This document contains data on all Dissemination and Communication activities in the first year of the project from M1 (January 2022) to M12 (December 2022).

The main objective of the dissemination and communication activities in this year was to raise awareness of the EPI project among policy makers, civil society, and the general public. It also aimed to highlight the importance of EPI for the development of the European exascale HPC industry. This was done through participation in scientific and industrial conferences, trade shows and summer schools in the HPC, semiconductor and scientific fields. It is important to emphasize that the presence was targeted to strengthen the EPI brand and recognition among key stakeholders.

As major achievements in the first year of the project, we can hightlight that plenty of dissemination and communication activities took place that started with a joint press release with EuroHPC, EPI and the two pilot projects – EUPEX and EUPILOT. EPI managed to maintain and expand its presence at major events for the HPC community, such as Supercomputing Asia, ISC 2022, Teratec, HiPEAC 2022, and Supercomputing 2022. Partners have participated in many events around the world, showcasing EPI and their work. Also, to emphasize EU integrated focus on collaboration activities between major HPC projects, we made agreements with EUPILOT and EUPEX to be jointly present at major global events to strengthen and continue this collaboration through our online presence (website and social media) and press coverage where EPI took a lead in synchronizing all those activities.

Furthermore, it is important to note that we have taken steps to ensure EPI's trademark protection. Thanks to the trademark, EPI is no longer viewed as a project, but as a brand, which is what all the partners strived for and which puts additional value to the EuroHPC goals.

This report also provides an overview of the materials and channels used for the same purpose. The visual identity and standards were maintained and applied to online communications (website, social media), offline communications (posters, roll-ups, flyers, promotional materials) and internal communications (templates, teasers). These "tools" have also been used to reinforce the EPI brand to a wider audience.

The activities are grouped in:

- Events: organization of a conference, organization of a workshop, exhibition, flyer, training, participation to a conference, participation to a workshop, participation to an event other than a conference or a workshop, brokerage event, pitch event, trade fair, participation in activities organized jointly with other EU projects, other;
- Interviews/press releases/magazines: non-scientific and non-peer-reviewed publication (popularized publication), communication campaign (e.g., TV, radio), video/film, press release, Scientific publications and
- website and social media.

To allow for comprehensive reporting, these categories were grouped under more general types corresponding to the chapters in this document, with tables addressing the activity, participant groups, and key messages directed to those participants.

Keywords

Dissemination, communication, channels of communication, messages, social media, events, journals, interview, media, magazines.

Abbreviations

Acronym	Explanation
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BSC	Barcelona Supercomputing Centre
CA	Consortium Agreement
CORDIS	The Community Research and Development Information Service
CPU	Central processing unit
DG RTD EC	Directorate-General for Research and Innovation in the European Commission
DOA	Description of Action (Technical Annex or Annex I to the Grant Agreement)
GA	Grant Agreement
EC	European Commision
EPI	European Processor Initiative
EPI SGA 1	European Processor Initiative Specific Grant Agreement 1
EPI SGA 2	European Processor Initiative Specific Grant Agreement 2
EU	European Union
EuroHPC JU	European High-performance Computing Joint Undertaking
F2F	Face to face
FPA	Framework Partnership Agreement
HPC	High-performance Computing
IP	Intellectual Property
KPI	Key Performance Indicators
OA	Open Access
ODMs	Original Design Manufacturer
OEMs	Original Equipment Manufacturer
Project Partner	Partner Institution, also referred to as Beneficiary and Party to the Consortium Agreement, or Consortium Partner
PO	Project Officer (EC supervisor of the Grant Agreement)
SC	Steering Committee
SGA1	Specific Grant Agreement 1
SGA2	Specific Grant Agreement 2
SLs	Stream Leaders
SoA	State of the art
UNIZG-FER	University of Zagreb (Faculty of Electrical Engineering and Computing)
WG	Working Group
WP	Work Package (followed by a number)

1 Introduction

EPI SGA2 officially launched in January 2022, with the launch taking place online on January 21, 2022 (the COVID -19 restrictions were still in effect). EuroHPC JU issued a press release in early February about the launch of 3 new research and innovation projects, which further increased the visibility of EPI to the public. In January and February, Phase 2 of the project received significant media and social media attention.

During the initial Phase 1 of EPI, significant global awareness of EPI was achieved. In Phase 2 of the project, D&C activities were planned with the goal of building on the activities of Phase1 and maintaining and improving awareness and understanding of EPI activities that affect both HPC and other areas. In addition, EPI dissemination and communication activities are aligned with EuroHPC JU activities. EPI has also focused on collaboration with the two other projects, the EUPILOT and EUPEX, over the past year.

As mentioned above, EPI reaches a wide range of stakeholders through D&C activities such as attending events, submitting general review articles for publication, giving interviews, writing articles for journals, and issuing newsworthy press releases. WP28's goal is to use social media channels and the EPI website to communicate about these activities. EPI social media channels and the WP28 website are the primary tools for communicating about the goals, plans, roadmap, and content created by partners to interested audiences.

This deliverable presents these materials, D&C activities, and key messages.

The Specific Grant Agreement and the D28.1 Dissemination and Communication Plan identified four goals for dissemination and communication of EPI:

- **Dissemination for Awareness**: The main objective is raising awareness by promoting the project, communicating its vision. Good management of communication streams is key for this purpose.
- **Dissemination for Understanding**: The objective is to contribute to knowledge and understanding by publishing the project results to selected target audiences within the international industry, academic and general public communities.
- **Dissemination for Action**: The goal is to stimulate interaction with external stakeholders and policy makers during the project. External stakeholders can provide relevant support for the EPI project.
- **Integration Driven Dissemination**: Following Integration Driven Development of project research activities all partners will be involved in dissemination activities with the clear goal of full integration of the research, innovation and publication process in both internal and external dissemination including e.g., industrial sessions, panels, exhibitions, etc.

Various dissemination/communication tools were used to implement the above mentioned communication plan and strategies. For EPI, the main task was to be present at all major supercomputing conferences worldwide and to maintain a presence at major RISC-V events. In addition, the dissemination work package ensured that press coverage was positive during the first year of SGA2. This year, there were several interviews with prominent individuals from the project, which helped to give the project a high profile.

It was also important to maintain and consistently apply the visual identity of EPI. Partners were reminded of the importance of the visual identity guidelines at the beginning of the year and the visual identity guidelines were shared with them. The website was continuously updated with activities, presentations, press releases, and other important materials. Social media, another important communication tool, was updated with relevant content and was a very important part of the collaboration with other EU projects and initiatives. Throughout the year, EPI has managed to maintain excellent collaboration with key stakeholders.

The activities of D&C have further strengthened the cohesion among the project partners and made them feel part and actors of an important project.

In the chapters of this report, all dissemination and communication activities are presented with the key messages that the members of EPI have communicated to the audience when participating in events, publishing articles, giving interviews and submitting scientific publications.

2 Visual identity

As mentioned earlier, the visual identity of EPI (including the logo and font) was applied to all graphic materials in Phase 2. This year, the dissemination team created new posters and flyers that were updated with the current EPI roadmap and aligned with partner institutions' visual guidelines (e.g., changes to partner logos).

Figure 1. EPI project logo

Promotional materials

Promotional and informational materials were acquired and distributed at every available opportunity. With the lifting of COVID-19 related restrictions, there are now many more opportunities to distribute promotional materials - phone hangers, USB sticks, lanyards, pre-flight removal key chains, and flyers.

Figure 2. EPI Poster at Teratec 2022

Figure 3. EPI Flyer

EPI Trademark

Steps have been taken to ensure the protection of the EPI trademark. Thanks to the trademark, EPI is no longer seen as a project but as a brand, which was the aim of all partners and adds value to the objectives of EuroHPC JU. We can confirm that the EPI logo is registered in the European Union, the United Kingdom and Switzerland as an extension of the original registration in France.

Designated countries	**Suisse, Union Européenne, Royaume Uni**
Filing / Registration Number:	**1681547 / 1681547**
Filing and Registration Date :	**8 June 2022 / 8 June 2022**
Basis registration :	**France – N°224839034 of 31 January 2022**
Classe(s) :	**9, 35, 42, 45**
Notification date :	**8 September 2022**
Next renewal date :	**8. June 2032**

Figure 4. EPI trademark protection

3 Reports on main D&C activities

In D28.1 Dissemination and Communication Plan, the Consortium identified a list of D&C activities to be undertaken to maintain and improve awareness and understanding of EPI activities that affect both HPC and other areas.

3.1 Events

The consortium also participated in numerous events this year, in the same two categories as in Phase 1:

1) Partners who presented EPI on behalf of the entire consortium,

2) Partners who attended events in their own capacity but took the opportunity to promote EPI,

EPI was present at key events such as Supercomputing Asia, Euro HPC Summit Week 2022, Spring 2022 RISC-V Week, ISC High Performance 2022, Forum Teratec 2022, HiPEAC 2022, and Supercomputing 2022. EPI also presented a full tutorial at the HiPEAC 2022 conference in Budapest, Hungary.

The following table (Table 1) provides a complete list of all events where the consortium has taken the opportunity to advertise EPI and share project results with the scientific and industrial community and potential users. The table lists the events, the materials presented at these events (whether it was an exhibition or a presentation/lecture), the main group of participants per sector (academia, industry, civil sector, media, customers, etc.), and the main message conveyed by EPI to these participants.

All events have been uploaded on the dedicated page on the website here: https://www.european-processor-initiative.eu/events/ as well as they have been promoted via the dedicated social media channels.

In addition to the information listed here, several industry partners of EPI also inform WP28 about face-to-face or virtual meetings with their respective customers, which are not officially reported due to the confidentiality requiremements of their own institutions and related discussions with industry.

Table 1. Events report

Date	Event	Link	Partner	Activity, materials used	Key message for attendees on EPI
11 January 2022, online	IEEE Computer Society Israel Webinar	https://ieee.org.il/event/monthly-webinar-the-european-processor-initiative-epi-project/	Jesus Labarta (BSC)	RISC-V vector processor in EPI	Jesus Labarta provided in his presentation a vision on HPC, towards holistic Co-design and talked about architecture and Software Development Vehicles in EPI.
23 February 2022, Bologna, Italy	The European Commissioner for Innovation visits the Technopole in Bologna	https://www.cineca.it/en/hot-topics/visit-Gabriel	Andrea Bartolini (UNIBO)	The European Commissioner for Innovation visits the Technopole in Bologna	Andrea Bartolini and the European Commissioners visit the CINECA site where the Leonardo supercomputer was installed. Later they moved to a meeting on the role of EPI in the European supercomputing system.
1-3 March 2022, Singapore	Supercomputing Asia	https://www.sc-asia.org/	Jean-Marc Denis (SiPearl)	EPI Booth	Introducing Europe as innovation leader in the future Exascale age
1-3 March 2022, Singapore	Supercomputing Asia/Conga 2022	https://www.sc-asia.org/conga/	Federico Rossi (UNIPI)	Small reals representations for Deep Learning at the edge: a comparison	Federico Rossi presented a publication at Conga 2022. The paper presents results using posits in several neural networks and datasets, showing the small accuracy degradation between 32-

					bit floats and 16-bit (or even 8-bit) posits, comparing the results also against the bfloat family.
1-3 March 2022, Singapore	Supercomputing Asia/ Conga 2022	https://www.sc-asia.org/conga/	Benoit Dupont de Dinechin (Kalray)	A Posit8 Decompression Operator for Deep Neural Network Inference	We propose a hardware operator to decompress Posit8 representations with exponent sizes 0, 1, 2, 3 to the IEEE 754 binary 16 (FP16) representation. The motivation is to leverage the tensor units of a manycore processor that already supports FP16.32 matrix multiply-accumulate operations for deep learning inference. According to our experiments, adding instructions to decompress Posit8 into FP16 numbers would enable to further reduce the footprint of deep neural network parameters with an acceptable loss of accuracy or precision. We present the design of our decompression operator and compare it to lookup-table implementations for the technology node of the targeted processor.

1-3 March 2022, Singapore	Supercomputing Asia/ Conga 2022	https://www.sc-asia.org/conga/	Marco Cococcioni (UNIPI)	CoNGA technical committee	Marco Cococcioni participated as a member of CoNGA 2022 technical committee.
1-3 March 2022, Houston, Texas, USA	2022 Energy HPC Conference	https://2022energyhpcconference.sched.com/event/sOtL	Franz-Josef Pfreundt and Jens Krüger from Fraunhofer	Talk titled: "The STX Processor – Hardware Acceleration for RTM."	Fraunhofer ITWM presented STX Hardware and Software Toolchain related activities of the EPI project during the 2022 Energy HPC Conference, one of the major oil and gas conferences.
3 March 2022, Grenoble, France	Journée de l'IA embarquée	https://www.minalogic.com/panorama-de-lintelligence-artificielle-embarquee-retour-sur-la-journee-du-3-mars/	Renaud Stevens (Kalray)	EMBEDDED AI for automotive and industrial applications	One of the main challenge for future embedded AI solutions (automotive, networks, industry) is to design complex intelligent systems that are capable of analyzing large amounts of data in real time and integrating several critical applications on a same chip.
14-23 March 2022, online	DATE 2022	https://www.date-conference.com	KIT	KIT will present a paper about the results carried out in EPI SGA1	On DATE we had the chance to present our final results for the eFPGA derived from SGA1. Eventhough it was an online meeting we got great feedback and questions.
14-23 March 2022, online	DATE 2022	https://www.date-conference.com	Denis Dutoit (CEA)	Chiplet Based Architecture: an	CEA's RISC-V based VRP/VXP accelerator

				answer for Europe Sovereignty in Computing?	supporting extended precision floating-point arithmetics (more than 128 bits) enable higher stability and performance on commonly used HPC linear and eigenvalues scientific solvers.
14-23 March 2022, online	DATE 2022	https://www.date-conference.com	Victor Jimenez (BSC)	Design Verification of a RISC-V Vector Accelerator	The partners haven't delivered the key message.
21 March 2022, Buenos Aires, Argentina	Presentation about European Processor Initiative project	/	Mario Kovač (UNIZG)	Presentation about European Processor Initiative project	Mario Kovač, Director of the HPC Architecture and Application Research Center and Chief Communications Officer of the European Processor Initiative, held a presentation at the University of Buenos Aires on March 21, 2022. The presentation showcased the EU Exascale HPC strategy and EuroHPC JU ambitious mission.
22-24 March 2022, Paris, France	EuroHPC Summit Week 2022 / PRACEdays22	https://prace-ri.eu/event/eurohpc-summit-week-2022-pracedays22/	Fabrizio Magugliani, Daniele Gregori (E4)	Presentations	E4 is an active member of the EPI project for the development of the prototype.
22-24 March 2022, Paris, France	EuroHPC Summit Week 2022 / PRACEdays22	https://prace-ri.eu/event/eurohpc-summit-week-2022-pracedays22/	John D. Davis (BSC)	Building an Open HPC Ecosystem	The partners haven't delivered the key message.
22-24 March	EuroHPC Summit	https://prace-	Etienne Walter (Atos)	Participation at the	Etienne Walter held a

2022, Paris, France	Week 2022 / PRACEdays22	ri.eu/event/eurohpc-summit-week-2022-pracedays22/		European HPC ecosystem workshop	brief presentation at EuroHPC Summit Week 2022 about European Processor Initiative. The presentation showcased EPI SGA2 goals in the upcoming years and EPI's role in European HPC ecosystem.
22-24 March 2022, Paris, France	EuroHPC Summit Week 2022 / PRACEdays22	https://prace-ri.eu/event/eurohpc-summit-week-2022-pracedays22/	Jean-Marc Denis, Craig Prunty, Anna Riverola (SiPearl)	Presence at the event	Informal meetings to consolidate the project visibility among stakeholders at the European level: Prace, ETP4HPC, EuroHPC and the European Commission.
22-24 March 2022, Paris, France	EuroHPC Summit Week 2022 / PRACEdays22	https://prace-ri.eu/event/eurohpc-summit-week-2022-pracedays22/	Jean-Marc Denis (SiPearl)	Conference about "Sovereignty in motion"	The topic of the conference "Sovereignty in motion" aims to build a broader awareness about the EPI project especially for Politics.
22-24 March 2022, Paris, France	EuroHPC Summit Week 2022 / PRACEdays22	https://prace-ri.eu/event/eurohpc-summit-week-2022-pracedays22/	Anna Riverola (SiPearl)	PRACE & ETP4HPC Workshop on HPC Education and Training - Industry Perspectives	The participation to the workshop "Skills needs of "Supply-side" industry" is dedicated to consolidating the project visibility through a transverse topic "Education & training" among the different stakeholders at European level.
23-25 March 2022, online	TechTour Future22	https://future22.techtour.com/	Yoan Dupret (Menta)	Pitch	Mention of EPI project (HPC (Atos, SiPearl), Automotive (BMW,

					Infineon). Message: "SEVERAL DEFENSE & SPACE, EDGE SERVERS AND AUTOMOTIVE COMPANIES helped us prove the technology". Great testimonial design-wins across the world.
28-30 March 2022, online	HPC User Forum Spring 2022	https://www.hpcuserforum.com/event/hpc-user-forum-spring-2022/	John D. Davis (BSC)	RISC-V in Europe: The Road to an Open Source HPC Stack	John D. Davies had a presentation about RISC-V in Europe. He talked about the HPC Vision and RISC-V HPC Research in Europe.
28-30 March 2022, online	HPC User Forum Spring 2022	https://www.hpcuserforum.com/event/hpc-user-forum-spring-2022/	Craig Prunty (SiPearl)	Conference: Innovative Technologies: New Directions in Processors for HPC	The topic of the conference "Trends & design choices for the European microprocessor" aims to facilitate the understanding of the EPI project progress and achievements.
2-6 April 2022, Seoul, South Korea	HPCA 2022	https://hpca-conf.org/2022/	ZeroPoint Technologies	Presentation	ZeroPoint Technologies – Remove Waste. Release the Power. Digitalization quickly accelerates energy consumption. In 2030, the ICT (Information and Communications Technology) sector is projected to stand for more than one-fifth of the global electricity demand. Maximizing

					performance per watt in servers and smart devices is critical to breaking the trend. ZeroPoint technology delivers up to 50% more performance per watt by removing unnecessary information from microchips in data centers (CPU) and smart devices (SoC), meaning that: • Data centers can maximize performance and reduce energy consumption. • Smart device developers can maximize performance and user experience without compromising on battery life.
2-6 April 2022, Seoul, South Korea	HPCA 2022	https://hpca-conf.org/2022/	Francesco Minervini (BSC)	Vitruvius: An Area-Efficient RISC-V Decoupled Accelerator with 256-DP Element Vectors	The partners haven't delivered the key message.
7 April 2022, Paris, France	Atos AI & Business computing and HPC & Quantum University 2022	/	Craig Prunty (SiPearl)	Conference: SiPearl-Rhea, the European High-Performance Microprocessor	The topic of the conference "SiPearl-Rhea, the European High-Performance Microprocessor" aims to raise the awareness about the project among

					the employees of one of EPI member, Atos, ans its business partners.
7 April 2022, Paris, France	Atos AI & Business computing and HPC & Quantum University 2022	/	Jean-Marc Denis and Craig Prunty (SiPearl)	Booth with EPI logo on a poster	It is intented to raise the awareness about the project among the employees of one of EPI member, Atos, ans its business partners.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Roger Espasa (Semidynamics)	Atrevido: SemiDynamics Out-of-Order RISC-V Core	Semidynamics introduced its Out-of-order RISC-V Atrevido core supporting RVV1.0 to be used in EPI2 and PILOT.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Daniele Gregori and Fabrizio Magugliani (E4)	Sponsors of the conference; Presentation at the Plenary Session	E4 is an active member of the EPI project for the development of the prototype.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Roger Ferrer (BSC)	Presentation - SW Toolchain for RISC-V Vector Extensions	The RISC-V Vector Extension (RVV) provides vector capabilities to the RISC-V ecosystem. It does this by providing a very flexible and rich ISA which features vector length and masking support. This flexibility comes with some challenges in implementing it in compilers. In this talk we will see how we tackled these issues in the context of the EPI

					project, which ideas were ultimately implemented in upstream LLVM and which didn't. With code generation well understood now, the focus shifts on how to make good use of the extension in the compiler via vectorization. We will see the ongoing work in the LLVM Loop Vectorizer, what is there and what is still missing.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Andrea Bartolini (UNIBO)	Presentation - RISC-V based Power Management Unit for an HPC processor	The RISC-V week is based on collaborations about open-source hardware. Regarding the European Processor Initiative (EPI), Andrea Bartolini presented ControlPULP. This study is a complete, open-source HW/SW RISC-V parallel power controller system platform for High-Performance Computing processors.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Jesus Labarta (BSC)	Presentation - The Accelerator Tile of European Processor Initiative	The European Processor Initiative (EPI) project aims at developing European processor technology for High Performance Computing (HPC) and emerging application areas. An important objective of the

					project is to develop a fully owned implementation of accelerators based on RISC-V cores. The resulting EPAC architecture integrates generic RISC-V vector cores plus other more specialized accelerator component (STX) also based on RISC-V targeting AI and stencil kernels acceleration plus a RISC-V processor (VRP) with support for variable and high precision arithmetic. The talk will introduce the fundamental vision behind the design and the overall resulting architecture. The project has produced a test chip in GF 22 nm technology, featuring 4 vector cores, 2 STX clusters and one VRP processor. In parallel, an FPGA implementation of the vector core and memory subsystem has been implemented to be used as a software development vehicle (SDV), continuous

					integration (CI) and co-design support infrastructure. This system runs as stand alone self hosted Linux node where general purpose application from the HPC but also other domains can be run. I will report some initial results of these evaluations and comparisons to other state of the art architectures.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Francesco Minervini (BSC)	Presentation - Vitruvius: An Area-Efficient RISC-V Decoupled Vector Accelerator for High Performance Computing	The availability of domain-specific instruction set extensions, like vector processing, make RISC-V a good candidate for supporting the integration of specialized hardware in processor cores. This talk presents Vitruvius, the first RISC-V vector accelerator developed at BSC for the Supercomputing domain, as part of the EPI project. Vitruvius implements the RISC-V vector extension specification V0.7.1. and can be easily connected to a scalar core using the Open Vector Interface (OVI) standard in a plug-and-play fashion.

					Vitruvius natively supports long vectors: 256 Double Precision (DP) floating-point elements in a single vector instruction. It is composed of a set of identical vector pipelines (lanes), each containing a slice of the Vector Register File (VRF) and functional units (one integer, one floating-point). It adopts a novel hybrid in-order/out-of-order execution scheme, supported by vector register renaming and arithmetic/memory instruction decoupling. When configured with eight vector lanes, Vitruvius reaches a maximum frequency of 1.25 GHz when synthesized using GLOBALFOUNDRIES 22FDX FD-SOI. The silicon implementation has a total area of 1.13 mm2 and total estimated power around 1W.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Matheus Cavalcante (ETHZ)	Presentation - The RISC-V based Stencil Tensor Accelerator of EPI	ETH Zurich is working on cluster-based many-core domain specific accelerators around its open-source 32bit RISC-

					V Snitch cores.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	César Fuguet-Tortolero (CEA)	Presentation - VRP/VXP: VaRiable eXtended Precision RISC-V Accelerator for High-Precision	CEA's RISC-V based VRP/VXP accelerator supporting extended precision floating-point arithmetics (more than 128 bits) enable higher stability and performance on commonly used HPC linear and eigenvalues scientific solvers.
3-5 May 2022, Paris, France	Spring 2022 RISC-V Week	https://open-src-soc.org/2022-05/	Nick Kossifidis (FORTH)	Demystifying the RISC-V Linux software stack	• It is challenging to support an architecture as modular as RISC-V, while also keeping track of relevant Linux kernel updates. • Overview of key kernel features that are currently supported, ongoing work on new features. • Experience on upstream contributions as part of FORTH's work on the system software support for EPI prototypes.
16-19 May 2022, Karolinka, Czech Republic	High Performance Computing in Science and Engineering 2022 conference (HPCSE 2022)	https://hpcse.it4i.cz/HPCSE22/	Daniele Cesarini, Federico Ficarelli, Federico Tesser, Andrea Piserchia, Fabio Affinito (CINECA)	Microarchitecture performance assessment and energy monitoringof MaXcodes through Linux Perf and power management API	Presentation of EPI codesign outcomes and energy efficiency strategies.

				interfaces	
17-19 May 2022, Torino, Italy	CF 2022	https://www.computingfrontiers.org/2022/	Federico Ficarelli, Mohsen Sadegh, Martin Molan (UNIBO)	Meet Monte Cimone: Exploring RISC-V High Performance Compute Clusters	In the EPI context, Cineca, UniBo, and E4 presented the work done to design, and implement deploy Monte Cimone, the world's first fully RISC-V production HPC cluster: this system has been and is currently used as a development and testing platform for EPI outputs on widespread HPC applications like quantumESPRESSO, HPC industry benchmarks, the EXAMON power and energy monitoring infrastructure for HPC deployments data analytics and RISC-V optimized toolchains
25-27 May 2022, Alba, Italy	33rd Parallel CFD International Conference	https://parcfd2022.org/	Fabrizio Magugliani (E4)	MiniSimposio MS3: Solutions, ideas, and perspectives for CFD, HPC and Exascale computing	E4 is active in the development of the prototype based on the EPI processor which may be used by the CFD community.
28 May - 1 June 2022, Austin, USA (virtual)	IEEE International Symposium on Circuits and Systems (ISCAS)	https://www.iscas2022.org/	Nuno Neves (IST)	Presentation (virtual) of the paper entitled "Unified Posit/IEEE-754	A new vector MAC architecture in light of the transprecision computing trend. It offers variable-precision SIMD

				Vector MAC Unit for Transprecision Computing"	operations and maintains a unified support for the Posit and IEEE formats.
29 May - 2 June 2022, Hamburg, Germany	2022 ISC High Performance	https://www.isc-hpc.com/	Daniel Hofman and Nikolina Lednicki (UNIZG)	EPI booth	Presentation of European Processor Initiative, project goals and meetings with interested attendees.
29 May - 2 June 2022, Hamburg, Germany	2022 ISC High Performance	https://www.isc-hpc.com/	Fabrizio Magugliani and Daniele Gregori (E4)	E4 booth, presentations	E4 is an active member of the EPI project for the development of the prototype, which will be used in several EuroHPC projects.
29 May - 2 June 2022, Hamburg, Germany	2022 ISC High Performance	https://www.isc-hpc.com/	Daniele Cesarini, Federico Ficarelli, Federico Tesser, Andrea Piserchia, Fabio Affinito (CINECA)	Performance Assessment and Energy Efficiency of MaXCodes	Presentation of EPI mini-application work and codesign activities.
29 May - 2 June 2022, Hamburg, Germany	2022 ISC High Performance	https://www.isc-hpc.com/	Estela Suarez (Juelich)	Workshop speaker, Birds of a Feather (BoF) session leader	General project overview
29 May - 2 June 2022, Hamburg, Germany	2022 ISC High Performance	https://www.isc-hpc.com/	Philippe Notton, Jean-Marc Denis, Craig Prunty, Vincent Casillas (SiPearl)	Meetings during the begining of ISC (2 days) with an introductive part dedicated to EPI	Meetings to promote the achievements and future product of the project to stimulate the future demand.
29 May - 2 June 2022, Hamburg, Germany	2022 ISC High Performance	https://www.isc-hpc.com/	Fraunhofer	Booth	Fraunhofer ITWM presented STX Hardware and Software Toolchain related activities of the EPI project.
2 June 2022,	MODA22: 3rd ISC Monitoring and	https://easychair.org/cfp/MODA22	Mohsen Sadegh (UNIBO)	Rule-based Thermal Anomaly	The work is focused on the power management

Hamburg, Germany	Operational Data Analytics Workshop			Detection for Tier-0 HPC Systems	strategy of the European Processor Initiative. It aims to improve the data center performance by predicting the thermal anomalies in advance.
14 June 2022, Paris, France	Scaling Up with the EIC	/	Philippe Notton (SiPearl)	Announcement of SiPearl being the first equity investment of EIC Fund. Intervention on stage of Philippe Notton explaing SiPearl and EPI.	Introducing the project and its members to an uninitiated audience of venture capitalist, EU and French officials, entrepreneurs.
14 - 15 June 2022, Paris, France	Forum Teratec 2022	https://teratec.eu/gb/forum/inscription-april.html	Josip Ramljak and Luka Mrković (UNIZG)	EPI Booth	Presentation of European Processor Initiative, project goals and meetings with interested attendees.
14 - 15 June 2022, Paris, France	Forum Teratec 2022	https://teratec.eu/gb/forum/inscription-april.html	Philippe Notton, Jean-Marc Denis, Craig Prunty, Romain Dolbeau, Marie-Anne Garigue, Grégory Bosson	Booth with EPI logo on the wall	Informal meetings to consolidate the project visibility among stakeholders at the European level, Engineering students and Academics.
14 - 15 June 2022, Paris, France	Forum Teratec 2022	https://teratec.eu/gb/forum/inscription-april.html	Jean-Marc Denis (SiPearl)	Presentation "Designing microprocessors for the exascale and artificial intelligence era: SiPearl approach" mentioning EPI	The topic of the presentation is positioning Europe as innovation leader in the future Exascale age.
14 - 15 June 2022, Paris,	Forum Teratec 2022	https://teratec.eu/gb/forum/inscription-	Jean-Marc Denis (SiPearl)	Subject: Key power	The topic of this workshop is to promote

France		april.html		consumption metrics for general purpose microprocessors in the exascale era	the results of the project.
18-22 June 2022, New York, USA	ISCA 2022	https://iscaconf.org/isca2022/	ZeroPoint Technologies	Presentation	ZeroPoint Technologies – Remove the Waste. Release the Power. Digitalization quickly accelerates energy consumption. In 2030, the ICT (Information and Communications Technology) sector is projected to stand for more than one-fifth of the global electricity demand. Maximizing performance per watt in servers and smart devices is critical to breaking the trend. ZeroPoint technology delivers up to 50% more performance per watt by removing unnecessary information from microchips in data centers (CPU) and smart devices (SoC), meaning that: • Data centers can maximize performance and reduce energy consumption. • Smart device

					developers can maximize performance and user experience without compromising on battery life.
19-24 June 2022, Les Fermes de Marie, Megève, France	MPSoC 2022	http://mpsoc-forum.org/	Eric Monchalin (Atos)	Presentation titled "European Sovereignty for Cloud continuum and HPC"	Eric Monchalin held a presentation at MPSoC 2022 titled: Cloud Continuum & Swarm Computing. Moreover, presentation has showcased topics such as building a leading European HPC ecosystem and the ecosystem road to EU exascale.
20-22 June 2022, Budapest, Hungary	HiPEAC 2022	https://www.hipeac.net/2022/budapest/#/	ZeroPoint Technologies	Presentation	ZeroPoint Technologies – Remove Waste. Release the Power. Digitalization quickly accelerates energy consumption. In 2030, the ICT (Information and Communications Technology) sector is projected to stand for more than one-fifth of the global electricity demand. Maximizing performance per watt in servers and smart devices is critical to breaking the trend. ZeroPoint technology delivers up to 50% more

					performance per watt by removing unnecessary information from microchips in data centers (CPU) and smart devices (SoC), meaning that: • Data centers can maximize performance and reduce energy consumption. • Smart device developers can maximize performance and user experience without compromising on battery life.
20-22 June 2022, Budapest, Hungary	HiPEAC 2022	https://www.hipeac.net/2022/budapest/#/	Andrea Bartolini and Giovanni Bambini (UNIBO)	EPI Tutorial Session: A Scalable RISC-V Power Controller Platform for HPC Processors	In the EPI context, UNIBO team presented a work-in-progress framework for the HW/SW co-design of a power thermal management controller. The framework pairs a trace-driven HPC processor simulation with an FPGA microcontroller IP instantiation for ControlPULP, and it is connected to the Examon tool for HPC data analytics.
20-22 June 2022, Budapest, Hungary	HiPEAC 2022	https://www.hipeac.net/2022/budapest/#/	Roger Espasa (Semidynamics)	Booth and Roger Espasa is also presenting Semidynamics	Semidynamics presented its roadmap, including Avispado, Atrevido and the vector

				products in an industrial sesion at the Conference	unit. Atrevido will be used in EPI2 and PILOT.
20-22 June 2022, Budapest, Hungary	RAPIDO 2022 workshop/HIPEAC	https://rapidoworkshop.github.io/2022/index.html	Fatma Jebali, Oumaima Matoussi, Arief Wicaksana, Amir Charif, Lilia Zaourar (CEA)	Decoupling processor and memory hierarchy simulators for efficient design space exploration	A simulation approach based on decoupling processor emulation and memory hierarchy simulation for the purpose of efficiency with VPSim tool. Our approach reduces the overhead of simulating complex memory hierarchies without sacrificing the accuracy of the performance evaluation results.
20-22 June 2022, Budapest, Hungary	RAPIDO 2022 workshop/HIPEAC	https://rapidoworkshop.github.io/2022/index.html	Lilia Zaourar (CEA)	European Processor Initiative: a full co-design approach based on multi-level simulation	In EPI, processor development is driven via co-design, a bi-directional and iterative interaction process between application owners, hardware- and system-software developers. The success of the co-design strategy relies on establishing an efficient methodology to tightly connect application and benchmark experts with the hardware and software development team and across the various members of the project using differents

					tools and level of simulation.
20-22 June 2022, Pisa, Italy	PhD School	https://phd.dii.unipi.it/formazione/item/4627-prof-massimo-alioto,-ece-department,-national-university-of-singapore-singapore,-ultra-low-power-integrated-systems-for-green-growth-to-the-trillion-scale-,-20-22-june-2022.html	Sergio Saponara (UNIPI)	Prof. Massimo Alioto, ECE Department, National University of Singapore - Singapore, "Ultra-low power integrated systems for green growth to the trillion scale"	The course focuses on ultra-low power integrated circuit design for distributed and decentralized systems (e.g., IoT, AIoT), and in particular on the design of chips for edge nodes. The course provides an insight into system requirements imposed by real-world applications, the fundamentals to understand the related challenges, and advanced design ideas to address them. Several aspects are discussed from a design viewpoint, ranging from ultra-low power system architectures, architectures and circuits for processing, data sensemaking (e.g., machine learning on a chip), energy harvesting, on-chip power conversion, sensor interfaces and wireless communications.
23 June 2022, Palaiseau, France	Association Aristote	https://www.association-aristote.fr/tous-les-evenements/	Frédéric Hannoyer (SiPearl)	Séminaire "Transition numérique et écologique : un	Conference about "The low-power microprocessor" introducing the project,

				oxymore ?"	its results and future product to an unitited audience of academics, students and politics.
30 June – 1 July 2022, Barcelona, Spain	Barcelona Build vs Buy HPC Summit	https://www.bsc.es/news/events/barcelona-build-vs-buy-hpc-summit-3b4hpc	Jean-Marc Denis (SiPearl)	Keynote "SiPearl and EPI: how a European research & innovation project has become a successful industrial story: a chapter about EPI.	The target of this keynote is to consolidate the relationships between the project and some of its target audiences: scientists, scientific bodies, industry…
4-6 July 2022, Pafos, Cyprus	ISVSLI 2022	http://www.eng.ucy.ac.cy/theocharides/isvlsi22/index.html	Tim Hotfilter, Fabian Kreß, Fabian Kempf and Jürgen Becker, Imen Baili (KIT)	Data Movement Reduction for DNN Accelerators: Enabling Dynamic Quantization Through an eFPGA	On ISVLSI we had a nice session about European funded projects. Out talk made the current efforts and technical highlights of EPI visible to the VSLI community who attended the conference. It was a great opportunity after two years online meetings!
6-13 July 2022, Bologna, Italy	ICHEP 2022	https://www.ichep2022.it/#.	Daniele Gregori (E4)	Booth with a poster	E4 is an active member of the EPI project for the development of the prototype, which will be used in several EuroHPC projects.
17-22 July 2022, L'Aquila, Italy	School on Computational Fluid Dynamics & SuperComputing	https://www.cfdparschool.com/	Fabrizio Magugliani (E4)	Presentation at the Plenary Session	E4 is active in the development of the prototype based on the EPI processor which may be used by the CFD community.
20-27 July	Summer School -	https://www.unipi.it/inde	Sergio Saponara (UNIPI)	Organisation of a	The summer school

2022, Pisa, Italy	University of Pisa: Enabling Technologies for Industrial Internet of Things	x.php/engineering/item/6869-summer-school-internet-of-things		Summer School	provides theoretical and practical lessons about recent advances in enabling technologies for electronics, electromagnetics, future wireless transceivers and wireless sensor networks, systems, edge and cloud computing, networks in scenarios such as IoT, Industry 4.0, Cyber-PhysicalSystems (CPS), autonomous vehicles, robots.
2-4 August 2022, Santa Clara, USA	Flash Memory Summit	https://flashmemorysummit.com/	Tim Lieber (Kalray)	Accelerating data services and storage disaggregation thanks to DPUs	NVMe protocol is state-of-the-art technology that enhances the performance benefits of flash-based storage by removing performance bottlenecks. To fully exploit the performances of NVMe devices, storage nodes must dedicate significant portions of compute resources towards storage functions. This is especially true when storage services such as LVM, data protection, data reduction or data cryptography are employed. Performance of both local and

					NVMeoF based disaggregated storage can be adversely affected by system bottlenecks which reduces the expected benefits to TCO of modern NVMe architectures. This is amplified further in a virtualized environment, where hypervisors must offer storage virtualization and disaggregation to Virtual Machines. In this presentation we detail the benefits of using DPUs: demonstrating how DPU-based acceleration cards like the Kalray Smart Storage Accelerator PCIe card can seamlessly offload storage services as well as storage disaggregation by exposing many NVMe controllers on the PCIe bus while taking control of local or remote SSDs and share concrete outcomes for the most demanding workflows in domains such as AI, HPC and High-End Media

					Production.
22 - 25 August 2022, Trieste, Italy	CCTA 2022 Trieste	https://ccta2022.ieeecs.org/	Giovanni Bambini, Christian Conficoni, Andrea Tilli, Luca Benini, Andrea Bartolini (UNIBO)	Modeling the Thermal and Power Control Subsystem in HPC Processors	The work presented is a mathematical modeling of an HPC processor aimed at fast Hardware-in-the-Loop simulations. This model was used to compare the performance of a port of the IBM Power9 control algorithm with a custom cascade loop control used inside ControlPULP. The work is supported by the European processor initiative.
24-26 August 2022, Shangai, China	RISC-V Summit China 2022	https://riscv-summit-china.com/	Roger Espasa (Semidynamics)	Presentation - Semidynamic's RVV1.0 Out-of-order Vector Unit	Semidynamics presented details of its RVV1.0 vector unit. A part of this work, namely the OVI2.0 interface, will be used in EPI2 and PILOT.
29 August - 2 September 2022, Barcelona, Spain	2022 ACM Summer School on HPC Computer Architectures for AI and Dedicated Applications	https://europe.acm.org/2022-hpc-summer-school	Mario Kovač (UNIZG)	EPI presentation	Mario Kovač, Director of the HPC Architecture and Application Research Center and Chief Communications Officer of the European Processor Initiative, held a presentation at the ACM Summer school. The presentation showcased the EPI project and its objectives. EU Exascale HPC

					strategy and EuroHPC JU ambitious mission.
29 August - 2 September 2022, Barcelona, Spain	2022 ACM Summer School on HPC Computer Architectures for AI and Dedicated Applications	https://europe.acm.org/2022-hpc-summer-school	BSC	Organisation of a Summer School	The 2022 ACM Europe Summer School on "HPC Computer Architectures for AI and Dedicated Applications" took place in Barcelona from 29 August – 2 September 2022. The Barcelona Supercomputing Center (BSC-CNS) hosted the 3rd edition of the school. Distinguished scientists in the HPC field gave lectures and tutorials addressing architecture, software stack and applications for HPC and AI, invited talks, a panel on The Future of HPC and a final keynote by Prof Mateo Valero. On the last day of the week, the ACM School merged with MATEO2022 ("Multicore Architectures and Their Effective Operation 2022"), attended by world-class experts in computer architecture in the HPC field. The school was possible thanks to the direct financial support from

					ACM, BSC, EPI and the industrial sponsors: Huawei, IBM and Lenovo. RES, the national Spanish supercomputing network, also provided financial support. The project RISC2 offered financial support for Latin American students to attend the school. The summer school addressed young computer science researchers and engineers and was open to outstanding MSc students.
14 – 15 September 2022, Lyon, France	SIDO Lyon 2022	https://www.sido-lyon.com/	MENTA	Global presentation	Global mention of the EPI project.
19 - 23 September 2022, online	2022 IEEE High Performance Extreme Computing Conference (HPEC)	https://www.aconf.org/conf_181990.html	Benoit Dupont de Dinechin (Kalray)	Computing In-Place FFTs with SIMD Lane Slicing	We present an approach for implementing in-place FFTs on cores fitted with SIMD units and non-temporal load-store units. Loading the input samples with SIMD instructions decimates them in time across the SIMD lanes. A classic FFT implementation is extended to operate on SIMD data rather than

					scalar data and computes the sub-transforms concurrently. This enables efficient exploitation of the SIMD arithmetic and memory access instructions while involving little SIMD lane shuffling. A last FFT stage then recombines in-place the sub-transforms results to produce the output. We illustrate this approach on a Cooley- Tukey radix-4 decimated-in-frequency FFT implementation, which also integrates the two inner loop collapsing optimization of the TI C6x DSP _fft32×32 code that enables software pipelining and the Burrus technique for using bit-reversal in high-radix FFT implementations. Performance evaluations are performed on the Kalray KV3 core, which implements a 64-bit vector-scalar VLIW architecture with level-l cache bypass load instructions.
21-23 September	Jornadas Sarteco	http://www.jornadassarteco.org/?anyo=2022	Roger Espasa (Semidynamics)	Booth: Roger Espasa presented	Semidynamics presented its roadmap,

2022, Alicante, Spain				the company, its products and its activities in the Sarteco-Pro session at the Conference	including Avispado, Atrevido and the vector unit. Atrevido will be used in EPI2 and PILOT.
22-24 September 2022, Trieste, Italy	Trieste Next	https://www.triestenext.it/	Carlo Cavazzoni (Leonardo)	Presentation and panel Discussion	A panel discussion about the importance of supercomputers in the research and development of new materials for industry.
26-27 September, Genova, Italy	ApplePies	https://applepies.eu/	Saponara, Rossi, Cococcioni (UNIPI)	Presentations	The partners haven't delivered the key message.
26-27 September, Genova, Italy	ApplePies	https://applepies.eu/	Carlo Cavazzoni (Leonardo)	Presentation	A presentation about how to enable the potential of High-Performance Computing for engineering application in aerospace and defence.
26 - 30 September 2022, Assisi, Italy	13th International Conference on Relativistic Effects in Heavy-Element Chemistry and Physics	https://www.rehe2020.it/	Daniele Cesarini (CINECA)	The Leonardo Supercomputer at the Bologna Big Data Technopole and the CINECA's Evolution Roadmap	Presentation of EPI roadmap in the HPC technology contest of CINECA.
3-4 October 2022, Paris, France	International HPC User Forum	https://www.hpcuserforum.com/event-page-international-hpc-user-forum/	Jean-Marc Denis (SiPearl)	Panel HPC in Europe	The topic of the talk "SiPearl vision"aims to position SiPearl and Rhea in the context of the EPI project and the exascale race in Europe.

3-5 October 2022, Lausanne, Switzerland	Co-Design for HPC in Computational Materials and Molecular Science E151	https://www.cecam.org/workshop-details/1113	Jean-Marc Denis (SiPearl)	How Rhea1 has been co-designed for the HPC applications, with specific focus onmaterial and molecular science	Aims of the talk is to stimulate the demand for the new technological solutions developped within EPI.
3-5 October 2022, Lausanne, Switzerland	Co-Design for HPC in Computational Materials and Molecular Science E151	https://www.cecam.org/workshop-details/1113	Filippo Mantovani (BSC)	The European Processor Initiative: project overview and co-design for RISC-V accelerators.	The European Processor Initiative (EPI) is a project aiming to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications. Specifically, the project is developing a General Purpose Processor and an Accelerator as well as the software layers needed for their adoption and efficient use by the community. The Barcelona Supercomputing Center is promoting and participating in the development of the RISC-V-based accelerator targeting HPC. This talk will provide an overview of the EPI project with particular attention to the

					co-design effort performed with Software Development Vehicles (SDV) while developing the EPI accelerator leveraging the RISC-V vector extension.
11 October 2022, Zagreb, Croatia	Workshop about HPC Processor/Systems design and communication	https://www.linkedin.com/feed/update/urn:li:activity:6985510706620084224	Eric Monchalin, Etienne Walter, Pascale Bernier-Bruna (Atos); Mario Kovač, Igor Piljić, Mate Kovač, Luka Mrković, Josip Ramljak, Hana Ivandić, Nikolina Lednicki (UNIZG)	Workshop	FER and Atos will had an EPI and EUPEX Pilot workshop about HPC Processor/Systems design and communication.
11 October 2022, Zagreb, Croatia	Co-organisation and hosting of a lecture	https://www.linkedin.com/feed/update/urn:li:activity:6985547521175498752	Eric Monchalin (Atos) was presenting; Mario Kovač (UNIZG) organisation of a lecture	Presentation on "European Sovereignty for Cloud Continuum and HPC"	The pace of technological change is faster than ever with a digital revolution underway, enabling the transformation of manufacturing and services, and reshaping entire sectors of the economy. In such a context, the growth of ecosystems of smart machines is a foundation that is enabled by the datacenters, Edge Computing and IoT that become increasingly connected, emerging as a computing continuum. It is a big challenge in itself to bridge the gap between the European strengths and challenges

					to make Europe a leader of this digital revolution. However, much more is possible when a concerted academic, research and industrial effort is developed to break out of the technological locks. It is exactly the objective of the European Processor Initiative, with 30 partners from 11 European countries cooperating, to strengthen the competitiveness and leadership of European industry and science, designing European general purpose and accelerator microprocessor technologies with extreme performance and power ratio, as well as tackling important segments of broad and emerging HPC and Cloud continuum markets.
23 - 28 October, 2022, Villa Romanazzi Carducci, Bari, Italy	ACAT 2022	https://indico.cern.ch/event/1106990/	Estela Suarez (Juelich)	Presentation title: "The European Processor Initiative (EPI), a status update"	General project overview

20 October 2022, Barcelona, Spain	Arm SVE Hackathon 2022	https://www.bsc.es/education/training/other-training/arm-sve-hackathon-2022	BSC	Organisation of a hackathon	This hackathon is aimed at application developers interested in learning about the impact of the latest Arm processor features on their High Performance Computing and Machine Learning applications. Arm researchers and engineers will describe the company's HPC tools (including compilers, math libraries, debugging and profiling tools) to explore what benefits this processor can bring. During the hackathon, the MN4 CTE-ARM cluster was used and various applications developed at BSC will be optimized to be executed on this type of hardware. This activity is organized in collaboration with the Arm company, within the framework of the Arm-BSC Center of Excellence and the European EPI project.
20 October - 1 November 2022, Genoa, Italy	Festival della Scienza	http://www.festivalscienza.eu/site/en/home.html	Carlo Cavazzoni (Leonardo)	Panel discussion	During the panel discussion we talked about the new possibilities and opportunities that arise from the use of modern

					supercomputers, especially for what industry applications are concerned, and the current status and future directions of the field.
2-4 November 2022, Bordeaux, France	IEEE 34th International Symposium on Computer Architecture and High Performance Computing	https://project.inria.fr/sbac2022/	João Vieira (IST)	Presentation of the paper entitled "gem5-ndp: Near-Data Processing Architecture Simulation from Low-Level Caches to DRAM"	The use of accurate simulation environments is fundamental towards a real assessment of accelerators, particularly when deployed as near data computation schemes. The paper proposes one such schemes based on the gem5 simulation environment.
7 November 2022, Berlin, Germany	5th Workshop on RISC-V Activities	https://www.edacentrum.de/risc-v	César Fuguet (CEA)	VRP: VaRiable and extended Precision RISC-V Accelerator for HPC scientific applications	The partners haven't delivered the key message.
13 - 18 November 2022, Dallas, USA	Supercomputing 2022	https://sc22.supercomputing.org/	Mario Kovač, Igor Piljić, Nikolina Lednicki (UNIZG)	EPI booth	Presentation of European Processor Initiative, project goals and meetings with interested attendees.
13 - 18 November 2022, Dallas, USA	Supercomputing 2022	https://sc22.supercomputing.org/	Luca Benini (ETHZ and UNIBO)	Keynote "Open Platforms for Energy-Efficient Scalable Computing"	An important goal of the European processor initiative is to design more efficient computing systems to support large-scale data-parallel workloads. In this talk, Luca Benini presented

					open-source RISC-V HW and SW for energy-efficient computing, moving from tiny, parallel ultra-low power chips to high-performance many-core chiplets, and provide a personal view on future directions.
13 - 18 November 2022, Dallas, USA	Supercomputing 2022	https://sc22.supercomputing.org/	Denis Dutoit, Yves Durand (CEA)	Presentation of the VXP accelerator (video) as part of CEA booth	The partners haven't delivered the key message.
13 - 18 November 2022, Dallas, USA	Supercomputing 2022	https://sc22.supercomputing.org/	Estela Suarez (Juelich)	Workshop speaker, Birds of a Feather (BoF) session leader	General project overview
13 - 18 November 2022, Dallas, USA	Supercomputing 2022	https://sc22.supercomputing.org/	Fraunhofer	Booth	Fraunhofer ITWM presented STX Hardware and Software Toolchain related activities of the EPI project.
6-8 December 2022, Paris, France	SGA2 Modelling and Methodology Workshop Week	https://www.linkedin.com/feed/update/urn:li:activity:7005882153775333376/?utm_source=share&utm_medium=member_desktop	Nazareno Bruschi (UNIBO)	Virtual Platform for Power Management Subsystem (PMS)	Nazareno Bruschi from UNIBO team, described the WP6 activities to the EPI SGA2 partners. In this WP, the main activity of UNIBO is the power management subsystem (PMS) modeling. This latter controls the voltage and frequency of the HPC platform according to the power budget

					specified by the operating system of the HPC platform. The subsystem has been developed in the context of the PULP project and can be extended to simulate the critical PMS features. The simulator must be provided with a standard interface to be instantiated and controlled by the virtual platform, which will be the final scope of the WP6 activities.
6-8 December 2022, Paris, France	SGA2 Modelling and Methodology Workshop Week	https://www.linkedin.com/feed/update/urn:li:activity:7005882153775333376/?utm_source=share&utm_medium=member_desktop	Antonio Portero, Carlos Falquez, Nam Ho (Juelich)	Workshop speaker, Birds of a Feather (BoF) session participation	Modeling methodology discussion.
12-15 December 2022, online	RISC-V Summit 2022	https://riscv.org/event/risc-v-summit-2022/	Andrea Bocco (CEA)	The VRP: extended and VaRiable Precision RISC-V accelerator for scientific HPC floating-point applications	The partners haven't delivered the key message.

3.2 Press releases, Magazine articles, Interviews and Coverage

3.2.1 Press releases

During the indicated reporting period, the consortium, in collaboration with The European High Performance Computing Joint Undertaking (EuroHPC JU), EUPEX and the EUPILOT Project, issued a joint press release. It was announced that EuroHPC JU has launched 3 new research and innovation projects and what their goals are. Namely, to bring the EU and its partners in EuroHPC JU closer to the development of independent microprocessor and HPC technology and to drive a sovereign European HPC ecosystem. This press release was a success, attracting both media attention and social media engagement.

In addition, SiPearl, a company founded to commercialize EPI's technology, issued several press releases of its own. This year, SiPearl made great efforts to gain independent coverage and recognition among key stakeholders.

Tables 2 and 3 list the press releases issued by the project and its partners in the first year.

Table 2. Press release list

Date	Press release	Link	Key message
4 February 2022	3 new R&I projects to boost the digital sovereignty of Europe	https://www.european-processor-initiative.eu/3-new-ri-projects-to-boost-the-digital-sovereignty-of-europe/	The European High Performance Computing Joint Undertaking (EuroHPC JU) has launched 3 new research and innovation projects. The projects aim to bring the EU and its partners in the EuroHPC JU closer to developing independent microprocessor and HPC technology and advance a sovereign European HPC ecosystem. The European Processor Initiative (EPI SGA2), The European PILOT and the European Pilot for Exascale (EUPEX) are interlinked projects and an important milestone towards a more autonomous European supply chain for digital technologies and specifically HPC.

Table 3. SiPearl press release list

Date	Press release	Link	Key message
1 March 2022	SiPearl Selects Ansys' Power Signoff Solution for European	https://www.ansys.com/news-center/press-releases/3-1-22-sipearl-selects-ansys-power-	Ansys (NASDAQ: ANSS) has been selected by SiPearl to enable the development of its world-class high performance

	Supercomputer Chip	signoff-solution-for-european-supercomputer-chip	computing (HPC) microprocessor family as part of the European Processor Initiative (EPI) consortium for exascale supercomputing. SiPearl will leverage the best-in-class Ansys RedHawk-SC™ multiphysics simulation platform to validate semiconductor power integrity, minimize power consumption, and accelerate development time of its Rhea family of microprocessors.
28 April 2022	Pierre Marchal, Chief Financial Officer	https://sipearl.com/wp-content/uploads/2022/04/Press_release_SiPearl_Pierre_Marchal_CFO.pdf	Pierre Marchal (44, ESSEC Business School graduate) has been appointed Chief Financial Officer of SiPearl, the company designing the highperformance, low-power microprocessor for European exascale supercomputers.
17 May 2022	More than 100 employees	https://sipearl.com/wp-content/uploads/2022/05/PR_SiPearl_100_employees.pdf	SiPearl, the company designing the high-performance, lowpower microprocessor for European exascale supercomputers, has exceeded 100 employees. The company currently employs 104 microelectronics and software specialists across its 6 sites: Maisons-Laffitte (Headquarters), Barcelona, Duisburg, Grenoble, Massy and Sophia Antipolis.
29 May 2022	SiPearl Collaborates with NVIDIA on Enabling Accelerated Computing Solutions with European Microprocessor	https://sipearl.com/wp-content/uploads/2022/05/PR_SiPearl_collaboration_NVIDIA.pdf	SiPearl, the company designing the high-performance, low-power microprocessor for European exascale supercomputers, has entered into a strategic collaboration agreement with NVIDIA for joint technical and business developments aiming to combine both companies' portfolio of hardware and software solutions.
30 May 2022	Hewlett Packard Enterprise and SiPearl Partner to Develop HPC Solutions with European Processors and Accelerate Europe's Adoption of Exascale Supercomputers	https://sipearl.com/wp-content/uploads/2022/05/Embargoed-5.30-at-9am-CET_HPE-and-SiPearl-partnership-announcement.pdf	– Hewlett Packard Enterprise (NYSE: HPE) and SiPearl, the company designing a high-performance and low-power microprocessor for European exascale supercomputers, today announced a strategic partnership to jointly develop HPC solutions. The partnership, which expands heterogenous computing options for supercomputing and leverages European architectures, will support and accelerate adoption of exascale systems in Europe.
14 June 2022	European Innovation Council	https://sipearl.com/wp-content/uploads/2022/06/	The Commission announced today the first direct equity

	(EIC): first major equity investment by EIC Fund in strategic technology for Europe's future	220614-EIC-first-investment-press-announcement.pdf	investment by the European Innovation Council (EIC) Fund following its launch under Horizon Europe. The French start-up, SiPearl, was selected for support by the EIC Accelerator. In addition to a €2.5 million grant, the company will receive a €15 million equity investment to develop and scale up its breakthrough innovation in chip technology. This is part of a Series A financing round, through which the EIC Fund investment will catalyse more than €100 million with strategic and other public investors, which SiPearl will unveil soon.
12 July 2022	SiPearl Grenoble emménage dans le quartier Europole pour préparer la montée en puissance de ses effectifs	https://sipearl.com/wp-content/uploads/2022/07/CP_SiPearl_demenagement_Grenoble_VDEF.pdf	SiPearl, la société qui conçoit le microprocesseur haute performance et basse consommation destiné aux supercalculateurs exascale européens, déménage son établissement grenoblois au 4 place Robert Schuman, dans le quartier d'affaires Europole.
25 October 2022	Sébastien Kamphuis joins SiPearl as Chief Information Officer	https://sipearl.com/wp-content/uploads/2022/10/PR_SiPearl_CIO_nomination.pdf	Sébastien Kamphuis (39, Infosup Paris) has been appointed Chief Information Officer of SiPearl, the company designing the high-performance low-power microprocessor for European exascale supercomputers.
14 November 2022	SiPearl and AMD collaborate to address exascale1 supercomputing in Europe	https://sipearl.com/wp-content/uploads/2022/11/PR_SiPearl_AMD_collaboration_VDEF.pdf	SiPearl, the company designing the highperformance, low-power microprocessor for European supercomputers, has entered into a business collaboration agreement with AMD to provide a joint offering for exascale supercomputing systems, combining SiPearl's HPC microprocessor, Rhea, with AMD Instinct™ accelerators.

3.2.2 Magazine articles and interviews

During the first year of the project, the consortium, in collaboration with its members, published a number of interviews and articles. Table 4 lists the interviews/articles published by the projects and their partners during the first year.

Table 4. Interview list

Interview/article	Date and publisher	Link	Key message
Ransomware: who pays on the rise - European processor - Digital Service Act	April-29-2022 ***Radio24***	https://www.radio24.ilsole24ore.com/programmi/2024/puntata/ransomware-crescita-chi-paga--processore-europeo--digital-service-act-220528-AEeKjJVB?refresh_ce=1	In the context of European projects to reduce the technological dependence of the EU on the United States and Asia, the European Processor Initiative (EPI) which aims to design and build a new family of Made in EU processors is of particular importance. We talk about it with Luca Benini, professor of Electronics at the University of Bologna and member of the EPI steering committee.
EPI SGA2 - Building Europe's high performance computing capabilities	April-29-2022 ***CORDIS - European Commission***	https://eurohpc-ju.europa.eu/system/files/2022-05/ED-7309_CORDIS%20LotB_PIP%20European%20Supercomputing_Brochure_EN_LR%20acc.pdf	Interview with Etienne Walter (Atos): With the development of new processors and accelerators, this EU-funded project aims to equip the EU with its own world-class supercomputing technology. Because HPC has the capability to process extreme-scale simulations that are simply impossible to do with a single system, it has the power to transform research and business.
Innovation at scale	May-25-2022 ***Scientific Computing World***	https://www.scientific-computing.com/feature/innovation-scale	Interview with Etienne Walter (Atos): The European Processor Initiative (EPI) is an ongoing project funded by the European Commission, whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme-scale computing that includes high-performance big-data and a range of emerging applications. The EPI technology stack includes a General Purpose Processor (GPP) research stream and an accelerator stream which supports the development of multiple accelerator technologies. This is being co-developed to deliver a European-based HPC

			platform for exascale computing.
The IoT Radar Interview with Eric Monchalin	June-23-2022 ***The IoT Radar***	https://www.youtube.com/watch?v=mh2Mm1lNAxA&t=2s	The IoT Radar interview with Eric Monchalin (Atos), Chairman of European Processor Initiative: How the European Processor Initiative will change the Semiconductor Industry in Europe.
Q&A with EPI Chair Eric Monchalin, an HPCwire Person to Watch in 2022	September-9-2022 ***HPC Wire***	https://www.hpcwire.com/2022/09/09/qa-with-atos-eric-monchalin-an-hpcwire-person-to-watch-in-2022/	HPCwire presents our interview with Eric Monchalin (Atos), chair of European Processor Initiative & VP, head of machine intelligence, Atos, and an HPCwire 2022 Person to Watch. Monchalin recaps the EPI program strategy, explains the motivations for tech sovereignty, and gives a view to current and future computing trends.
La strategia europea e la difficile autonomia	November-7-2022 ***Corriere della Sera***	https://www.european-processor-initiative.eu/dissemination-material/la-strategia-europea-e-la-difficile-autonomia/	Interview with Carlo Cavazzoni (Leonardo) : Intanto nel 2019 è stata lanciata la European Processor Initiative, portata avanti da un consorzio che riunisce 30 società e università europee, finanziata dal programma di ricerca Ue Horizon 2020 e da un gruppo di Stati : Italia, Francia, Germania, Grecia, Olanda, Portogallo, Spagna, Svezia, Croazia e Svizzera. Per il nostro Paese fanno parte del consorzio le università di Bologna e Pisa, Cineca, E4 Computer Engineering, STMicroelectronics e Leonardo.

3.2.3 Press coverage

During the year, EPI continued to receive considerable coverage in the international press. Table 5 lists the press coverage, which can also be found in the project's Dissemination and Press Repository.

Table 5. Press coverage list

11 January, 2022	**Movi Electrica**	**Europe ups the ante: chips for autonomous driving** https://movielectrica.es/europa-sube-la-apuesta-chips-para-la-conduccion-autonoma/

		The automotive industry is much more than engines, wheels and bodies. The number of elements and processes involved in the production of a car are innumerable, and they end up assembling parts that come from different parts of the world. In the case of chips, they are designed in the United States and made in China. Stay with us to find out what Europe is doing to start producing its own chips for autonomous driving.
17 January, 2022	**Ceotech.it**	**E4 helps EPI in chip and HPC independence** https://www.ceotech.it/e4-aiuta-lepi-nellindipendenza-di-chip-e-di-hpc/ E4 Computer Engineering SpA has successfully participated in the first phase of the European Processor Initiative (EPI), a project aimed at enabling the independence of the European Union (EU) in chip technologies and infrastructures and infrastructure for High Performance Computing.
17 January, 2022	**Industry Weekly**	**E4 CONTRIBUTES TO THE SUCCESS OF THE EUROPEAN PROCESSOR INITIATIVE** https://industryweekly.it/e4-contribuisce-al-successo-della-european-processor-initiative/ E4 Computer Engineering SpA has successfully participated in the first phase of the European Processor Initiative (EPI), to enable the independence of the European Union (EU) in technologies.
21 January, 2022	**The Register**	**EC president promises European Chips Act to quadruple homegrown production by 2030** https://www.theregister.com/2022/01/21/european_chips_act/ The European Commission will introduce legislation next month designed to turn the continent into a center of chip expertise and manufacturing. The EC will propose the European Chips Act in early February, which will boost Europe's infrastructure for the production and supply chain of chip manufacturing, said Ursula von der Leyen, president of the commission, in an address to the World Economic Forum on Thursday.
21 January, 2022	**01factory**	**E4 contributes to the success of the European Processor Initiative** https://www.01factory.it/e4-contribuisce-al-successo-della-european-processor-initiative/ E4 Computer Engineering SpA has successfully participated in the first phase of the European Processor Initiative (EPI), a project aimed at enabling the independence of the European Union (EU) in chip technologies and infrastructures and infrastructure for High Performance Computing.

3 February, 2022	**EuroHPC JU**	**3 new R&I projects to boost the digital sovereignty of Europe** https://eurohpc-ju.europa.eu/press-release/3-new-ri-projects-boost-digital-sovereignty-europe The European High Performance Computing Joint Undertaking (EuroHPC JU) has launched 3 new research and innovation projects. The projects aim to bring the EU and its partners in the EuroHPC JU closer to developing independent microprocessor and HPC technology and advance a sovereign European HPC ecosystem. The European Processor Initiative (EPI SGA2), The European PILOT and the European Pilot for Exascale (EUPEX) are interlinked projects and an important milestone towards a more autonomous European supply chain for digital technologies and specifically HPC.
3 February, 2022	**HPC Wire**	**EuroHPC Launches 3 New Research and Innovation Projects** https://www.hpcwire.com/off-the-wire/eurohpc-launches-3-new-research-and-innovation-projects/ The European High Performance Computing Joint Undertaking (EuroHPC JU) has launched 3 new research and innovation projects. The projects aim to bring the EU and its partners in the EuroHPC JU closer to developing independent microprocessor and HPC technology and advance a sovereign European HPC ecosystem. The European Processor Initiative (EPI SGA2), The European PILOT and the European Pilot for Exascale (EUPEX) are interlinked projects and an important milestone towards a more autonomous European supply chain for digital technologies and specifically HPC.
3 February, 2022	**Econostrum**	**The specialist in reprogrammable semiconductors Menta obtains €7.5 million from the EIB** https://en.econostrum.info/The-specialist-in-reprogrammable-semiconductors-Menta-obtains-7-5-million-from-the-EIB_a1260.html The company works in particular for Thales Alenia Space, the French Defence Procurement Agency (DGA) and the European Defence Agency's EDA-SoC programme (EDA-EDA). It also belongs to the European Processor Initiative (EPI) consortium, which was created in December 2018 and brings together twenty-eight partners from ten European Union countries.
4 February, 2022	**The Next Platform**	**ARM CPUS TO TAKE A BITE OUT OF THE HPC MARKET** https://www.nextplatform.com/2022/02/04/arm-cpus-to-take-a-bite-out-of-the-hpc-market/

		Silicon Pearl, the company involved with the European Processor Initiative (EPI) project is using the Neoverse V1 design, Gorda disclosed. Meanwhile, the N1 design has been used in the "Quicksilver" and Mystique" Altra server chips from Ampere Computing, the startup founded by former Intel executive Renée James. Amazon's Graviton2 chip that powers some AWS EC2 instances uses the N1 core, and the Graviton3 uses the V1 core. Neoverse V series cores also apparently feature in Nvidia's planned "Grace" chip aimed at supercomputing, and in a server chip being developed by South Korea's Electronics and Telecommunications Institute (ETRI).
8 February, 2022	**The Register**	**Joined up thinking: Europe to oversee trio of projects for homegrown chips, HPC gear** https://www.theregister.com/2022/02/08/eu_chip_projects/ Efforts in Europe to devise sovereign chips has picked up the past two months, with the European Union now coordinating three separate campaigns to make homegrown processors and supercomputer-grade systems. An EU initiative called the European High Performance Computing Joint Undertaking this month said it has selected three projects to further boost the continent's high-performance computing ecosystem and design of microprocessors.
10 February, 2022	**HPC Wire**	**European Chips Act Aims to Establish EU Semiconductor Sovereignty** https://www.hpcwire.com/2022/02/10/european-chips-act-aims-to-establish-eu-semiconductor-sovereignty/ One of the farthest-reaching and longest-lasting impacts of the Covid-19 pandemic has been its impact on the global supply chain—a massive disruption that has increased scarcity, raised prices and introduced delays for a wide variety of products. The impacts have been particularly acute for products that require semiconductors, including everything from gaming consoles and phones to vehicles and healthcare devices. Now, the European Commission is proposing a "comprehensive set of measures to ensure the EU's security of supply, resilience and technological leadership in semiconductor technologies and applications": the European Chips Act, which, if passed, is anticipated to bring €43 billion ($49.2 billion USD) of public and private funding to bear on the European semiconductor industry through 2030.
16 February, 2022	**HPC Wire**	**Atos Tees Up New BullSequana Supercomputer for European Exascale**

		https://www.hpcwire.com/2022/02/16/atos-tees-up-new-bullsequana-supercomputer-for-european-exascale/ At a three-hour livestreamed launch event held today (Feb. 16) in Paris, French technology firm Atos unveiled its new supercomputer, the BullSequana XH3000, intended to provide from one petaflops to exaflops of traditional double-precision digital simulation and up to 10 exaflops of mixed-precision AI performance. Availability is planned for the fourth quarter of this year.
17 February, 2022	**HPC Wire**	**Atos Invokes Sovereignty, Sustainability at Next-Gen Supercomputer Launch** https://www.hpcwire.com/2022/02/17/atos-invokes-sovereignty-sustainability-at-next-gen-supercomputer-launch/ At an elaborate event yesterday, French computing firm Atos announced its newest supercomputer: the BullSequana XH3000, a system that the company can scale to an exaflops performance and which works with hardware from AMD, Intel, Nvidia and (when it arrives) SiPearl. (More feature coverage on the technical aspects of the XH3000 is available here.) At the event – which included a series of keynotes and two roundtables – Atos and its associates hammered home two key ideas that were repeated across nearly every speaker.
1 March, 2022	**Inside HPC**	**SiPearl Selects Ansys' Power Signoff Solution for European Supercomputer Chip** https://insidehpc.com/2022/03/sipearl-selects-ansys-power-signoff-solution-for-european-supercomputer-chip/ SiPearl today said the Ansys multiphysics platform has been selected by SiPearl, Europe's exascale supercomputer chip project for development of its high performance computing (HPC) microprocessor family as part of the European Processor Initiative (EPI). SiPearl will use the Ansys RedHawk-SC simulation platform with the intent to validate semiconductor power integrity, minimize power consumption and accelerate development time of its Rhea family of microprocessors.
1 March, 2022	**HPC Wire**	**SiPearl Selects Ansys' Power Signoff Solution for European Supercomputer Chip** https://www.hpcwire.com/off-the-wire/sipearl-selects-ansys-power-signoff-solution-for-european-supercomputer-chip/

		Ansys has been selected by SiPearl to enable the development of its world-class high performance computing (HPC) microprocessor family as part of the European Processor Initiative (EPI) consortium for exascale supercomputing. SiPearl will leverage the best-in-class Ansys RedHawk-SC multiphysics simulation platform to validate semiconductor power integrity, minimize power consumption, and accelerate development time of its Rhea family of microprocessors.
2 March, 2022	**Electronics Clap**	**SiPearl Picks Ansys's Power Signoff Solution for European Supercomputer Chip** https://electronicsclap.com/business/sipearl-picks-ansyss-power-signoff-solution-for-european-supercomputer-chip/ SiPearl selects Ansys (NASDAQ: ANSS) to enable the development of its world-class high performance computing (HPC) microprocessor family as part of the European Processor Initiative (EPI) consortium for exascale supercomputing. SiPearl will leverage the best-in-class Ansys RedHawk-SC multiphysics simulation platform to validate semiconductor power integrity, minimize power consumption, and accelerate development time of its Rhea family of microprocessors.
2 March, 2022	**Nasdaq**	**ANSYS' (ANSS) RedHawk-SC Solutions Being Leveraged By SiPearl** https://www.nasdaq.com/articles/ansys-anss-redhawk-sc-solutions-being-leveraged-by-sipearl SiPearl will utilize the Ansys RedHawk-SC simulation platform to develop its high-performance computing (HPC) microprocessor family within the European Processor Initiative (EPI) project for exascale supercomputing. The company plans to take advantage of ANSYS' simulation platform to substantiate semiconductor power reliability, optimize energy consumption and rev up the development time of its high-performance, low-power family of microprocessors called Rhea.
4 March, 2022	**Semi Engineering**	**Week In Review: Design, Low Power** https://semiengineering.com/week-in-review-design-low-power-186/ SiPearl selected Ansys' RedHawk-SC multiphysics simulation platform to validate semiconductor power integrity, minimize power consumption, and accelerate development time of its Rhea family of high-performance compute microprocessors. The HPC microprocessors will be used in the European Processor Initiative exascale supercomputing project.
10 March, 2022	**Benzinga**	**Server Microprocessor Market Outlook and Growth Stance Forecast 2022-2031** https://www.benzinga.com/pressreleases/22/03/26077899/server-microprocessor-market-outlook-and-growth-stance-forecast-2022-2031 The European Commission, in December 2018, declared the selection of the Consortium European Processor Initiative (EPI). The aim of the initiative is to "develop, co-design, and introduce a low-

		power microprocessor to the European market", thus being able to retain a significant part of that technology is Europe. - The EPI consortium proposes to create a long-term economic model by delivering a family of processors for the following markets: High-Performance Computing, Data centres and servers, and Autonomous vehicles.
15 March, 2022	**The Register**	**Intel to spend €17bn on chip mega-factory in Germany** https://www.theregister.com/2022/03/15/intel_germany_europe_investment/ SiPearl developed the Rhea processor with funding from the European Processor Initiative. The biz will pair the chip with Intel's Ponte Vechhio GPU-based accelerator for supercomputing applications. "SiPearl is building the European microprocessor for high-performance computing and sees great value in European-based leading-edge foundry services of Intel's caliber," Notton told The Register.
25 March, 2022	**Nasdaq**	ANSYS (ANSS) to Offer Latest EPYC Processors to Cloud Customers https://www.nasdaq.com/articles/ansys-anss-to-offer-latest-epyc-processors-to-cloud-customers A few days back, ANSYS' multiphysics simulation platform was selected by SiPearl, the company designing the high-performance and low-power microprocessor for European supercomputers. SiPearl will utilize the ANSYS RedHawk-SC simulation platform to develop its HPC microprocessor family within the European Processor Initiative project for exascale supercomputing. The company plans to take advantage of ANSYS' simulation platform to substantiate semiconductor power reliability, optimize energy consumption and rev up the development time of its high-performance, low-power family of microprocessors called Rhea.
29 March, 2022	**HPC Wire**	**People to Watch 2022** https://www.hpcwire.com/people-to-watch-2022/11/ Eric Monchalin, Chair of European Processor Initiative & VP, Head of Machine Intelligence, Atos Congratulations on being named a 2022 HPCwire Person to Watch!
5 April, 2022	**HPC Wire**	**Indigenous HPC: What It Means and Why Now** https://www.hpcwire.com/2022/04/05/indigenous-hpc-what-it-means-and-why-now/ Especially impressive are Europe's achievements in organizing more than two dozen nations to pursue this goal through the EuroHPC Joint Undertaking, which among other things has already

		deployed eight or so pre-exascale supercomputers. Initiatives such as ETP4HPC and the European Processor Initiative have advanced indigenous technologies. Europe is poised to become the global leader in democratizing exascale technologies through its Centers of Excellence and SMB initiatives aimed at scientific and industrial researchers in participating countries.
25 April, 2022	**The Next Platform**	**Oil And Gas Industry To Get Its Own Stencil Tensor Accelerator** https://www.nextplatform.com/2022/04/25/oil-and-gas-industry-to-get-its-own-stencil-tensor-accelerator/ The result is the STX compute engine – that STX is short for stencil and tensor accelerator, which is part of the growing trend toward domain-specific processing – that tries to balance the conflicting demands for high power efficiency, easy programmability, and low costs. The STX chip was designed as part of the larger European Processor Initiative (EPI) that is driving the push for European independence in HPC and, eventually, exascale computing by relying more on EU-developed technologies.
4 May, 2022	**Design&Reuse**	**European Processor Initiative will have ZeroPoint IP in their chip** https://www.design-reuse.com/news/51873/european-processor-initiative-zeropoint-ip.html ZeroPoint Technologies AB today announced that they are a member of the European Processor Initiative (EPI) consortium. ZeroPoint will contribute with their Ziptilion™ IP on the EPAC 2.0 chip. ZeroPoint Technologies provides the world's only available Memory Booster IP block for System on Chips (SoCs), effectively doubling a computer's main memory capacity and memory bandwidth; providing significantly more performance per watt.
18 May, 2022	**HPC Wire**	**HPE Announces New HPC Factory in Czech Republic** https://www.hpcwire.com/2022/05/18/hpe-announces-new-hpc-factory-in-czech-republic/ The new factory marks another major investment in sovereign European supercomputing as the European Union strives to build an independent foundation in the HPC world. Even before 2020, the EU had been working toward this goal through major initiatives like the EuroHPC Joint Undertaking and the European Processor Initiative (EPI), and the dual stressors of pandemic-induced supply chain shortages and the war in Ukraine have only exacerbated that desire for independence.
30 May, 2022	**The Register**	**Home-grown Euro chipmaker SiPearl signs deal with HPE, Nvidia** https://www.theregister.com/2022/05/30/sipearl_hpe_nvidia/ SiPearl itself was born out of the European Processor Initiative (EPI), aimed at developing a new generation of high-end European microprocessors.

		The Rhea processor is set to be the first fruit of this and is due to launch sometime before the end of this year. It is expected to comprise 72 of the Neoverse V1 (codenamed Zeus) 64-bit Arm cores, plus support for DDR5 or the high-performance HBM2E stacked memory technology.
30 May, 2022	**Design&Reuse**	**Hewlett Packard Enterprise and SiPearl Partner to Develop HPC Solutions with European Processors and Accelerate Europe's Adoption of Exascale Supercomputers** https://www.design-reuse.com/news/52027/hewlett-packard-enterprise-sipearl-partnership-exascale-supercomputers.html SiPearl is designing the high-performance, low-power microprocessor for European exascale supercomputers. This new generation of microprocessors will enable Europe to set out its technological sovereignty in strategic high performance computing (HPC) markets such as artificial intelligence, medical research or climate modelling. The company is working in close collaboration with its 27 partners from the European Processor Initiative (EPI) consortium - leading names from the scientific community, supercomputing centres and industry - which are its stakeholders, future clients and end-users. SiPearl is supported by the European Union.
30 May, 2022	**HPC Wire**	**HPE and SiPearl Partner to Develop HPC Solutions with European Processors and Accelerate Europe's Adoption of Exascale Supercomputers** https://www.hpcwire.com/off-the-wire/hpe-and-sipearl-partner-to-develop-hpc-solutions-with-european-processors-and-accelerate-europes-adoption-of-exascale-supercomputers/ SiPearl is designing the high-performance, low-power microprocessor for European exascale supercomputers. This new generation of microprocessors will enable Europe to set out its technological sovereignty in strategic high performance computing (HPC) markets such as artificial intelligence, medical research or climate modelling. The company is working in close collaboration with its 27 partners from the European Processor Initiative (EPI) consortium – leading names from the scientific community, supercomputing centres and industry – which are its stakeholders, future clients and end-users. SiPearl is supported by the European Union.
30 May, 2022	**Bakersfield.com**	**Hewlett Packard Enterprise and SiPearl Partner to Develop HPC Solutions with European Processors and Accelerate Europe's Adoption of Exascale Supercomputers** https://www.bakersfield.com/ap/news/hewlett-packard-enterprise-and-sipearl-partner-to-develop-hpc-solutions-with-european-processors-and-accelerate/article_0e9087ff-100f-5ee4-b0fd-598a00be40ba.html

		SiPearl is designing the high-performance, low-power microprocessor for European exascale supercomputers. This new generation of microprocessors will enable Europe to set out its technological sovereignty in strategic high performance computing (HPC) markets such as artificial intelligence, medical research or climate modelling. The company is working in close collaboration with its 27 partners from the European Processor Initiative (EPI) consortium - leading names from the scientific community, supercomputing centres and industry - which are its stakeholders, future clients and end-users. SiPearl is supported by the European Union.
30 May, 2022	**HPC Wire**	**SiPearl Emerging as Heavyweight for 'Made in Europe' Chips** https://www.hpcwire.com/2022/05/30/sipearl-emerging-as-heavyweight-for-made-in-europe-chips/ There's good reason for some of the top chipmakers to go with SiPearl. The Rhea CPU emerged from an EU-funded initiative called the European Processor Initiative (EPI), which is focused on creating "made-in-Europe" chips. The European DNA of the Rhea CPU, which is based on ARM's Neoverse V1 CPU design, is attracting the attention of European companies and universities in high-performance computing, including Atos, which is a participant in EPI and building exascale systems.
6 June, 2022	**eeNews Europe**	**$400m RISC-V design centre for Barcelona** https://www.eenewseurope.com/en/400m-risc-v-design-centre-for-barcelona/ The Barcelona centre is already a key partner in the development of RISC-V chips for European supercomputers, including a 22nm RISC-V chip accelerator for the European Processor Initiative.
13 June, 2022	**HPC Wire**	**As LUMI Launches, a Look at the State of EuroHPC** https://www.hpcwire.com/2022/06/13/as-lumi-launches-a-look-at-the-state-of-eurohpc/ "We have a very ambitious agenda of wanting a significant European technology footprint within the second exascale system that we're going to fund," Jensen continued; in his talk the following day, he specified a processor built by the European Processor Initiative (EPI). Like EuroHPC, EPI entered its second phase this year; that second phase aims to finalize EPI's first-gen low-power processors and develop second-generation processors. "In parallel to that, you have the whole [European Chips Act] that's come to life via the Commission, and all the interesting things that that's going to bring," Jensen continued, "and on the EuroHPC side we have already a placeholder for research and innovation calls in and around RISC-V and other processor technologies."

16 June, 2022	**The Next Platform**	**ATOS WINS MARENOSTRUM 5 DEAL AT BARCELONA SUPERCOMPUTING CENTER** https://www.nextplatform.com/2022/06/16/atos-wins-marenostrum-5-deal-at-barcelona-supercomputing-center/ It is absolutely unclear which compute engines BSC will choose, but we presume it will still have a production partition that comprises most of the machine and an experimental partition that blazes the trail for new compute engine testing. With the European Processor Initiative not yet ready (as far as we know) with its RISC-V parallel accelerator, and SiPearl partnering with Intel to hook its Ponte Vecchio GPU was done for some HPC center in Europe, and one that is deploying SiPearl Arm CPUs in its host. We do not think this will be the flagship Jupiter machine at Jülich, but Intel and Atos could work such a deal with BSC, if the numbers were right and there was enough juice to pay the electric bill. It is not outside of the realm of possibility that BSC might be using the future "Rialto Bridge" kickers to Ponte Vecchio, which presumably have a lot more performance and performance per watt than the first generation of the Xe HPC devices from Intel.
27 July, 2022	**The Next Platform**	**STRONG-ARMED INTO HPC, LIKE IT OR NOT** https://www.nextplatform.com/2022/07/27/strong-armed-into-hpc-like-it-or-not/ "The first one is the European Processor Initiative, which has selected the Arm ISA for the "Rhea" general purpose processor. E4 is a member of the European Processor Initiative, and we will integrate the Rhea CPU into systems.
17 August, 2022	**Scientific Computing World**	**Tech Focus: Software tools** https://www.scientific-computing.com/tech-focus/tech-focus-software-tools-2 The current iteration of the EU-funded DEEP projects, 'DEEP-SEA', started on 1 April 2021 and will help to underpin the European Processor Initiative (EPI), which is developing hardware for exascale systems.
9 November, 2022	**Impresa City**	**E4 Computer Engineering: l'HPC è pronto per le imprese** https://www.impresacity.it/news/27878/e4-computer-engineering-lhpc-e-pronto-per-le-imprese.html In queste evoluzioni E4 è parte in causa anche perché è una delle aziende selezionate per la European Processor Initiative (EPI), il programma UE per lo sviluppo di un processore tutto europeo da HPC. Il lavoro per arrivare a Rhea - questo il nome della prima generazione del processore - è lungo, E4 sta dando un importante contributo occupandosi dello sviluppo delle prime

		"lame" che ospitano i Test Chip. Un lavoro che avrà importanti ricadute anche fuori dal progetto in sé, portando allo sviluppo molte nuove soluzioni.
14 November, 2022	**ViPress**	**COLLABORATION ENTRE SIPEARL ET AMD DANS LE SUPERCALCUL EXASCALE EN EUROPE** https://vipress.net/collaboration-entre-sipearl-et-amd-dans-le-supercalcul-exascale-en-europe/ SiPearl travaille en étroite collaboration avec ses 27 partenaires du consortium European Processor Initiative (EPI) – grands noms de la communauté scientifique, centres de supercalcul et industries – qui sont ses parties prenantes, futurs clients et utilisateurs finaux. La start-up emploie plus de 100 personnes en France (Maisons-Laffitte, Grenoble, Massy, Sophia Antipolis), en Allemagne (Duisbourg) et en Espagne (Barcelone).
15 November, 2022	**Next Inpact**	**CPU et supercalculateurs européens : SiPearl multiplie les partenariats avec AMD, Graphcore, Intel, NVIDIA…** https://www.nextinpact.com/article/70372/cpu-et-supercalculateurs-europeens-sipearl-multiplie-partenariats-avec-amd-graphcore-intel-nvidia Le but de SiPearl est de « donner vie au projet du consortium European Processor Initiative (EPI) », qui regroupe pour rappel pas moins de 28 partenaires avec l'ambition de proposer un processeur capable d'alimenter un supercalculateur exaflopique. Cette frontière symbolique, dépassée pour le moment par un seul supercalculateur : Frontier avec 1,102 Exaflops.
15 November, 2022	**Hardware Upgrade**	**SiPearl, la CPU per i supercomputer europei funzionerà con gli acceleratori AMD Instinct** https://www.hwupgrade.it/news/skvideo/sipearl-la-cpu-per-i-supercomputer-europei-funzionera-con-gli-acceleratori-amd-instinct_111783.html SiPearl lavora con 27 partner del consorzio European Processor Initiative (EPI) - tra cui troviamo le italiane E4 Engineering, Università Alma Mater di Bologna, Università di Pisa, Cineca, Leonardo e STMicroelectronics - con l'obiettivo di dare all'Europa sovranità tecnologica in mercati strategici come l'HPC, l'IA, la ricerca medica o la modellazione climatica.
15 November, 2022	**The Register**	**SiPearl works with AMD on GPU support for Arm HPC chip** https://www.theregister.com/2022/11/15/sipearl_amd_arm_hpc_chip/ SiPearl is the company involved with the European Processor Initiative (EPI) to develop an Arm-based processor for an exascale supercomputer designed and built in Europe, slated for 2023.

16 November, 2022	**HPC Wire**	**Europe's Chip Sovereignty Altering US Chip Companies' Exascale Approach** https://www.hpcwire.com/2022/11/16/europes-chip-sovereignty-altering-us-chip-companies-exascale-approach/ Beyond hardware, the road for the EU to exascale includes tools, compilers, runtimes and system integration tools for chips and accelerators. The EU is funding multiple efforts that include the EPI (European Processor Initiative), EUPEX (European Pilot for Exascale) and EuroHPC. Participants in these efforts include academics, researchers and European commercial organizations such as Atos, which plans to build exascale systems under its BullSequana line.
17 November, 2022	**Network World**	**AMD partners with Arm developer for exascale computing** https://www.networkworld.com/article/3680388/amd-partners-with-arm-developer-for-exascale-computing.html SiPearl is also involved with the European Processor Initiative (EPI), a consortium selected by the European Union to support the development of a European microprocessor specifically for high performance computing (HPC), as well as emerging applications such as artificial intelligence. The EPI's goal is to develop an Arm-based processor for an exascale supercomputer by 2023.
18 November, 2022	**HPC Wire**	**RISC-V Is Far from Being an Alternative to x86 and Arm in HPC** https://www.hpcwire.com/2022/11/18/risc-v-is-far-from-being-an-alternative-to-x86-and-arm-in-hpc/ SiPearl was born out of funding from the European Union, which has a long-term goal to develop home-grown processors. The European Processor Initiative, which is also funded by the EU, is focusing on developing chips with RISC-V to break away from the proprietary x86 and Arm technologies.
18 November, 2022	**Computer World**	**AMD i francuski start-up będą budować eksaskalowy supercomputer** https://www.computerworld.pl/news/AMD-i-francuski-start-up-beda-budowac-eksaskalowy-superkomputer,442438.html Firma nawiązała następnie szereg sojuszy z kilkoma znanymi firmami z sektora IT (w tym z Intelem, Nvidią i HPE), współpracując również ściśle z EPI (European Processor Initiative; konsorcjum wybrane przez Unię Europejską, które zajmuje się rozwojem europejskiego mikroprocesora klasy HPC). Jednym z celów EPI jest opracowanie do 2023 roku procesora opartego na architekturze ARM, który będzie instalowany w eksaskalowych superkomputerach.

24 November, 2022	**LeMagIT**	**Le processeur HPC européen n'en finit pas de signer les partenariats** https://www.lemagit.fr/actualites/252527693/Le-processeur-HPC-europeen-nen-finit-pas-de-signer-les-partenariats Alors que le métacloud européen est sur le pas de tir, c'est un autre projet sponsorisé par l'UE qui avance : celui d'un processeur dédié au HPC (High performance computing) made in Europe. Et même made in France, puisque son design est réalisé par la société SiPearl, à l'origine du projet EPI (European Processor Initiative).
30 November, 2022	**Telecomlead**	**SIA warns U.S. chip design market share to plunge** https://www.telecomlead.com/telecom-chips/sia-warns-u-s-chip-design-market-share-to-plunge-107793 EU-funded European Processor Initiative to design and build a family of high-performance, low-power processors The EU's European Chips Act seeks to reinforce Europe's capacity to innovate in the design, manufacture, and packaging of advanced chips.
16 December, 2022	**HPC Wire**	**Europe to Dish out €270 Million to Build RISC-V Hardware and Software** https://www.hpcwire.com/2022/12/16/europe-to-dish-out-e270-million-to-build-risc-v-hardware-and-software/ The European Processor Initiative has developed RISC-V vector and machine-learning accelerators that will be on exascale computers in the coming years. BSC and Intel are jointly designing a supercomputing chip with a RISC-V CPU, but it is more of a lab project.
17 December, 2022	**Game-News24**	**EUROPE WILL ALLOCATE 270 MILLIONS FOR THE DEVELOPMENT OF THE RISC-V ECOSYSTEM** https://game-news24.com/2022/12/17/europe-will-allocate-270-millions-for-the-development-of-the-risc-v-ecosystem/ A European research institute has developed experimental models built on RISC-V. For example, people can see the SUPER-V platforms at the Barcelona Supercomputing Center and ExCALIBUR at the University of Edinburgh. And, the European Processor Initiative developed a multi-meter-to-reach accelerator, which are expected to become a computer application within the coming years. A RISC-V supercomputer chip was developed jointly by BSC and Intel.

3.3 Scientific Publications

In the first year of the SGA2, the consortium's partners have published several journal articles and conference proceedings, which are listed below.

- Gianluca Dini, Marco Rasori, Michele La Manna, Pericle Perazzo, "A Survey on Attribute-Based Encryption Schemes Suitable for the Internet of Things", IEEE Internet of Things Journal, 2022, https://doi.org/10.1109/JIOT.2022.3154039

- Luís Crespo, Pedro Tomás, Nuno Roma, and Nuno Neves, "Unified Posit/IEEE-754 Vector MAC Unit for Transprecision Computing", IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, https://doi.org/10.1109/TCSII.2022.3160191

- Rogério Paludo and Leonel Sousa, "NTT Architecture for a Linux-Ready RISC-V Fully-Homomorphic Encryption Accelerator", IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, https://doi.org/10.1109/TCSI.2022.3166550

- Gabriel Falcao, João Domingos, Nuno Neves, Nuno Roma, Pedro Tomás, "Compiling for Vector Extensions with Stream-based Specialization", IEEE Micro, 2022, https://doi.org/10.1109/MM.2022.3173405

- Federico Ficarelli, Andrea Bartolini, Emanuele Parisi, Francesco Beneventi, Francesco Barchi, Daniele Gregori, Fabrizio Magugliani, Marco Cicala, Cosimo Gianfreda, Daniele Cesarini, Andrea Acquaviva and Luca Benini, "Meet Monte Cimone: Exploring RISC-V High Performance Compute Clusters", CF '22: Proceedings of the 19th ACM International Conference on Computing Frontiers, 2022, Italy, https://dl.acm.org/doi/10.1145/3528416.3530869

- Carlos Álvarez, Daniel Jiménez-González, Fabian Kempf, Fabian Kreß, Imen Baili, Jesus Labarta, Juan Miguel De Haro, Jürgen Becker, Miquel Moretó, Tim Hotfilter, "Towards Reconfigurable Accelerators in HPC: Designing a Multipurpose eFPGA Tile for Heterogeneous SoCs", DATE 2022, 2022, Belgium, https://doi.org/10.23919/DATE54114.2022.9774716

- Fatma Jebali, Oumaima Matoussi, Arief Wicaksana, Amir Charif, Lilia Zaourar, "Decoupling processor and memory hierarchy simulators for efficient design space exploration", RAPIDO 2022 workshop (HiPEAC Conference), 2022, Hungary, https://doi.org/10.1145/3522784.3522796

- Marco Cococcioni, Federico Rossi, Emanuele Ruffaldi and Sergio Saponara, "Small reals representations for Deep Learning at the edge: a comparison", Conference on Next Generation Arithmetic (CoNGA 2022), 2022, https://doi.org/10.1007/978-3-031-09779-9_8

3.4 Website and Social Media

3.4.1 EPI Website

The public project website is located at https://www.european-processor-initiative.eu/.

In previous years, EPI website has been established as a key channel for communication of activities and dissemination of results. The website contains information about the project, consortium members, dissemination and communication repository, information about Streams, press/media kit repository and news and events section. It is important to point out that the website will remain to be a key channel of communication in the upcoming years.

Figure 5. EPI Website

The website has been changed so there is a clear difference between Phase 1 and Phase 2 of the project. Content on the website has been refreshed – both texts and photographs. There were changes also regarding the Streams, information about work in the next three years has been updated.

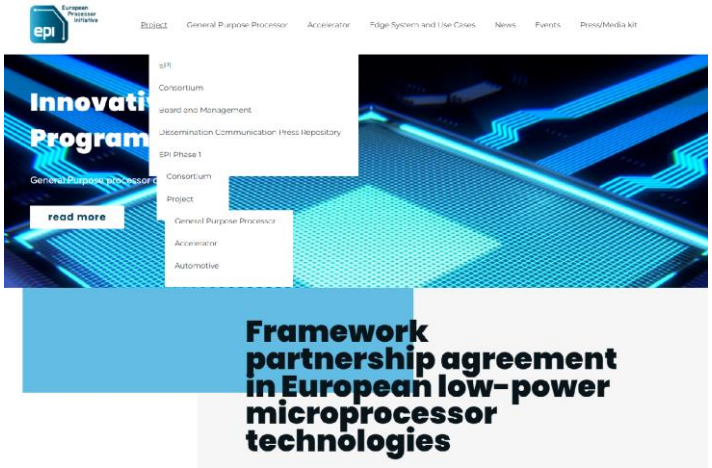

Figure 6. EPI Phase1 content archive

A part of the content from SGA1 was archived under the new sub-item – EPI Phase 1. Under the said sub-item, there is general information from the previous period about EPI, Consortium (partners from the Automotive Stream) and about Project. Under the Project, content about General Purpose Processor, Accelerator and Automotive from SGA1 was archived.

Figure 7. Addition to D&C Repository - Phases

Furthermore, Dissemination and Communication Press Repository search bar was updated with tags Phase 1 and Phase 2. Thus, journalists and interested stakeholders will be able to search the repository's content in an easier way.

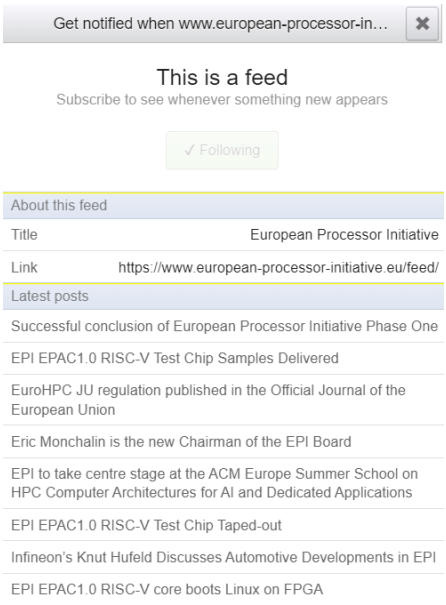

Figure 8. RSS feed

It should be pointed out that there is an RSS feed that allows all interested stakeholders to subscribe to EPI's website for the latest news and updates.

The RSS feed is located at https://www.european-processor-initiative.eu/feed/.

3.4.2 Twitter

The EPI project Twitter account (https://mobile.twitter.com/EuProcessor) is a very important social media channel for distributing information related to the project's activities. EPI's Twitter account is a useful tool for communication with important stakeholders, institutions, companies, and other relevant projects. It is also important to note that the Twitter account has been a very useful communication channel for showcasing participation in events which are very important for the project. In the past years, EPI has managed to create a community and a network of followers interested in common topics.

Figure 9. EPI Twitter

As it was done in the previous period, links, tags, and retweets will be made to other relevant content as appropriate. This strategy will boost the visibility and engagement of the posts.

3.4.3 LinkedIn

EPI's page is available at: https://www.linkedin.com/company/european-processor-initiative/.

LinkedIn is also a useful communication channel for sharing information with a community of interested professionals. Relevant content that is shared includes EPI participation in events, consortium press releases and news articles related to partner and project activities.

Figure 10. LinkedIn profile

The same strategy as on Twitter will be applied regarding links and tags to other relevant content. It is evident from the previous period that this strategy helps with the visibility and engagement of the project's page.

3.4.4 YouTube

EPI's channel is available at:
https://www.youtube.com/channel/UCGvQcTosJdWhd013SHnIbpA/featured.

Previous Dissemination and Communication Plans highlighted the YouTube platform as an audio-visual repository for EPI videos and other AV materials. Videos from events, conferences, presentations and tutorials were posted on the channel and achieved thousands of views.

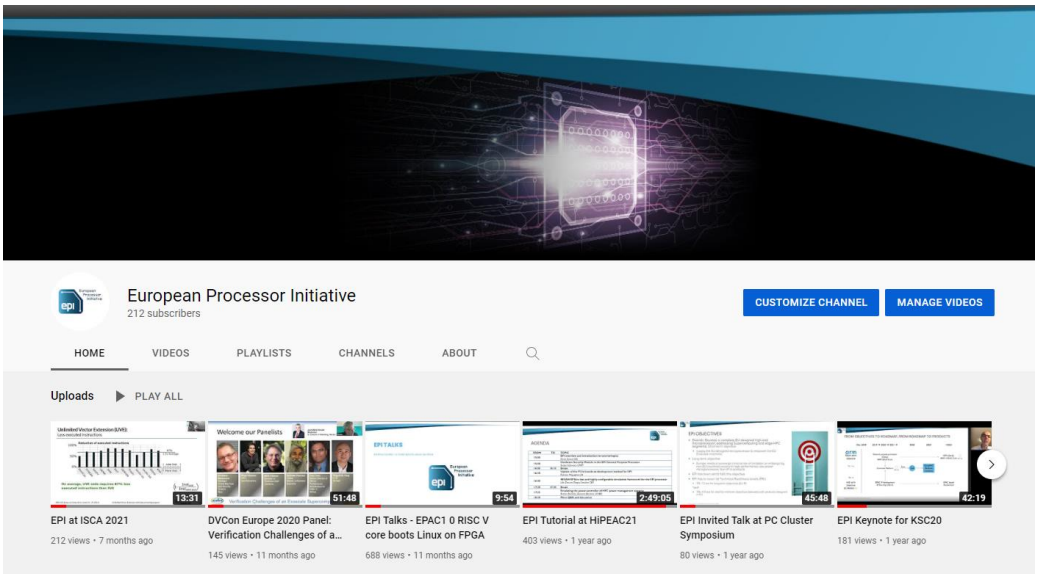

Figure 11. EPI YouTube channel

In the next phase of the project, EPI's YouTube channel will continue to be used as a repository for videos and other AV materials. If there is an opportunity, videos will also be shared on other EPI social media channels, so that the YouTube channel can gather more subscribers and more views.

4 Conclusion

Various dissemination and communication activities have been performed in the first year of the project - participation in several major exhibitions and conferences, interviews, and numerous presentations and talks. EPI has managed to maintain and expand its presence at major events for the HPC community, such as Supercomputing Asia, ISC 2022, Teratec, HiPEAC 2022, and Supercomputing 2022. Partners have participated in many events around the world, showcasing EPI and their work.

This year, there has been a large focus on collaboration with the EUPILOT and EUPEX. We plan to strengthen and continue this collaboration through our online presence (website and social media) and press coverage as well as organizing joint activities such as joint booths.

This document shows that EPI has managed to meet all KPIs and milestones and will try to continue this trend. Since events have returned to in-person, we have managed to distribute many of our materials (posters, flyers and gadgets) at the events. We have also continually updated the website with materials (presentations and articles) from conferences and workshops attended by our partners. In addition, we are continuously working to improve our online presence with interesting articles and generating content. EPI has also had great press coverage, especially with the announcement of Phase 2 and with the press release issued in February by EuroHPC JU.

EPI's academic and industrial partners are working actively to disseminate the project results, which you can read about in this report. In particular, the ACM Summer school organized in August can be highlighted and attracted lots of visitors to the project website.