The European Processor Initiative:
Project overview and co-design for RISC-V accelerators

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EPI OBJECTIVES

Contribute to the development of European supercomputing technologies that can compete on the global HPC market

Strengthen the competitiveness and leadership of European industry and science

Develop key components for the European Union to equip itself with a world-class supercomputing infrastructure
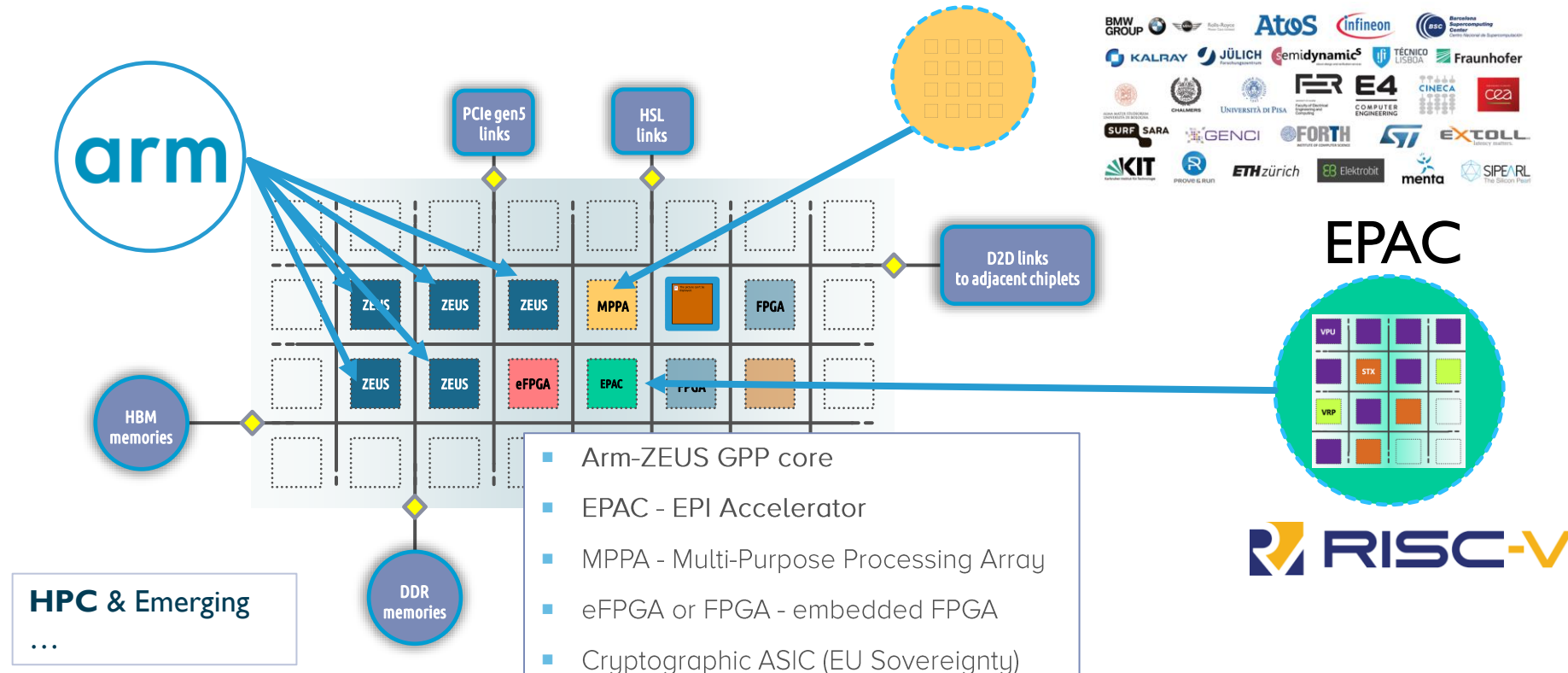
Develope European microprocessor and accelerator technologies with drastically better performance and power ratios; tackle important segments of broader and/or emerging HPC and Big-Data markets

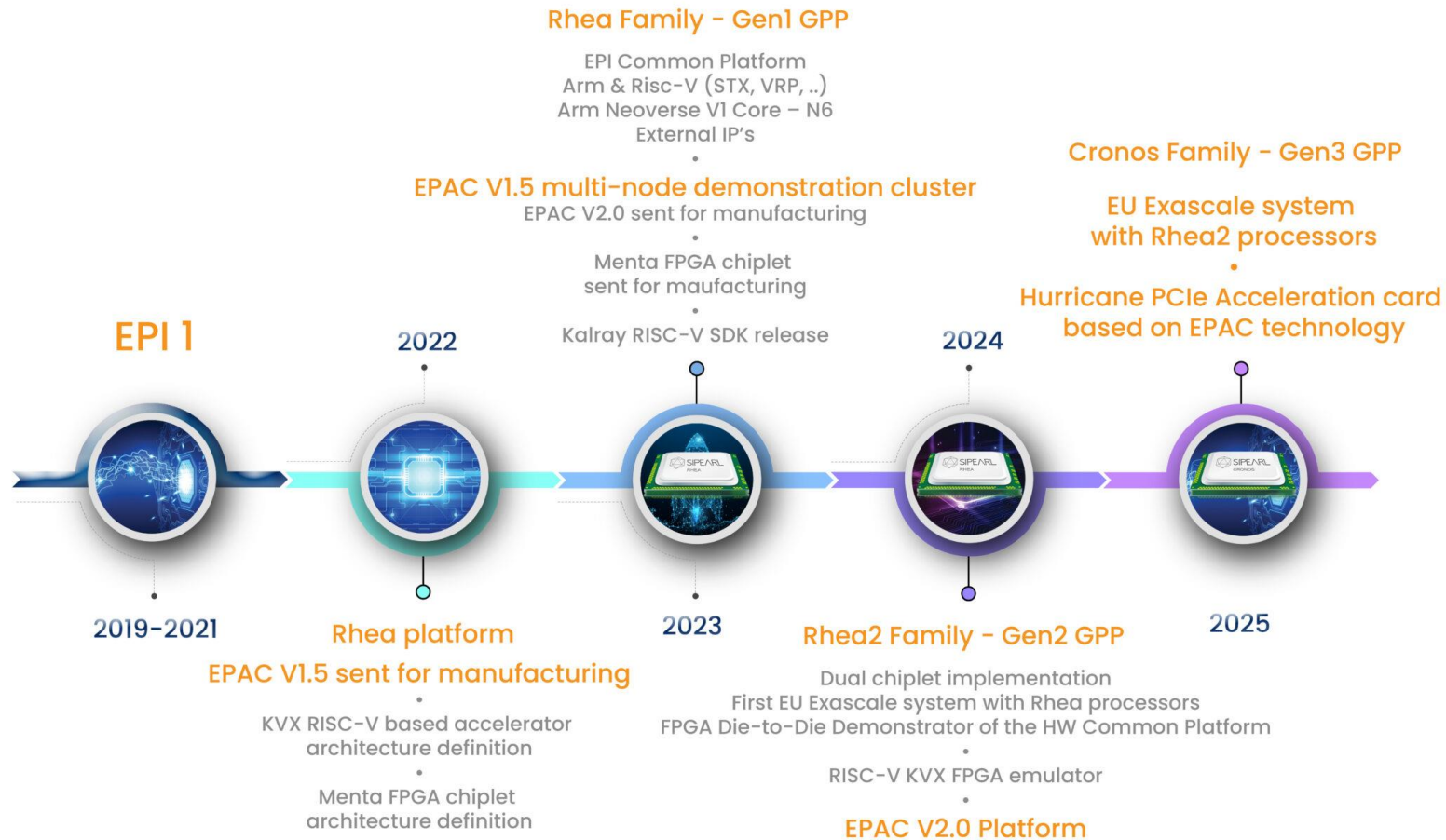More details 👉 Wed, 10:00 – 10:30, talk by Jean-Marc Denis

EPI ORGANIZATION: 3 STREAMS

- **Stream 2 -** General Purpose Processor (GPP)

  - Arm SVE ☞ SiPearl chip integrator

  - Atos/Bull system integrator

- **Stream 3 -** EPI Accelerator (EPAC)

  - RISC-V

  - EU design: BSC. Semidynamics, EXTOLL, FORTH, ETHZ, UniBo, Chalmers, …

- **Stream 1 -** Prototyping EPI technology and co-design of

  - System software

  - Benchmarks and scientific applications

EPAC WITHIN EPI

- Arm-ZEUS GPP core
- EPAC - EPI Accelerator
- MPPA - Multi-Purpose Processing Array
- eFPGA or FPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)

EPI TIMELINE

Rhea Family - Gen1 GPP

EPI Common Platform
Arm & Risc-V (STX, VRP, ..)
Arm Neoverse V1 Core – N6
External IP's

•

EPAC V1.5 multi-node demonstration cluster
EPAC V2.0 sent for manufacturing

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Menta FPGA chiplet
sent for maufacturing

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Kalray RISC-V SDK release

Cronos Family - Gen3 GPP

**EU Exascale system
with Rhea2 processors**

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**Hurricane PCIe Acceleration card
based on EPAC technology**

EPI 1

2022

2024

2019-2021

2023

2025

Rhea platform

EPAC V1.5 sent for manufacturing

KVX RISC-V based accelerator
architecture definition

•

Menta FPGA chiplet
architecture definition

Rhea2 Family - Gen2 GPP

Dual chiplet implementation
First EU Exascale system with Rhea processors
FPGA Die-to-Die Demonstrator of the HW Common Platform

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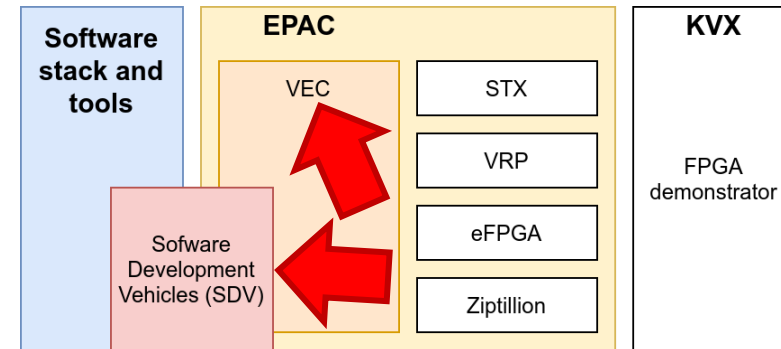RISC-V KVX FPGA emulator

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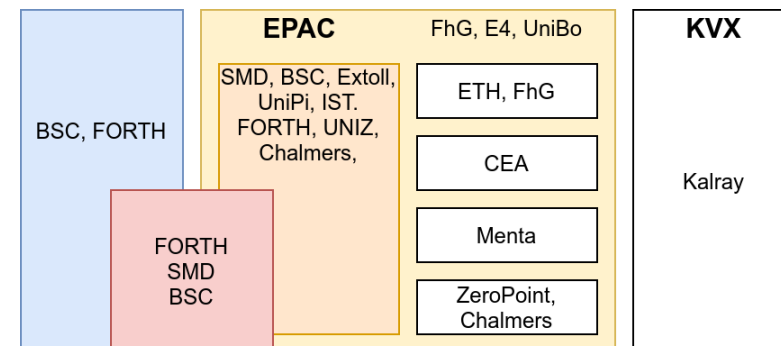**EPAC V2.0 Platform**

VISIONS AND COLLABORATIONS

- **VEC -** Self-hosted RISC-V CPU + wide VPU (256 double elements) supporting RVV 0.7.1 / 1.0

- **STX -** RISC-V CPU + specific cores for stencil and neural network computation

- **VRP -** RISC-V CPU with support for variable precision arithmetic (data size up to 512 bit)

- **eFPGA -** On-chip reconfigurable logic

- **Ziptillion -** IP compressing/decompressing data to/from the main memory

- **KVX -** FPGA demonstrator of the Kalray RISC-V CPU targeting HPC and ML
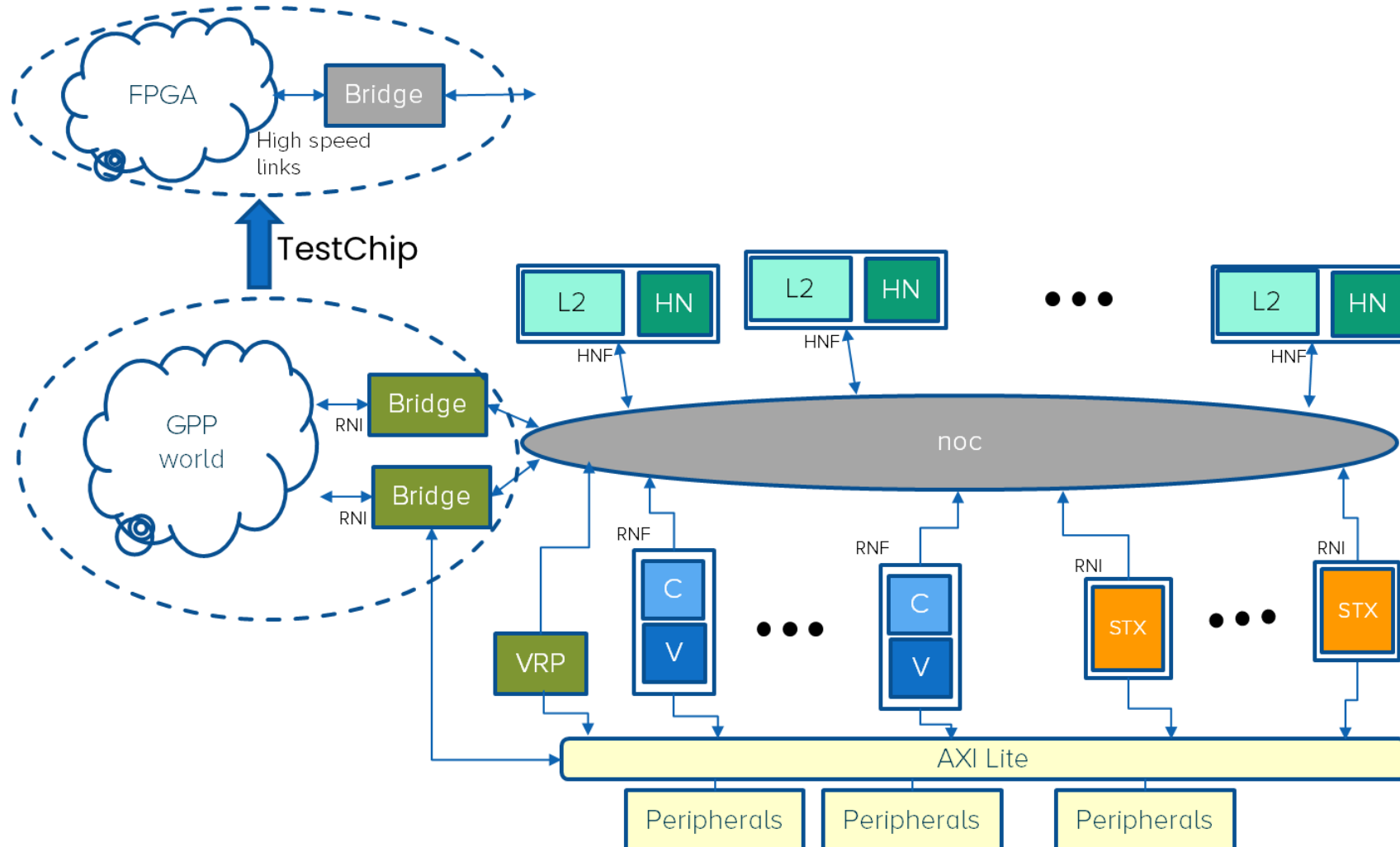
VISION

Software stack and tools	EPAC		KVX
	VEC	STX	
		VRP	FPGA demonstrator
Sofware Development Vehicles (SDV)		eFPGA	
		Ziptillion	

COLLABORATIONS

BSC, FORTH	EPAC	FhG, E4, UniBo	KVX
	SMD, BSC, Extoll, UniPi, IST. FORTH, UNIZ, Chalmers,	ETH, FhG	
		CEA	Kalray
	FORTH SMD BSC	Menta	
		ZeroPoint, Chalmers	

EPAC ARCHITECTURE

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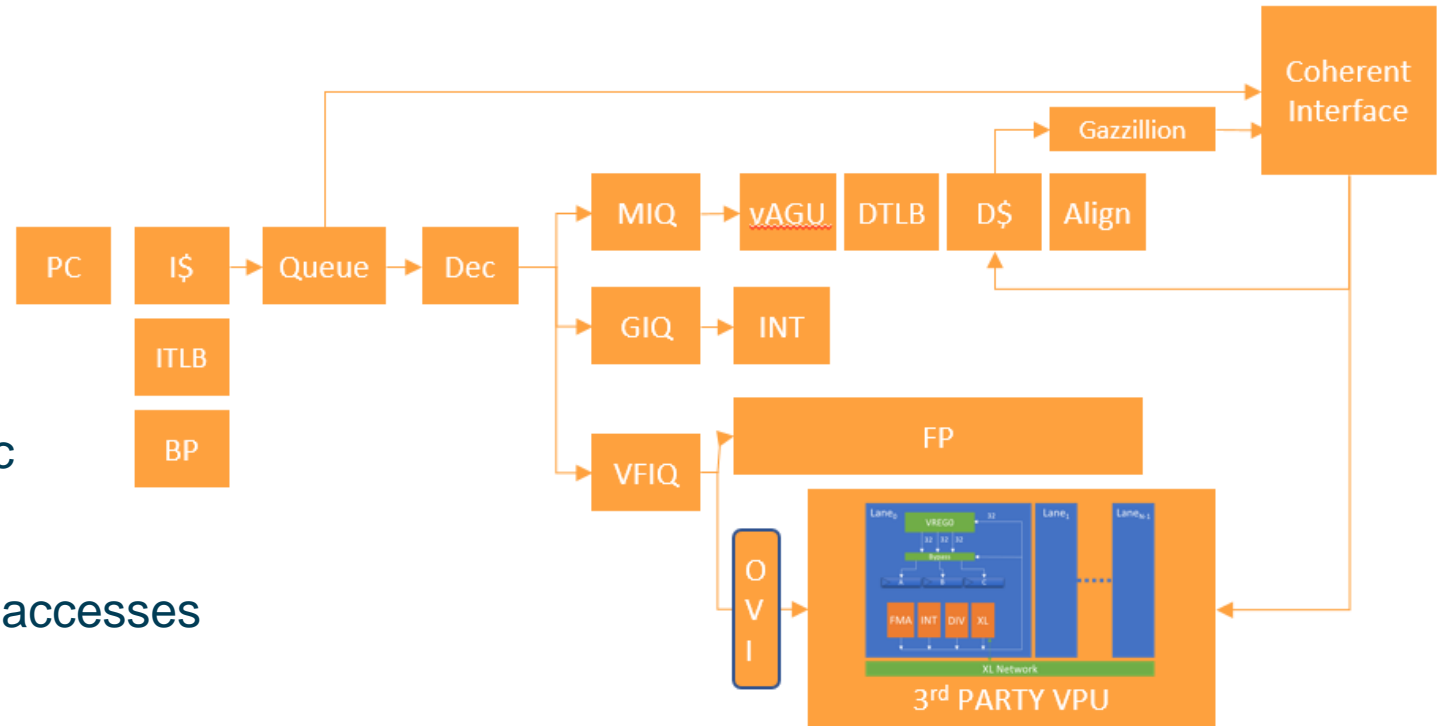
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AVISPADO 220 WITH VPU

RISCV64GCV

- SV48
- 16KB I$
- Decodes upcoming V1.0 vector spec
- 32KB D$
- Full hardware support for unaligned accesses
- Coherent (CHI)
- Vector Memory (vle, vlse, vlxe, vse, ...) processed by MIQ/LSU

Courtesy R. Espasa.

VECTOR PROCESSING UNIT

Architecture	Vector register size (1 cell = 1 double element)																	
Intel AVX512	D1	D2	D3	D4	D5	D6	D7	D8										
Arm Neon	D1	D2																
Arm SVE @ A64FX	D1	D2	D3	D4	D5	D6	D7	D8										
NEC Aurora SX	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	...	D256
RISC-V EPAC Vec	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	...	D256

- Implementation
  - #FUs << VL   (lanes=8, VL=256)
  - Some OoO
    - Resources to overlap?
      - L/S, FU, shuffling
    - Renaming
      - 40 physical registers
  - Single ported register file
    - Large state
    - 5 banks/lane providing sufficient bandwidth for 1 op/cycle (latency/BW trading)
  - Data shuffling: directional ring

"Vitruvius: An Area-Efficient Decoupled Vector Accelerator for High Performance Computing"
F. Minervini, O. Palomar. RISC-V Summit 2021

HOW TO USE THE V-EXTENSION IN OUR PROGRAMS?

- Assembler
  - Always a valid option but not the most pleasant 😁

- C/C++ builtins
  - Low-level mapping to the instructions but allows embedding it into an existing C/C++ codebase
  - Allows relatively quick experimentation

- #pragma omp simd (aka "Semi automated vectorization")
  - Relies on vectorization capabilities of the compiler
    - Usually works but gets complicated if the code calls functions
  - Also usable in Fortran

- Autovectorization
  - All bets are off 😉

SOFTWARE EMULATOR: VEHAVE
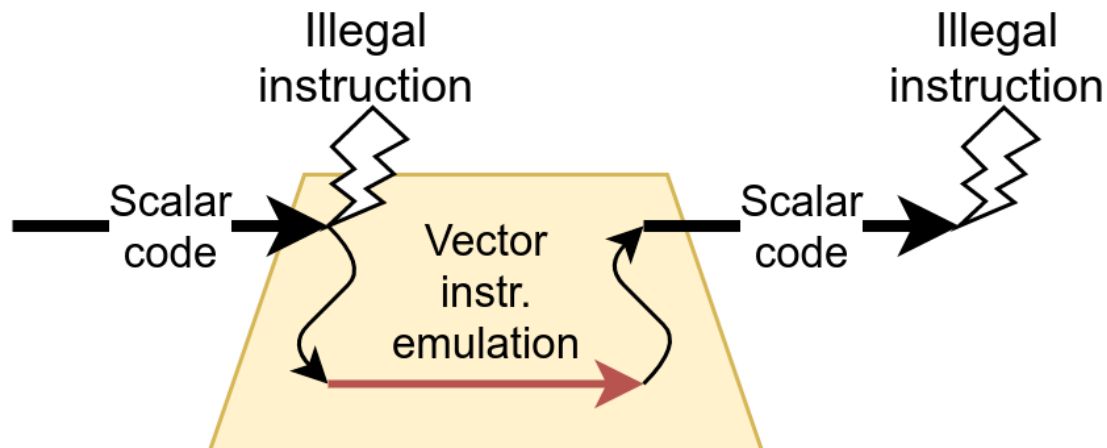
PROS:

- Useful to understand the level of vectorization achieved by the code

- Easy to use and accessible with no need of hardware infrastructure

- It supports RVV-0.7 and RVV-1.0

- Output compatible with Paraver

CONS:

- Slow

- No information about performance (no timing)

RISC-V PLATFORMS: COMMERCIAL AND FPGA-BASED

Self hosted RISC-V vector node @ 50 MHz

RISC-V scalar commercial
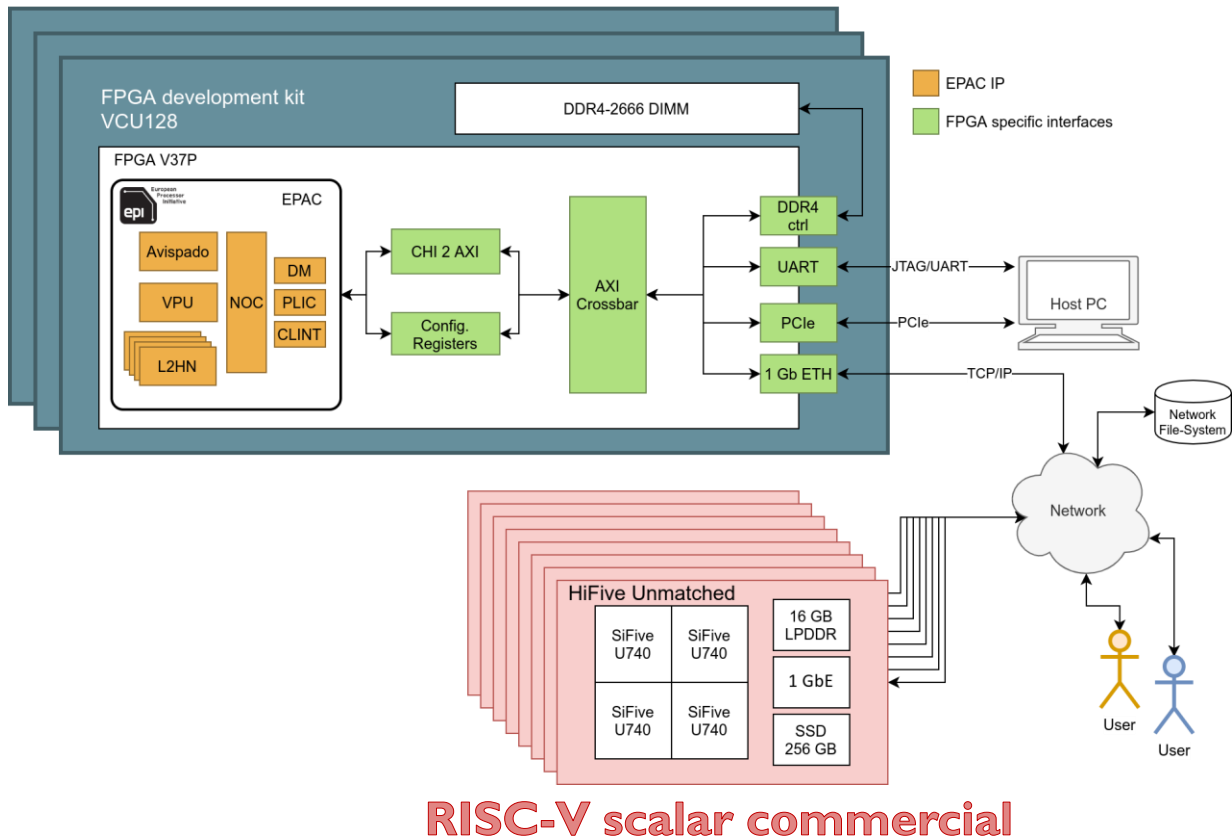
Scalar RISC-V commercial platforms coupled with EPAC development

- Hardware/Software infrastructure for Continuous Integration and RTL check

- Playground to demonstrate a full HPC software stack
  - Linux, compiler, libraries, job scheduler, MPI

- Platform to test latest RTL with complex codes
  - Advances performance analysis tools
  - Accurate timing available

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RISC-V PLATFORMS: COMMERCIAL AND FPGA-BASED

EXAMPLE OF CO-DESIGN STUDY #1

- Sparse Matrix-Vector multiplication

Gómez, Constantino, Filippo Mantovani, Erich Focht, and Marc Casas. "Efficiently running spmv on long vector architectures." In Proceedings of the 26th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, pp. 292-303. 2021.
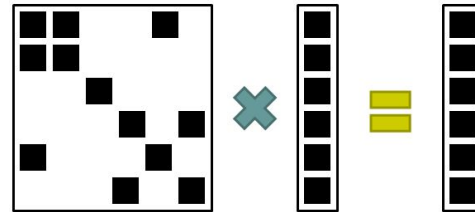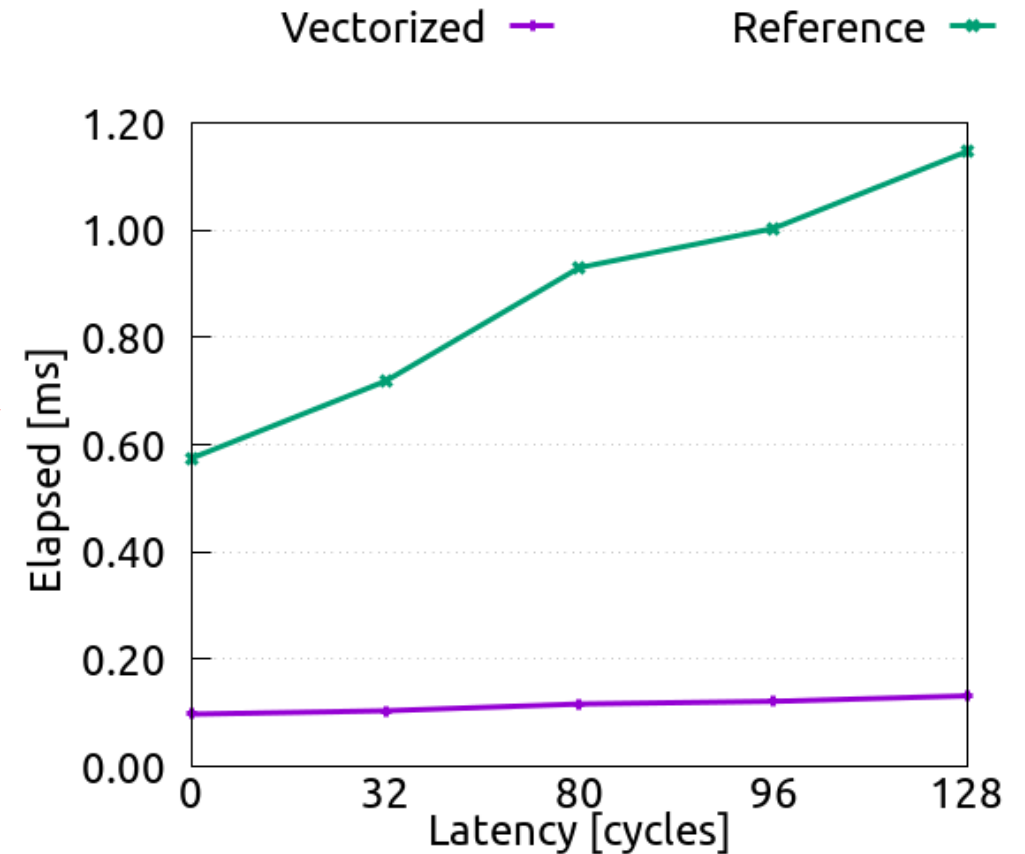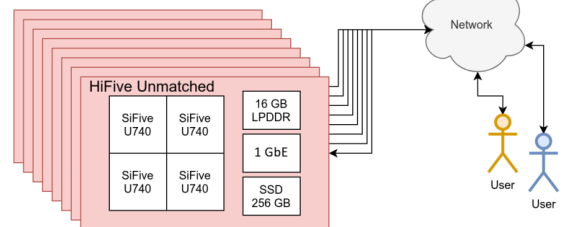
- Naïve implementation struggles taking advantage of the vector unit

- Implementation of "vector friendly" SpMV algorithm: Sell-C-sigma

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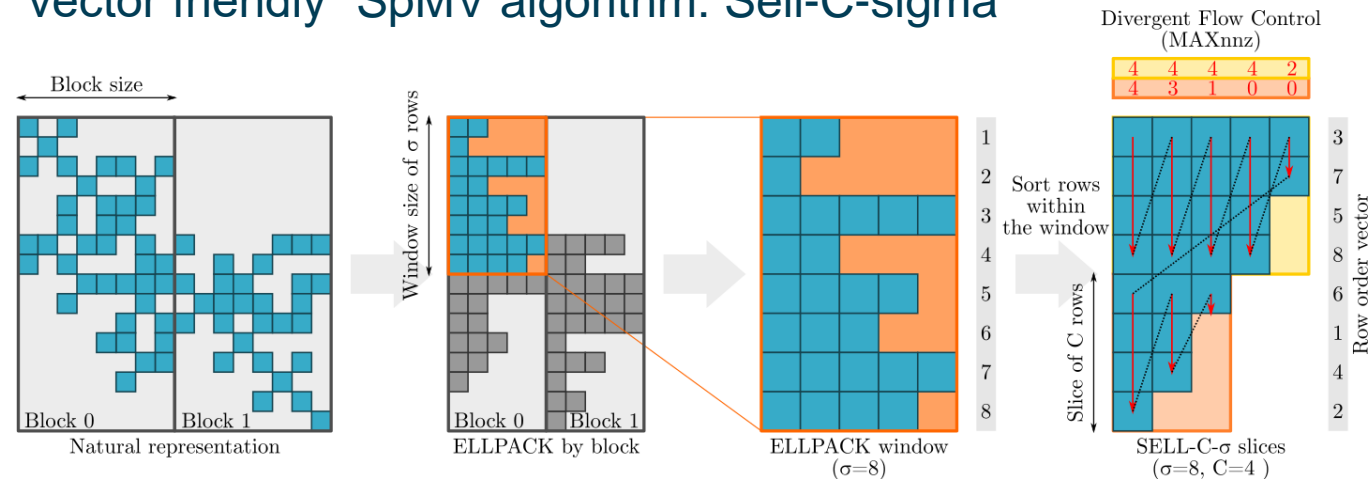
EXAMPLE OF CO-DESIGN STUDY #2

- How sensitive are vectorized/non vectorized codes to the latency accessing the memory?

Self hosted RISC-V vector node @ 50 MHz

Configurable delay
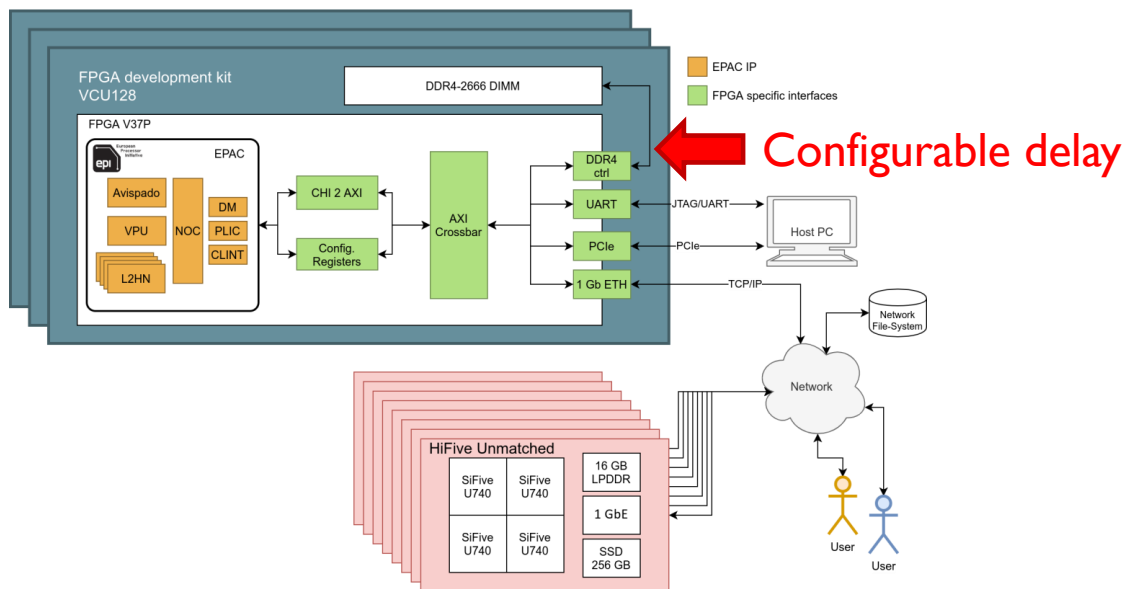
RISC-V scalar commercial

PERFORMANCE ANALYSIS TOOLS

- Fine grained analysis (at level of instructions) is possible

- Graphical representation of timelines

- In depth study can help highlighting:

    1. Low usage of the vector unit
        - Feedback to the **code developer**

    2. Suboptimal saturation or resources (FU, mem)
        - Feedback to the **RTL implementation team**

    3. Suboptimal overlap of instructions
        - Feedback to the **compiler team** (improve scheduling)
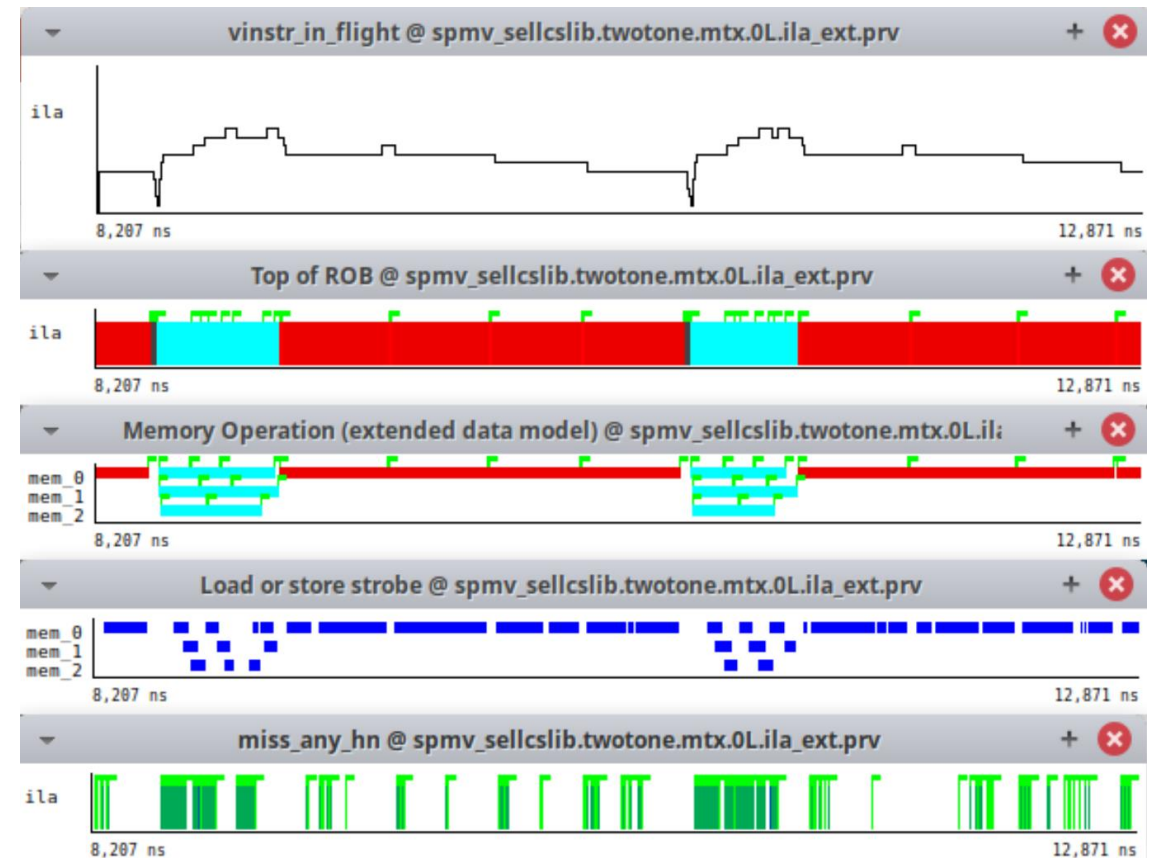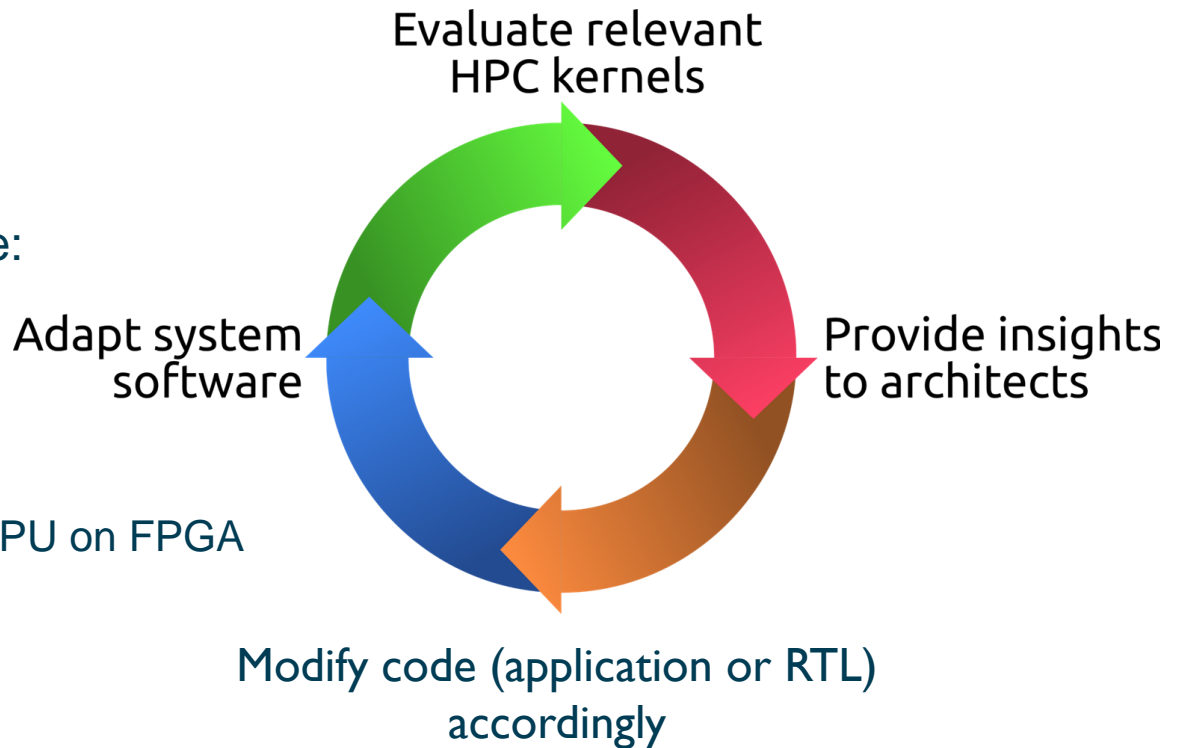
CONCLUSIONS

- EPI develops the first RISC-V based accelerator targeting HPC leveraging the V-extension

    - RTL design of a Vector Unit

    - LLVM compiler support for the V-extension

- While RTL is becoming actual hardware,
  EPI develops tools for boosting the co-design cycle:
  Software Development Vehicles

    - Emulator of V-instructions (Vehave)

    - Commercial RISC-V-based clusters

    - FPGA-sdv: self-hosted RISC-V core coupled with a VPU on FPGA

    - Performance analysis tools

> **Interested in testing your code on EPAC?**
> ☞ Filippo Mantovani filippo.mantovani@bsc.es

Evaluate relevant HPC kernels

Provide insights to architects

Modify code (application or RTL) accordingly

Adapt system software

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CONTACTS

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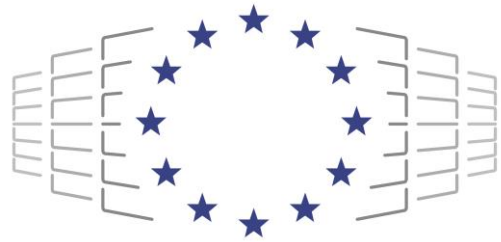
w www.european-processor-initiative.eu

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in [European Processor Initiative](https://www.linkedin.com)

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EPI FUNDING