SemiDynamics RISC-V Cores

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Semidynamics

Semidynamics RISC-V Cores

AVISPADO 222 

2-wide In-Order
Gazzillion Misses™
Ready for RVV 1.0
AXI & CHI

ATREVIDO 222 

2-wide Out-of-Order
Gazzillion Misses™
Ready for RVV 1.0
AXI & CHI

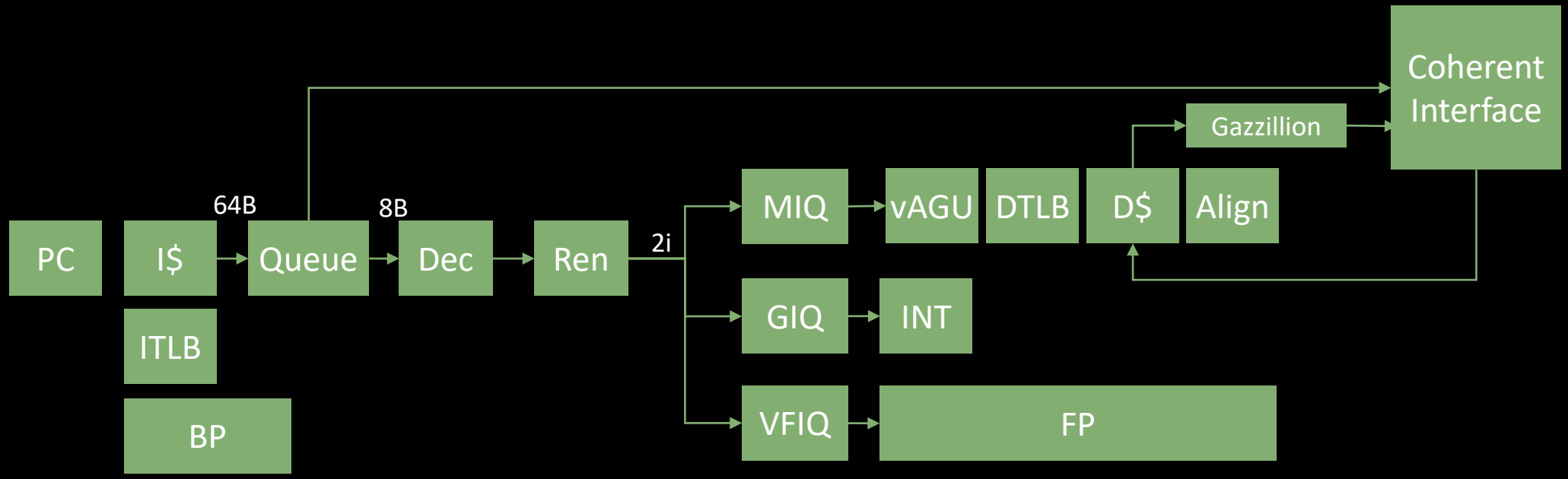
VPU 822 

8-Lane Vector Unit
Supports OOO

IP cores available for licensing

ATREVIDO 222

RISCV64GCV



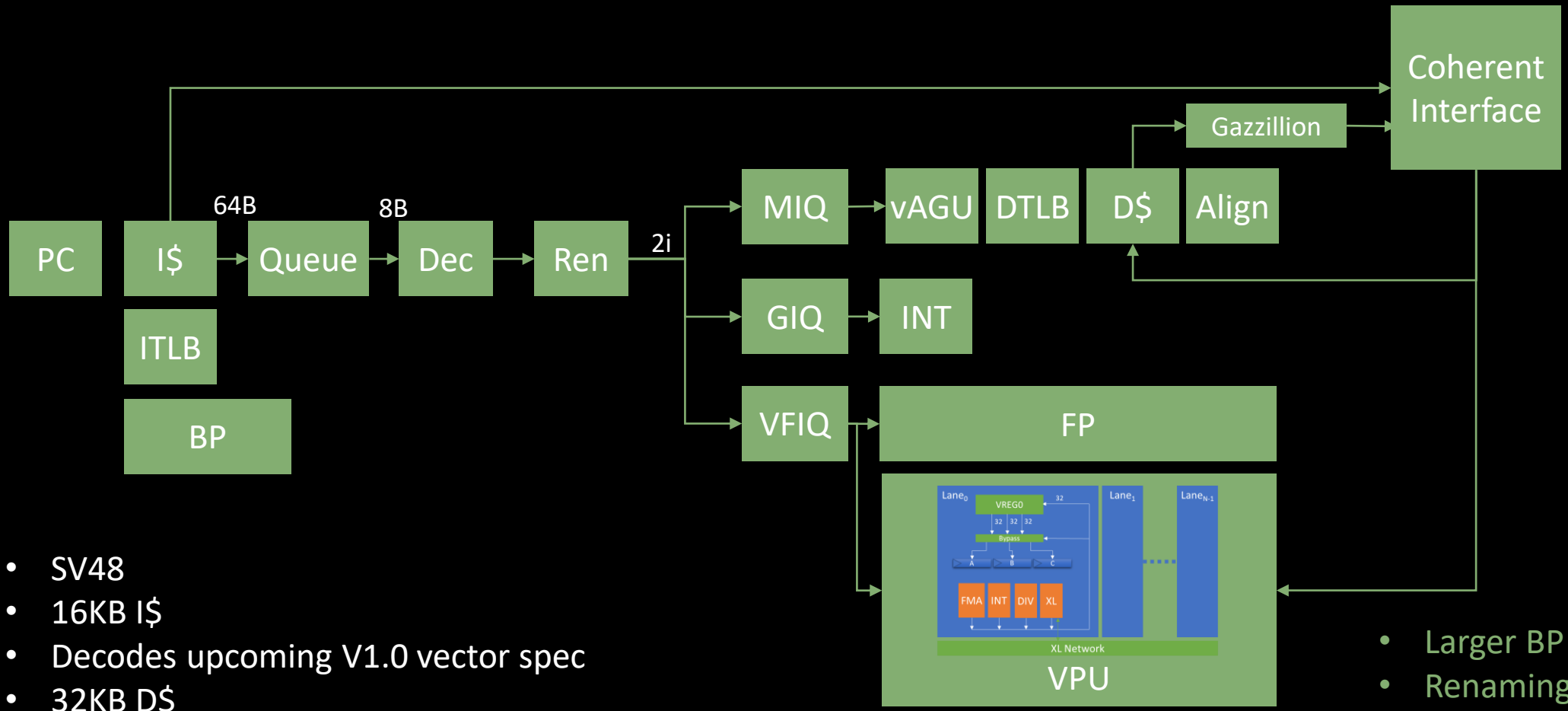
- SV48
- 16KB I$
- Decodes upcoming V1.0 vector spec
- 32KB D$
- Full hardware support for unaligned accesses
- Coherent (CHI)

- Larger BP
- Renaming
- Retirement Logic

Available for licensing

ATREVIDO 222 with OOO VPU (RVV1.0)

RISCV64GCV



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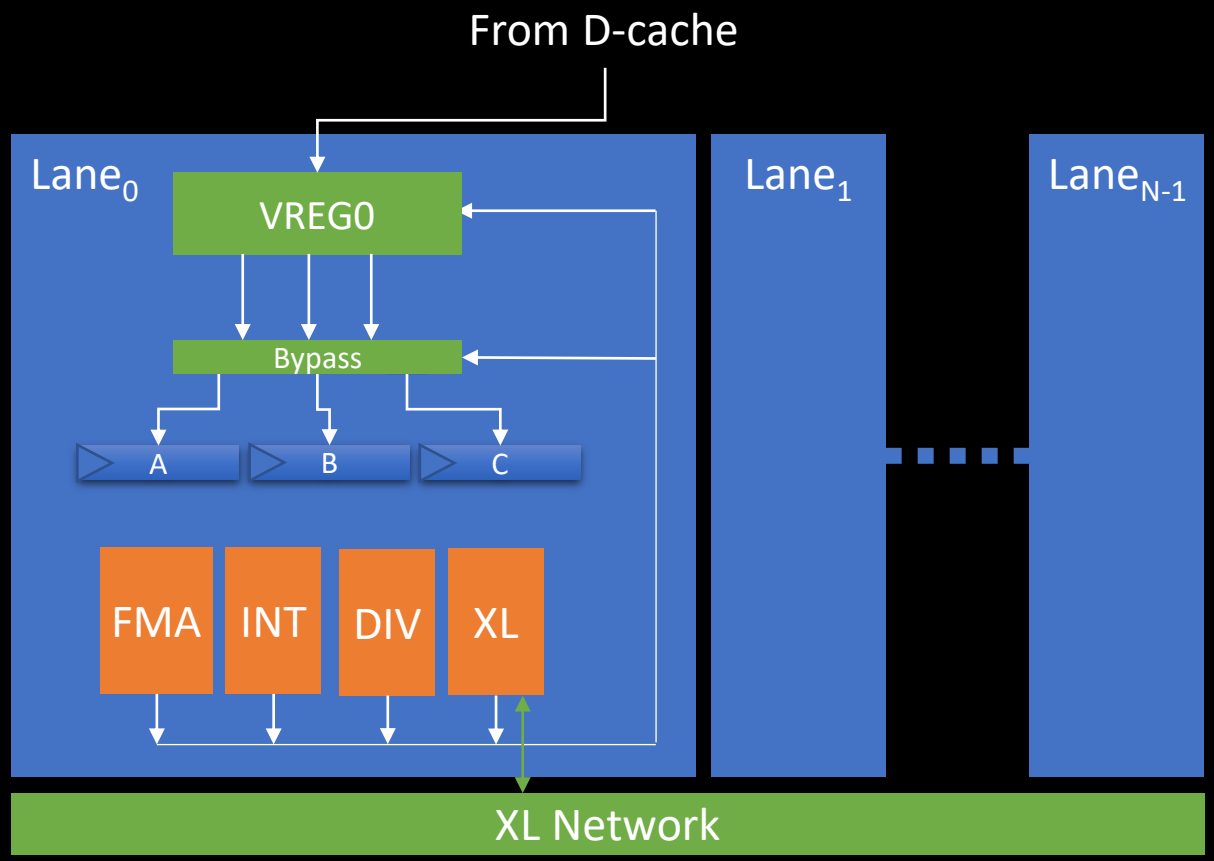
SemiDynamics' VPU

- Implements the RISC-V Vector 1.0 Specification
  - Including lmul, segmented loads
  - No vector atomics currently
- Ready for OOO support
  - Renaming
- Customizable settings
  - VLEN = vector register bits = from 128b to 4096b
  - DLEN = Data path bits = from 128b to 512b
  - Fast cross-lane network for slide/rgather/compress/expand

VPU Block Diagram



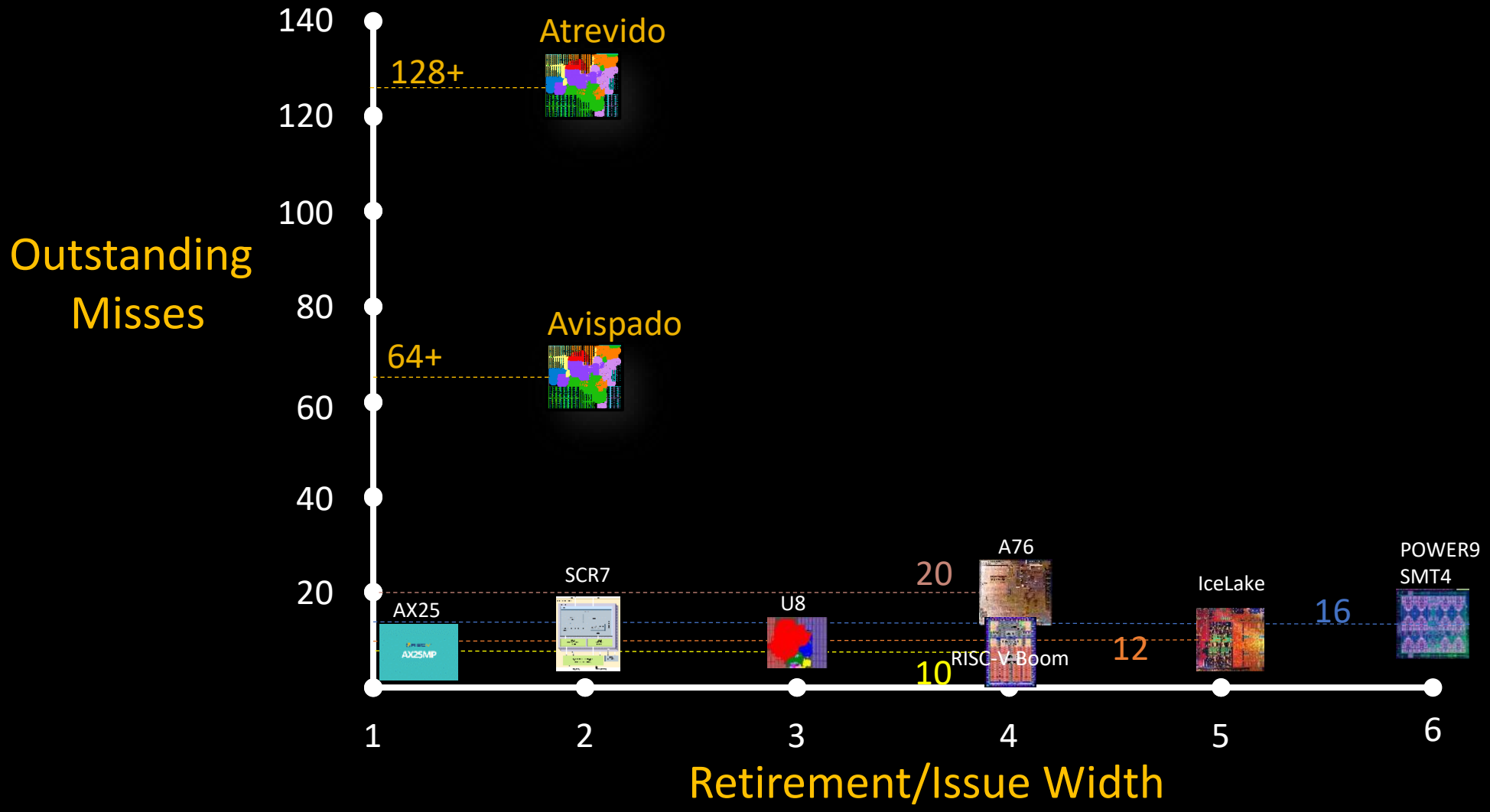
- Lane based organization
- Full cache-line bus from D-cache
- Units per lane
  - FMA
  - INT
  - DIV
  - XL: Cross-lane (rgather, …)
- Full masking support

Gazzillion Misses™

Definition *The ability of Semidynamics' cores to generate a very large number of outstanding memory requests*

Informally *A ton of bandwidth, Good for big data, HPC and AI*

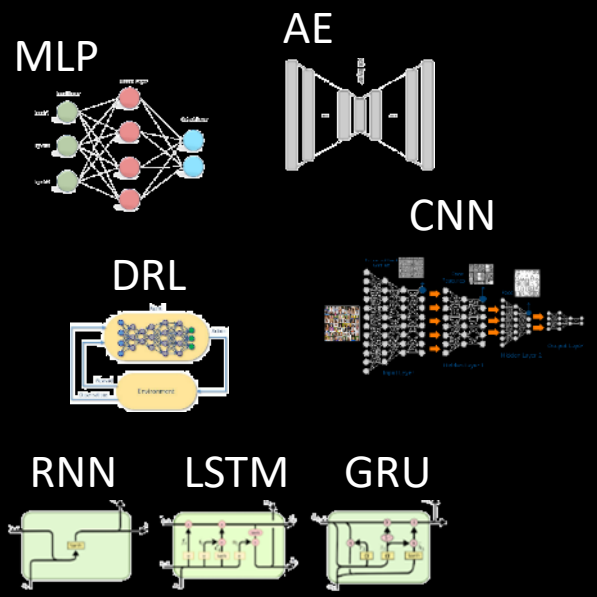
Comparison to other cores



Gazzillion Misses™ good for…

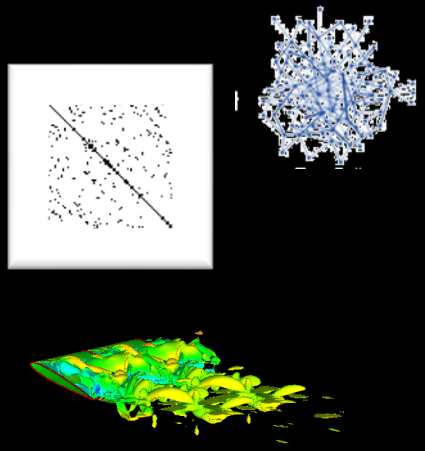
Machine Learning

Recommendation Systems



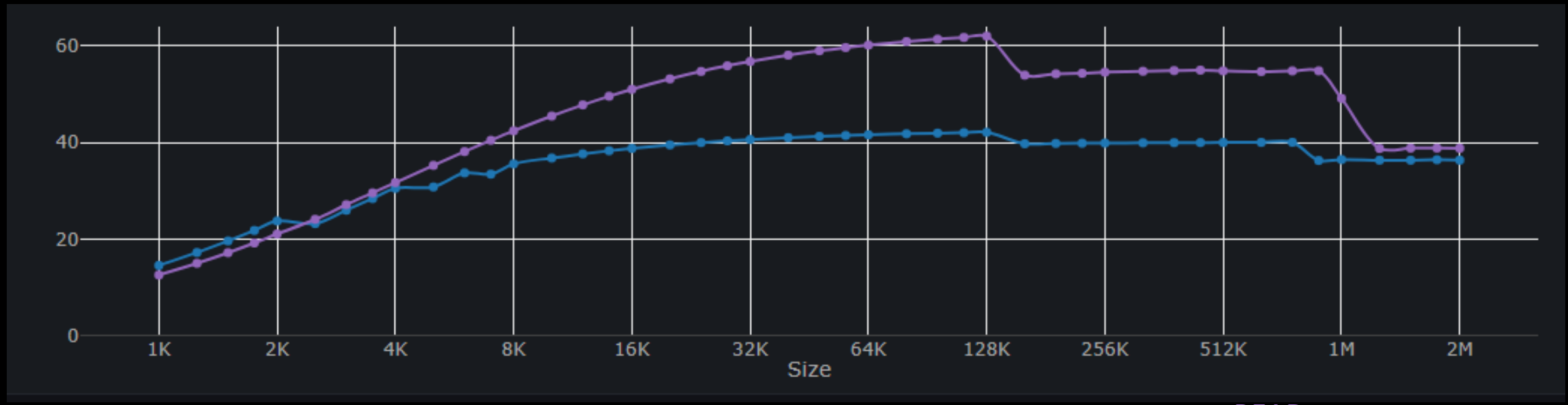
Key-Value Stores

Sparse Data / HPC



Gazzillion Misses™ incredibly good for RVV

Can you find a core out there capable of streaming data at over 60 Bytes/cycle?



Semidynamics RISC-V Cores

- Application cores, in-order and out-of-order, coherent
- Great for “Big data”, “high bandwidth” situations
- Great for RVV

- Happy to share PPA with you under NDA
- Happy to customize the core & the vpu for you

Thank you!

Thank you!