EUROPEAN PROCESSOR INITIATIVE

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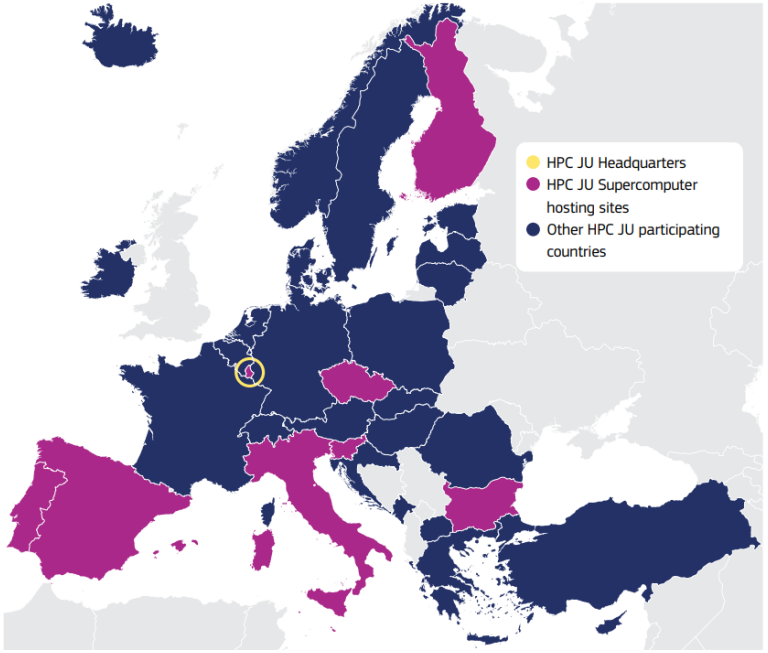
THE STRATEGIC INTERPLAY

EU EXASCALE HPC STRATEGY

- March 2017, Rome: EC launched the ***EuroHPC declaration***
- November 2018, EuroHPC Joint Undertaking, a 1 billion Euro joint initiative between the EU and European countries to develop a World Class Supercomputing Ecosystem in Europe
- 13.7.2021.: EU Council established new EuroHPC JU
  - the 27 Member States, 6 other countries, 2 Private Members
  - €7 billion investment

EuroHPC
Joint Undertaking



EUROHPC JU AMBITIOUS MISSION

- **Supercomputers**
  - reaching the next frontier of high-performance computing: the acquisition of exascale supercomputers
- **Interconnectivity**
  - interconnection through terabit networks of this supercomputing infrastructure, as well as in allowing access from the cloud to a large number of public and private users from anywhere in Europe
- **Applications for life**
  - further development of novel scientific and industrial applications
- **Skills and engagement with business**
  - increased investment in skills, education and training in the use of HPC, co-investment with industry in the acquisition of dedicated systems and in the development of large-scale industrial applications, creation of HPC Centres of Excellence
- **Technology activities**
  - the development of high-end European technologies, for example in the European Processor Initiative (EPI)

DRIVERS OF THE EPI PROPOSAL

Societal challenges

- Climate change
- Cybersecurity
- Increasing energy needs
- Intensifying global competition
- Aging population
- Sovereignty (data, economical, embargo)

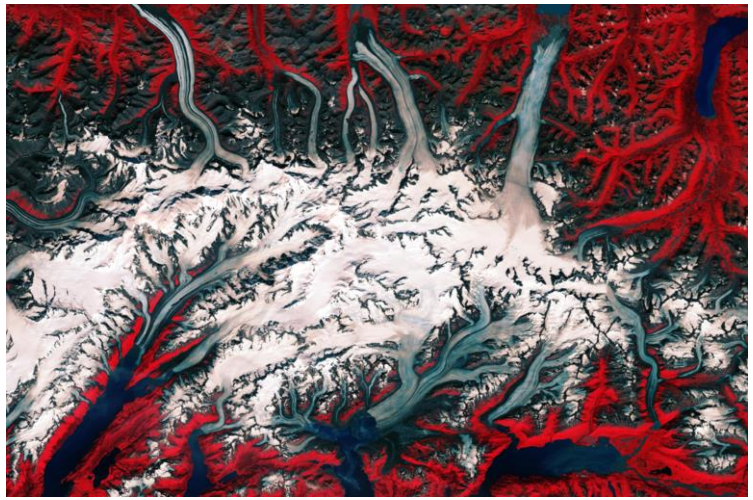


Image: https://www.compbiomed.eu/services/software-hub/

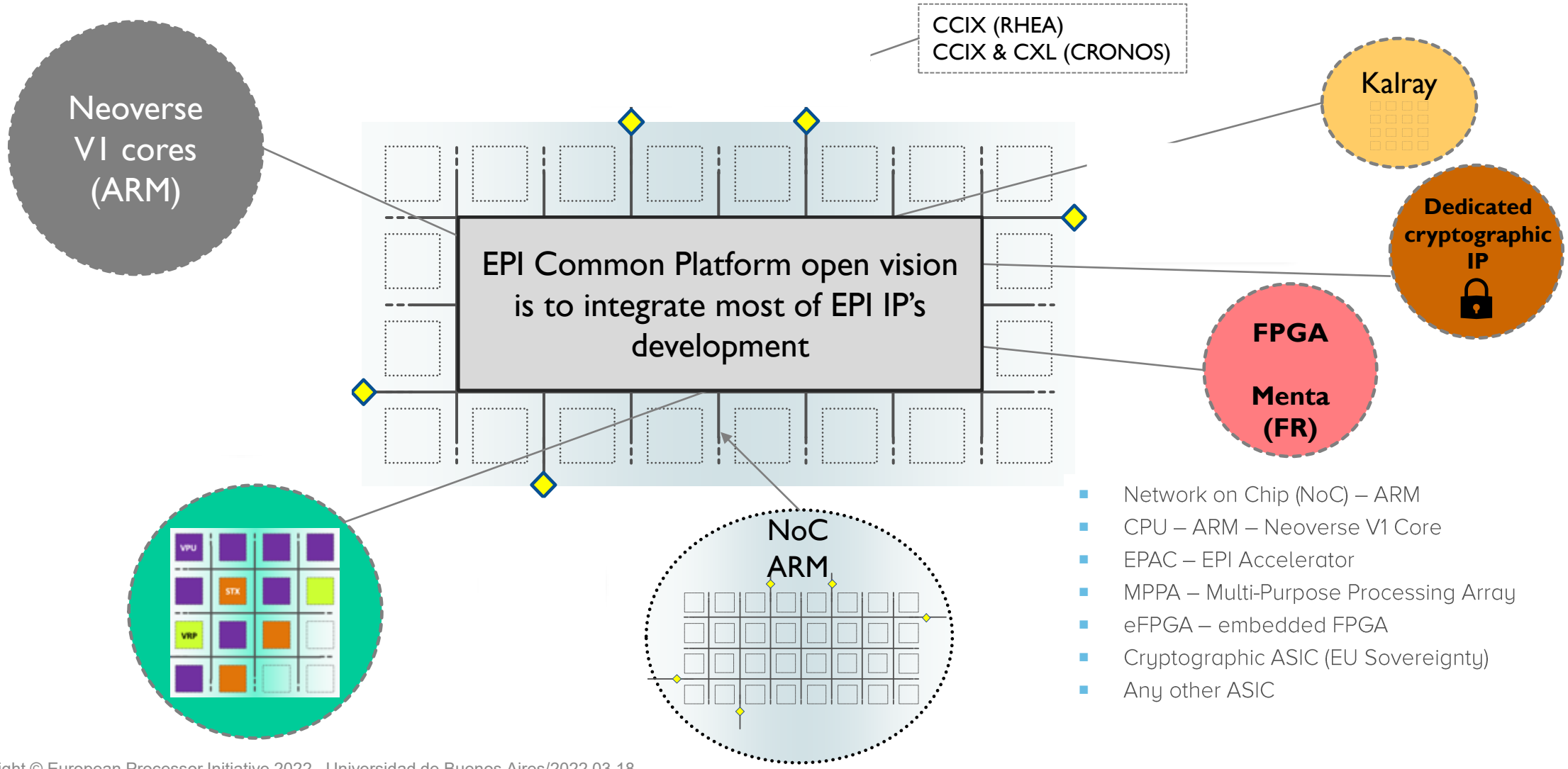
EPI PARTNERS

EPI OBJECTIVES

- Overall: **Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments**
- **Short-term objective**
  - supply the EU-designed microprocessor to empower the future Exascale machines
- **Long-term objective**
  - Europe needs a sovereign access to high-performance, low-power microprocessors, from IP to products
  - contribute to the emergence of Risc-V as an open alternative to proprietary chip standards
  - enable the emergence of an EU high-end processor industry (Arm & Risc-V based) that will have long term benefits

THE EPI TECHNOLOGY: COMMON PLATFORM

GPP AND COMMON ARCHITECTURE



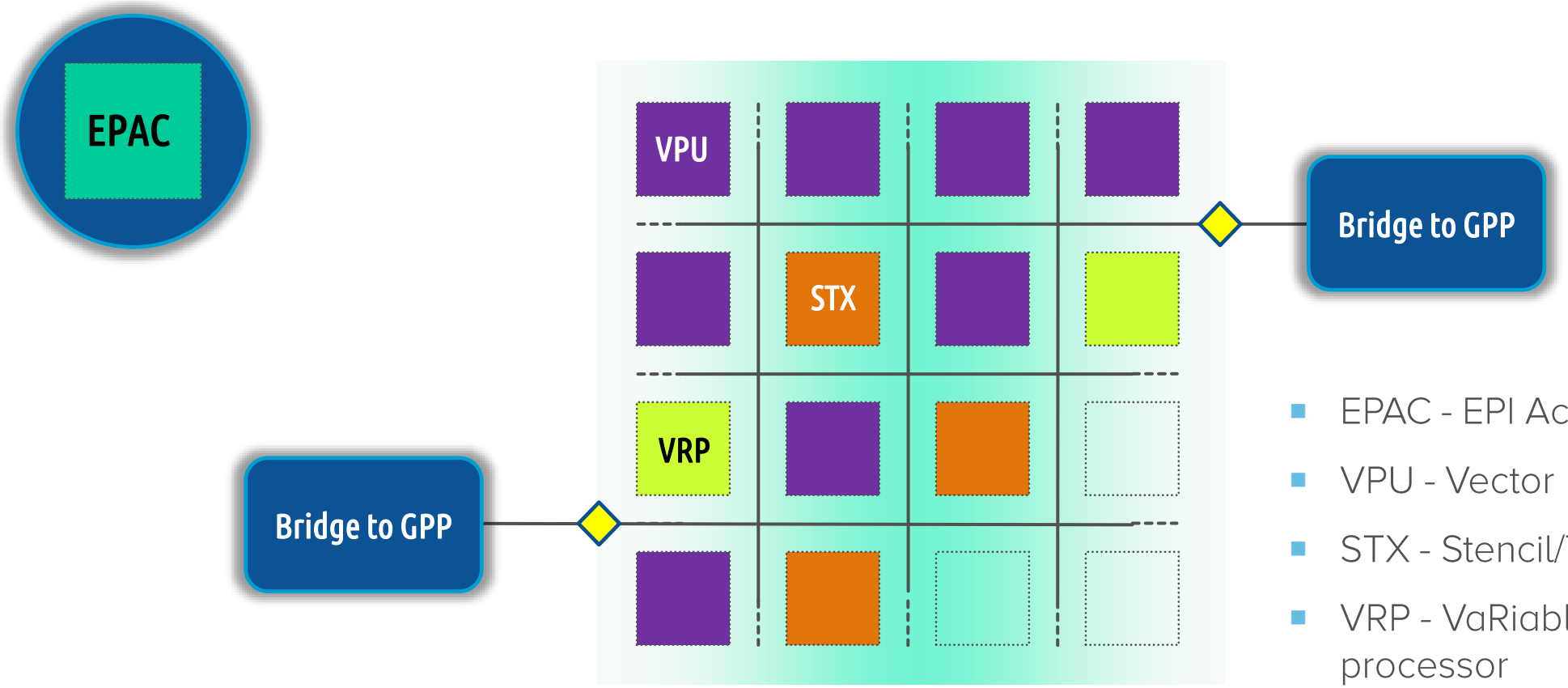
- Network on Chip (NoC) – ARM
- CPU – ARM – Neoverse V1 Core
- EPAC – EPI Accelerator
- MPPA – Multi-Purpose Processing Array
- eFPGA – embedded FPGA
- Cryptographic ASIC (EU Sovereignty)
- Any other ASIC

THE EPI TECHNOLOGY: ACCELERATORS

TOP10 (GREEN) OVER THE LAST 10 YEARS

	2009 – Nov.	2014 – Nov.	2020 – Nov.	2021 – Nov.
CPU only	9	5	2	0
CPU + ACC.	1	5	8	10

EPAC – RISC-V ACCELERATOR FOUNDATIONS

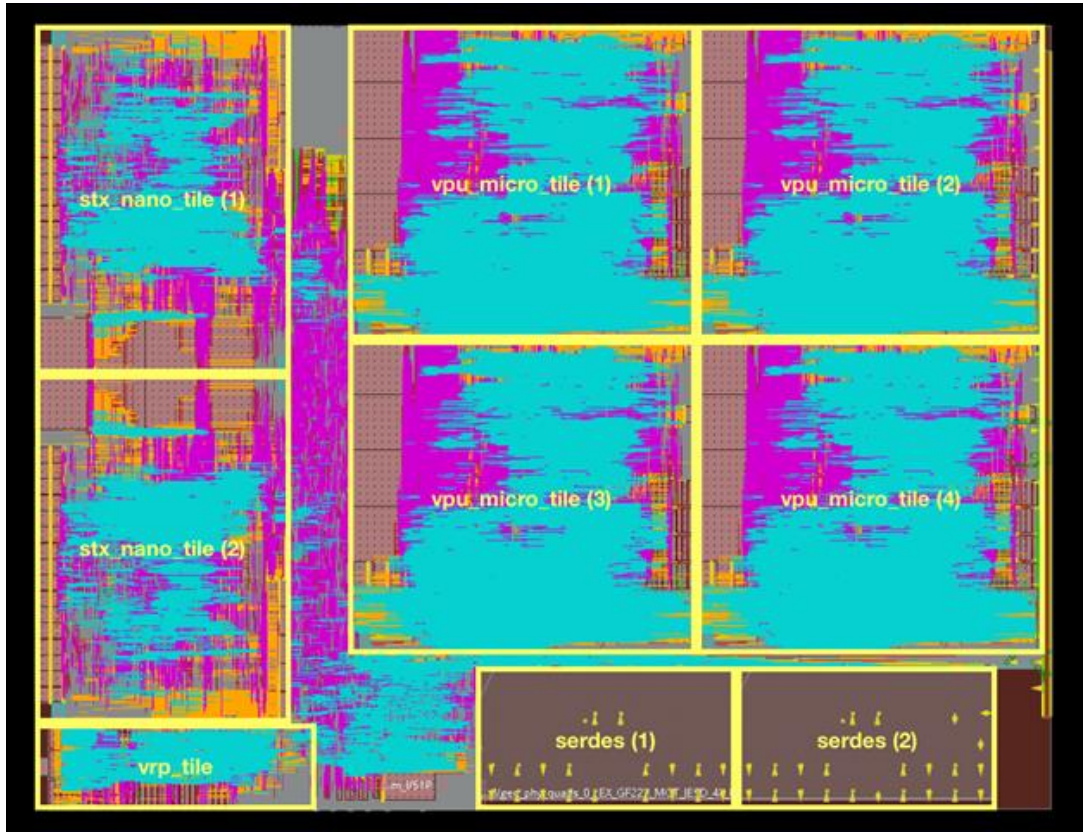


- EPAC - EPI Accelerator
- VPU - Vector Processing Unit
- STX - Stencil/Tensor accelerator
- VRP - VaRiable Precision co-processor

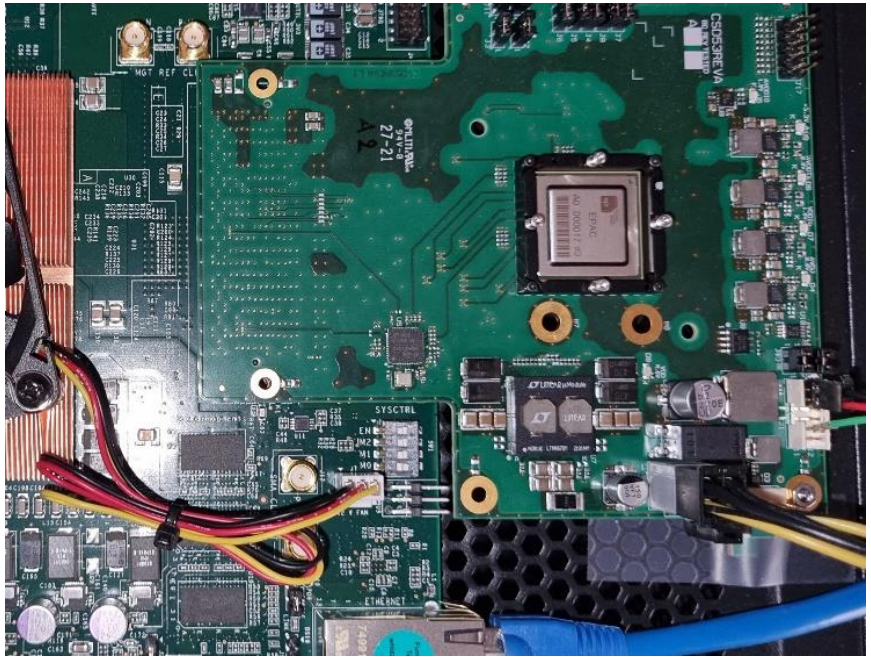
EPAC1.0

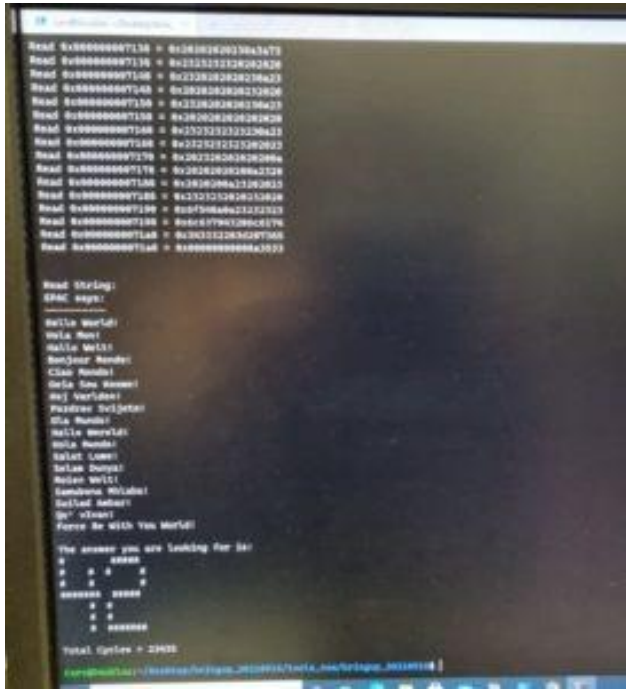
- EPAC test chip combines several accelerator technologies specialized for different application areas:
  - four vector processing micro-tiles (VPU) composed of an Avispado RISC-V core designed by SemiDynamics and a vector processing unit designed by Barcelona Supercomputing Center and the University of Zagreb
  - Home Node and L2 cache, designed respectively by Chalmers and FORTH
  - two additional accelerators:
    - the Stencil and Tensor accelerator (STX) designed by Fraunhofer IIS, ITWM and ETH Zürich
    - variable precision processor (VRP) by CEA LIST
  - All accelerators on the chip are connected with a very high-speed network on chip and SERDES technology from EXTOLL.

EPAC 1.0

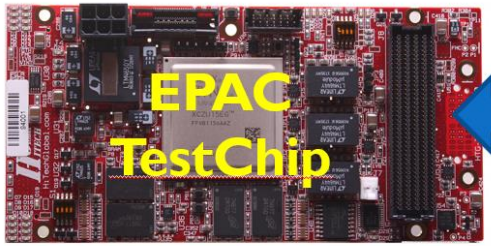


AND THE “HELLO WORLD” IN EU LANGUAGES

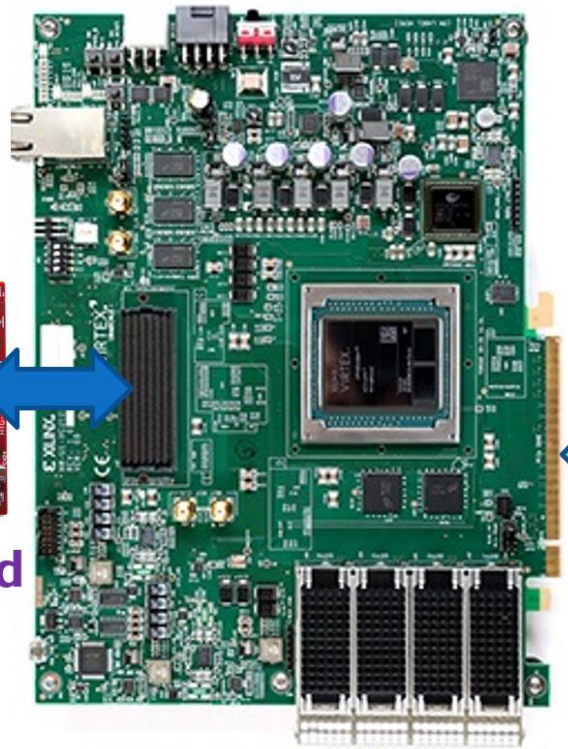




EPAC BOARD SUPPORT FOR EARLY TECHNOLOGY ADOPTERS



EPAC Daughter Board (by E4)

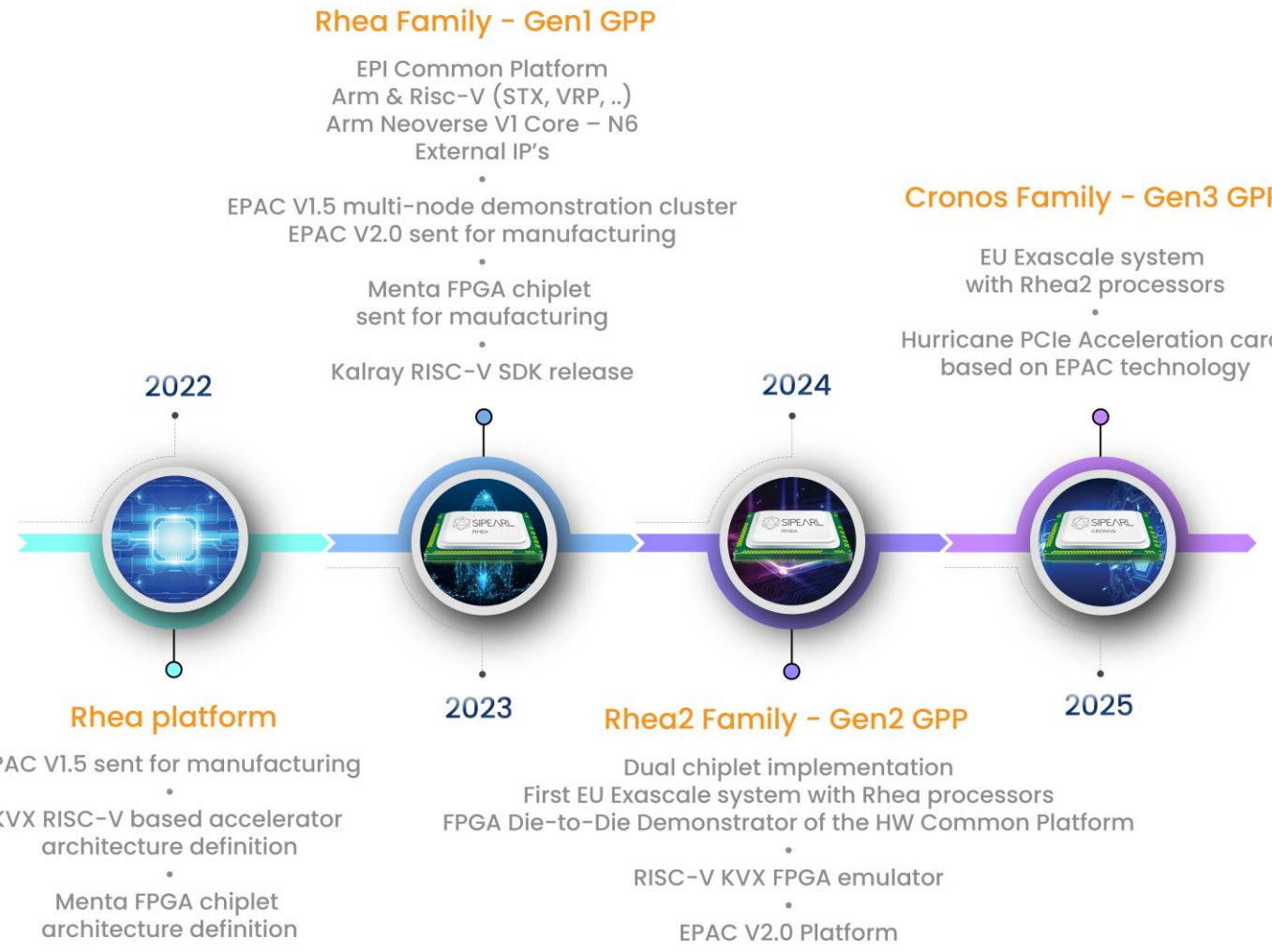


EPAC Carrier Board

Virtex UltraScale+ HBM VCU128 FPGA

EPI PHASE2

EPI2 ROADMAP



EXPECTED OUTCOMES

- We expect, at the end of our second phase, to have
  - The first generation of our GPP validated & exposed to customers
  - The second generation of our GPP designed
  - Several flavours and versions of Risc-V accelerators developed and tested, for instance EPAC 1.5 & 2.0 test chips
- and, as indirect outcomes,
  - developed and validated systems that integrate that GPP into data centres
  - contributed to the emergence of Risc-V as an open alternative to proprietary chip standards
  - enabled the emergence of an EU high-end processor industry (Arm & Risc-V based) that will have long term benefits

EPI CONCLUSION

- Use of HPC and AI is cornerstone of successful address of societal and global challenges
- Future science, technologies and applications require processing of vast amount of data and there is a large need for efficient HPC
- HPC provides needed competitiveness for industry and society
- The expertise for developing high-end and complex processing units in Europe, after decades of dis-investment
- The European Processor Initiative aims to provide an EU HPC processor, accelerators and system/application design for exascale HPC systems in Europe and around the globe

www.european-processor-initiative.eu

@EuProcessor

European Processor Initiative

European Processor Initiative

UNIVERSITY OF ZAGREB

- Founded in 1669
- 29 Faculties, 3 Academies
- approx. 70,000 students
- 167 Undergraduate Programs
- 21 Integrated Programs
- 182 Graduate Programs
- 66 Doctoral Programs
- 146 Postgraduate Specialist Programs

- Studnets enrolled in the 1st year of study:11,500
- PhD degrees:400 / year

FACULTY OF ELECTRICAL ENGINEERING AND COMPUTING (FER)

- ~ 650 employees
- 12 departments
- 4000 students
- 450 PhD students
- Bachelor & Master Study Programs:
  - Electrical Engineering and Information Technology
  - Information and Communication Technology
  - Computing
- PhD Programs:
  - Electrical Engineering
  - Computing

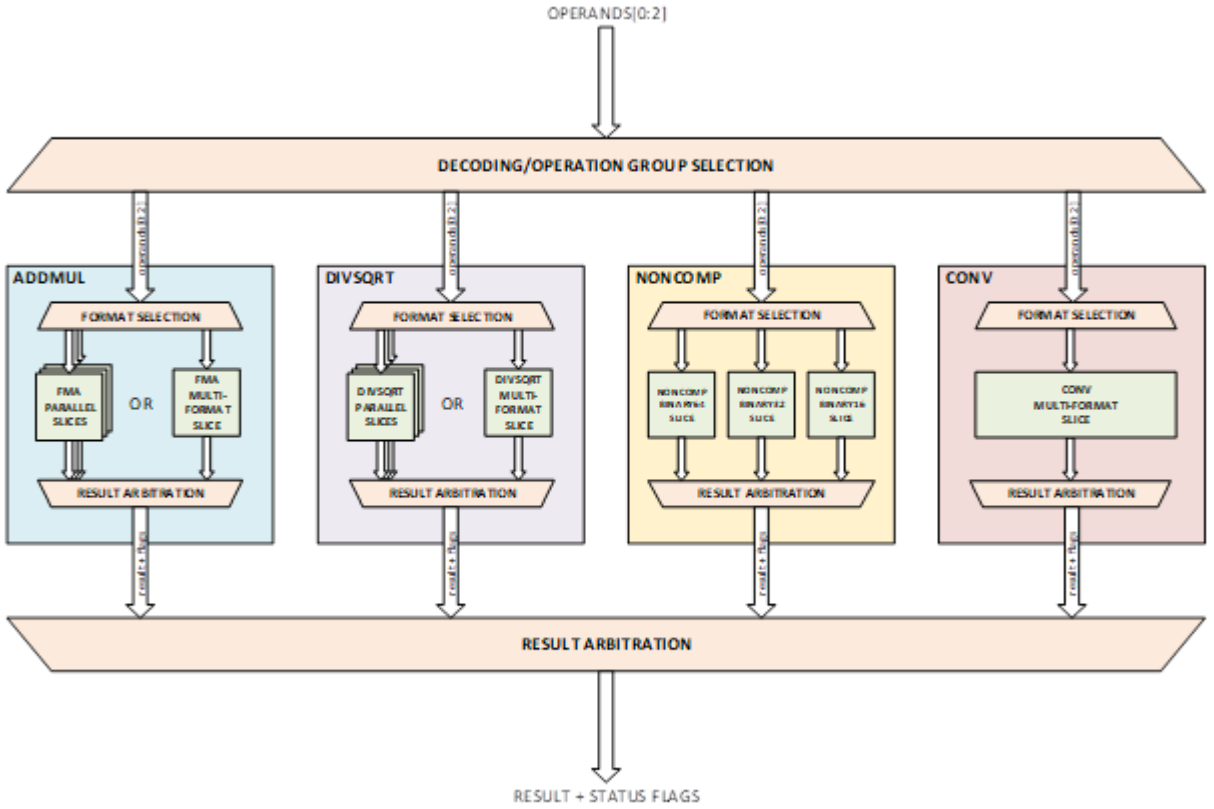
HPC ARCHITECTURES AND APPLICATIONS RESEARCH CENTER @ FER

- GPP/Accelerator architecture
- FAUST – our Risc-V pipelined vector FPU
  - Implemented in EPAC VPU
- Risc-V based accelerators
  - SA
- Imaging apps/optimisations
  - Bolt65
  - Jaguar

FAUST – RISC-V PIPELINED VECTOR FPU

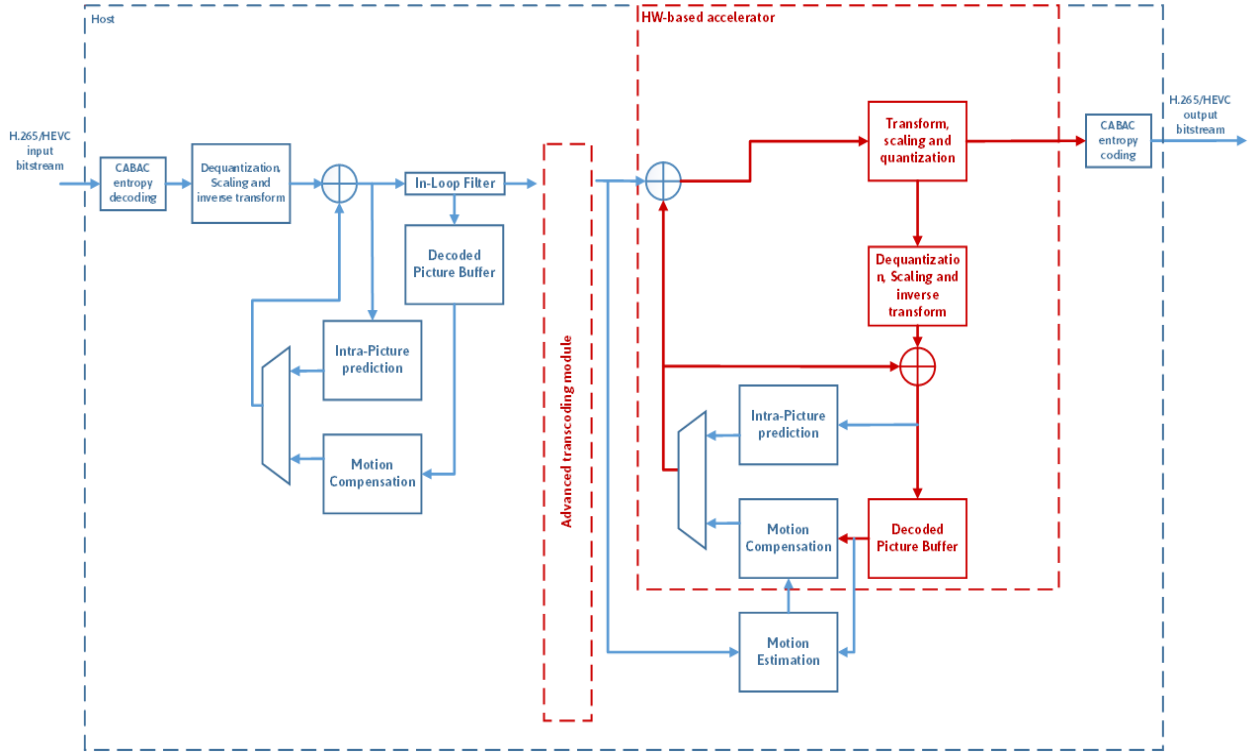
- **Compliance with IEEE 754-2019 Standard**
  - Only minor deviation
- **Supported all floating-point operations defined in RISC-V ISA**
  - RVV 1.0: all operations except reciprocal estimate operations
- **Floating-point formats**
  - binary16 (half precision format)
  - binary32 (single precision format)
  - binary64 (double precision format)
- **Rounding modes**
  - Round to nearest, ties to even
  - Round to nearest, ties to max magnitude
  - Round up
  - Round down
  - Round towards zero
- **Supported all IEEE 754 status flags**
  - Invalid operation
  - Divide by zero
  - Overflow
  - Underflow
  - Inexact
- **Supported subnormal numbers**
- **Support for vector unit integration**
  - Masking support
  - Handshake interface for data flow control to and from the floating-point unit

Parameterized design: configurable architecture and pipeline stages



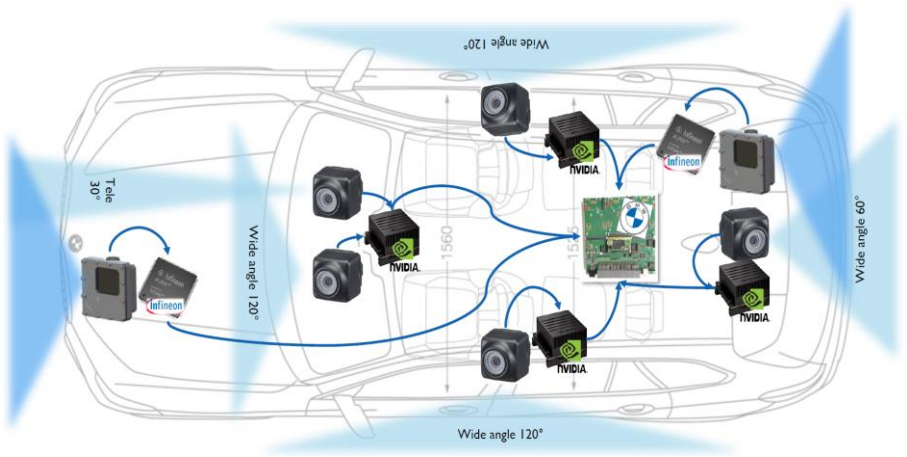
BOLT65

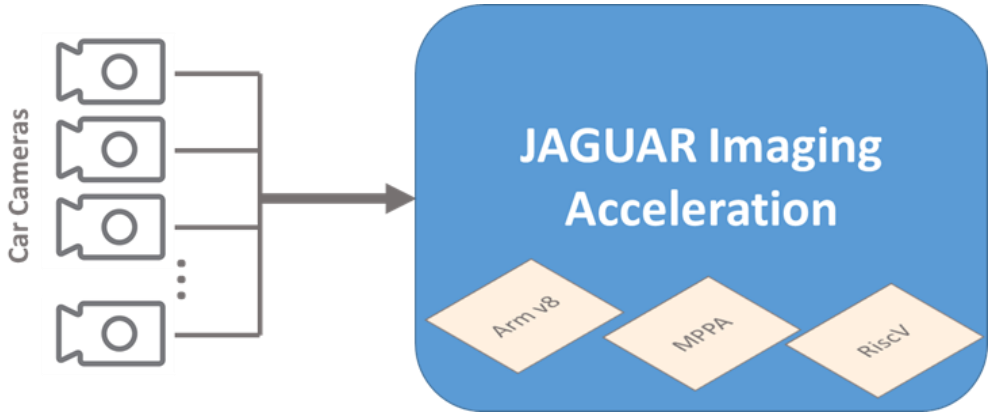
- Bolt65 is a HEVC/H.265 hardware/software suite
  - focus on Just-in-Time video processing
    - constrainted by processing time
  - clean room project created on FER - UNIZG
  - consists of encoder, decoder, transcoder
- Portability
  - written in C++
  - compiled and executed on ARM and x86
  - can be compiled for Linux and Windows
  - no external libraries used
- Optimizations
  - Partially optimized for AVX, SVE, NEON
  - Custom accelerator and GPU support

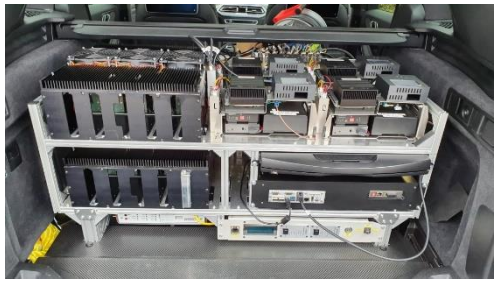


JAGUAR

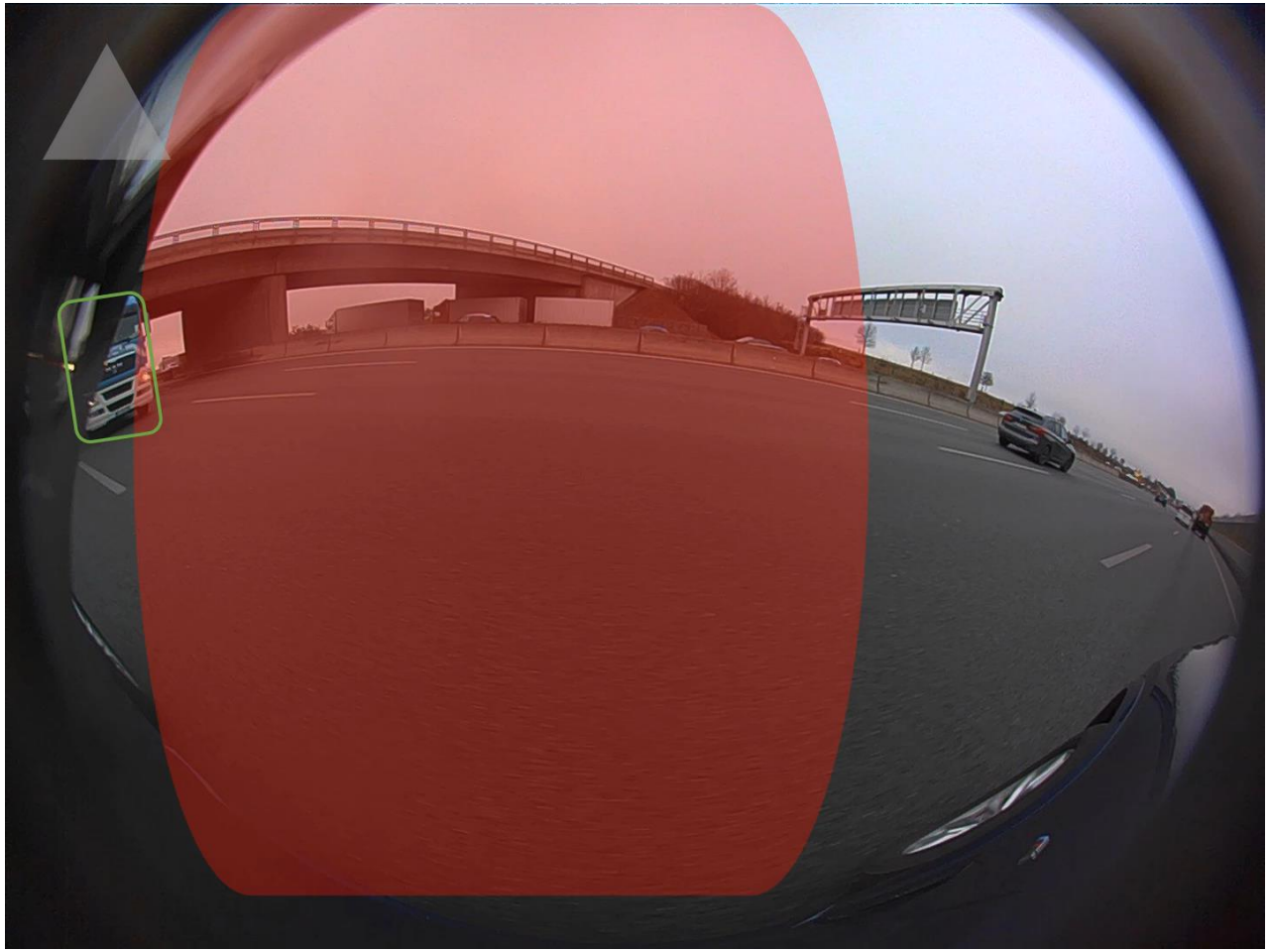
- Jaguar Imaging and AI Framework
  - 8/12-bit JPEG image codec
  - SW/HW accelerator kernels







REAL CAR DRIVING DETECTION RESULTS



Blind spot detection area

Blind spot alert

Detected moving object

UNIZG - UBA POSSIBLE AREAS OF COLLABORATION

- The Agreement between Ministries of science Argentina and Croatia was signed…

THANK YOU FOR YOUR ATTENTION

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