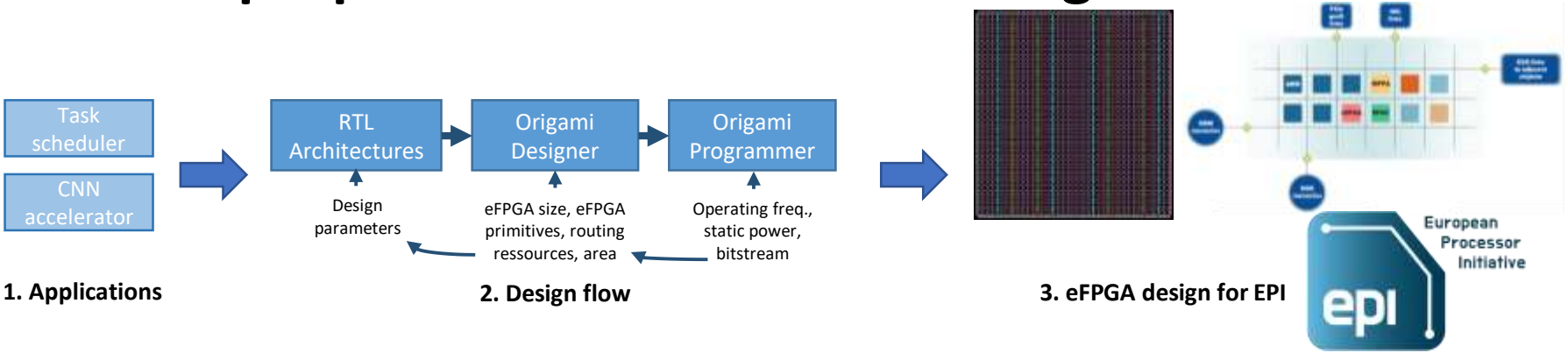
DATE 22
DESIGN, AUTOMATION & TEST IN EUROPE
14 – 15 March 2022 · on-site event
16 – 23 March 2022 · online event
The European Event for Electronic System Design & Test

Towards Reconfigurable Accelerators in HPC: Designing a Multipurpose eFPGA Tile for Heterogeneous SoCs

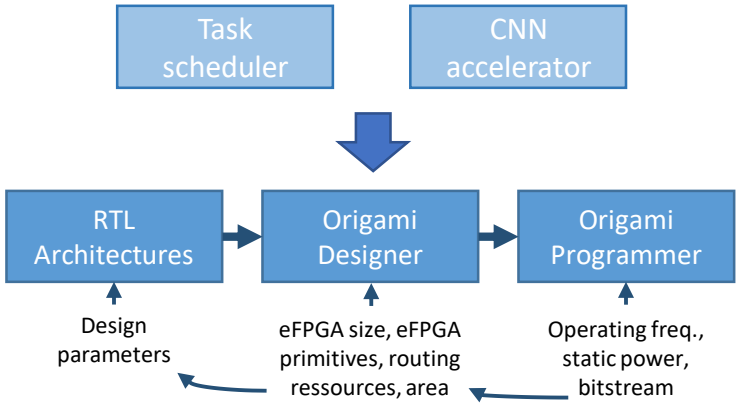


Hotfilter, T.[1]; Kreß, F. [1]; Kempf, F. [1]; Becker, J. [1]; de Haro, J. [2]; Jimenez-Gonzalez, D. [2]; Moreto, M. [2]; Alvarez, C. [2]; Labarta, J. [2]; Baili, I. [3]

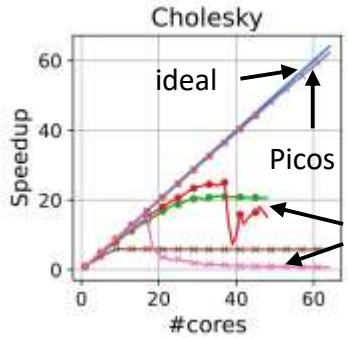
[1] Karlsruhe Institute of Technology (KIT) [2] Barcelona Supercomping Center, Universitat Politècnica de Catalunya (UPC) [3] Menta S.A.S.

Path to a well-fitting eFPGA for EPI

- **Research challenges**
  - Stick to the 1% area budget
  - Ability to host both architectures
  - Keep flexibility for future use cases



- **Results**
  - 38 x 40 eFPGA shape
  - Static power: 1,74 mW (7nm Process)
  - CNN: Face recognition in 150 ms
  - Picos: near perfect scalability
  - Enough and diverse resources for future architectures



SW run-times

Parameter	Amount	Util. CNN	Util. Picos
LUT6	9632	78%	51%
FFs	12086	72%	29%
DSPs	52	92%	0%
Memories	80 (2Kx16)	5%	46%
f_{max}		159 MHz	100 MHz