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EXCELENCIA SEVERO OCHOA

RISC-V in Europe: The Road to an Open Source HPC Stack

John D. Davis, Ph.D.

3/2022

Overview

- BSC Background
- The HPC Vision
- RISC-V HPC Research in Europe
- Concluding thoughts

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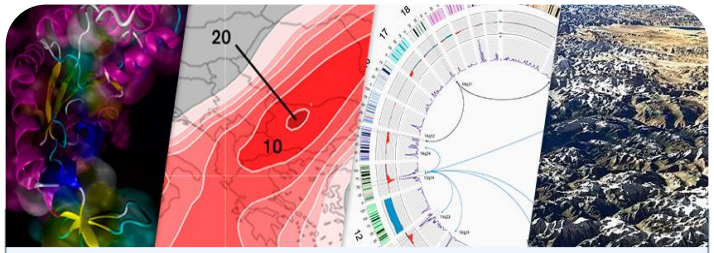
BSC-CNS objectives

Supercomputing services
to Spanish and EU researchers



R&D in Computer, Life, Earth and
Engineering Sciences

PhD programme, technology
transfer, public engagement

BSC-CNS is a consortium that includes

Spanish Government	**60%**	Gobierno de España · Ministerio de Ciencia, Innovación y Universidades
Catalan Government	**30%**	Generalitat de Catalunya · Departament d'Empresa i Coneixement
Univ. Politècnica de Catalunya (UPC)	**10%**	Universitat Politècnica de Catalunya · BarcelonaTech

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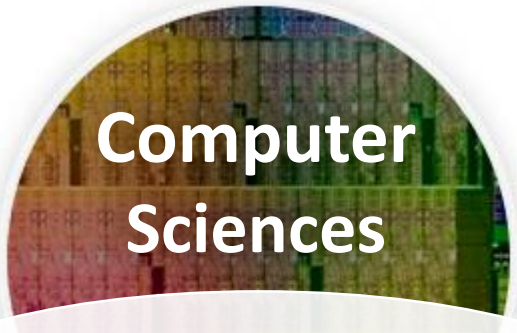
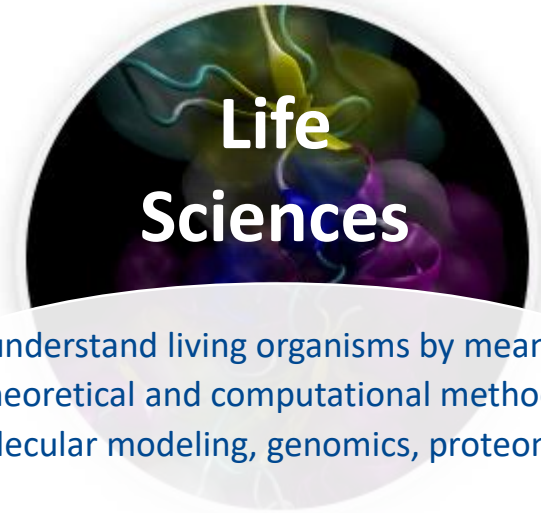
Mission of BSC Scientific Departments



To influence the way machines are built, programmed and used: programming models, performance tools, Big Data, Artificial Intelligence , computer architecture, energy efficiency

To develop and implement global and regional state-of-the-art models for short-term air quality forecast and long-term climate applications



To understand living organisms by means of theoretical and computational methods (molecular modeling, genomics, proteomics)

To develop scientific and engineering software to efficiently exploit super-computing capabilities (biomedical, geophysics, atmospheric, energy, social and economic simulations)

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June 2020

MareNostrum 4

Total peak performance: **13.9** Pflops		
General Purpose Cluster:	11.15 Pflops	(1-07-2017)
CTE1-P9+Volta:	1.57 Pflops	(1-03-2018)
CTE2-Arm V8:	0.65 Pflops	(12-2019)
CTE3-AMD:	0.52 Pflops	(12-2019)

MareNostrum 5 Coming Soon!

MareNostrum 1
2004 – 42.3 Tflops
1st Europe / 4th World
New technologies

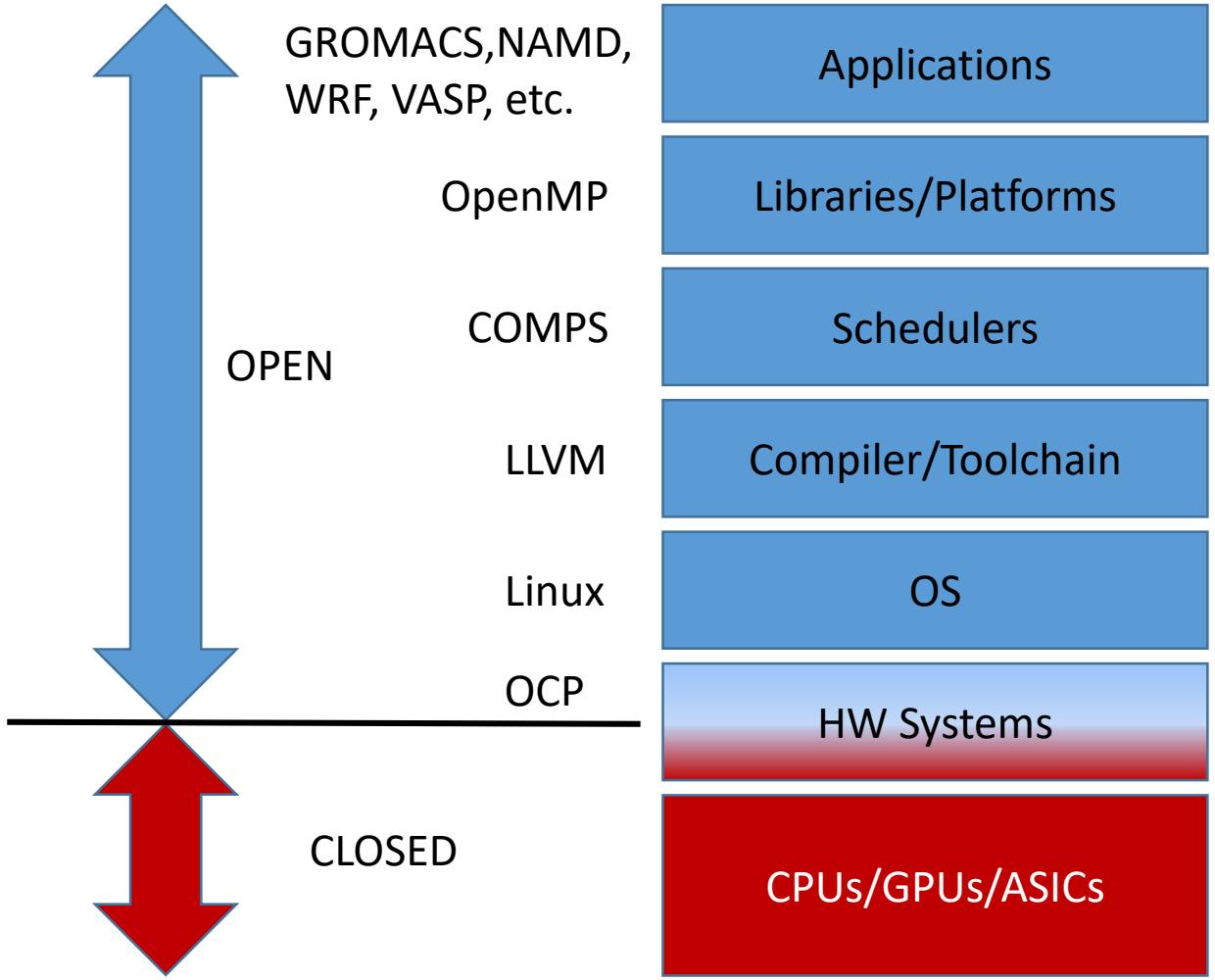
MareNostrum 2
2006 – 94.2 Tflops
1st Europe / 5th World
New technologies

MareNostrum 3
2012 – 1.1 Pflops
12th Europe / 36th World

MareNostrum 4
2017 – 11.1 Pflops
2nd Europe / 13th World
New technologies

HPC Today

- **Europe has led the way in defining a common open HPC software ecosystem**
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU?**



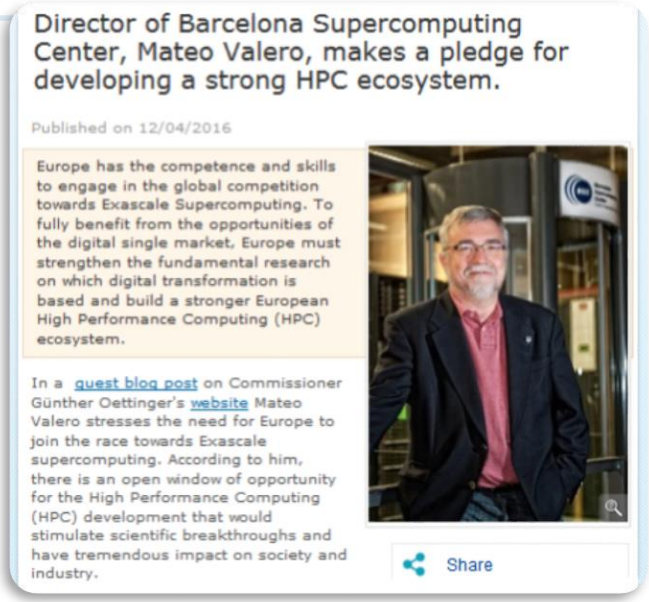
BSC and the EC

Final plenary panel at ICT - Innovate, Connect, Transform conference, 22 October 2015 Lisbon, Portugal.

the transformational impact of excellent science in research and innovation

"Europe needs to develop an entire domestic exascale stack from the processor all the way to the system and application software"

Mateo Valero, Director of Barcelona Supercomputing Center



Director of Barcelona Supercomputing Center, Mateo Valero, makes a pledge for developing a strong HPC ecosystem.

Published on 12/04/2016

Europe has the competence and skills to engage in the global competition towards Exascale Supercomputing. To fully benefit from the opportunities of the digital single market, Europe must strengthen the fundamental research on which digital transformation is based and build a stronger European High Performance Computing (HPC) ecosystem.

In a guest blog post on Commissioner Günther Oettinger's website Mateo Valero stresses the need for Europe to join the race towards Exascale supercomputing. According to him, there is an open window of opportunity for the High Performance Computing (HPC) development that would stimulate scientific breakthroughs and have tremendous impact on society and industry.

Share

The European Commission and HPC

European Commission President
Jean-Claude Juncker

"Our ambition is for Europe to become one of the top 3 world leaders in high-performance computing by 2020"

Paris, October 2015

European Commission President
Ursula von der Leyen

"There is no digital without chips.
We will present a new European Chips Act.
The aim is to jointly create a European chip ecosystem, including production"

SOTEU, September 2021

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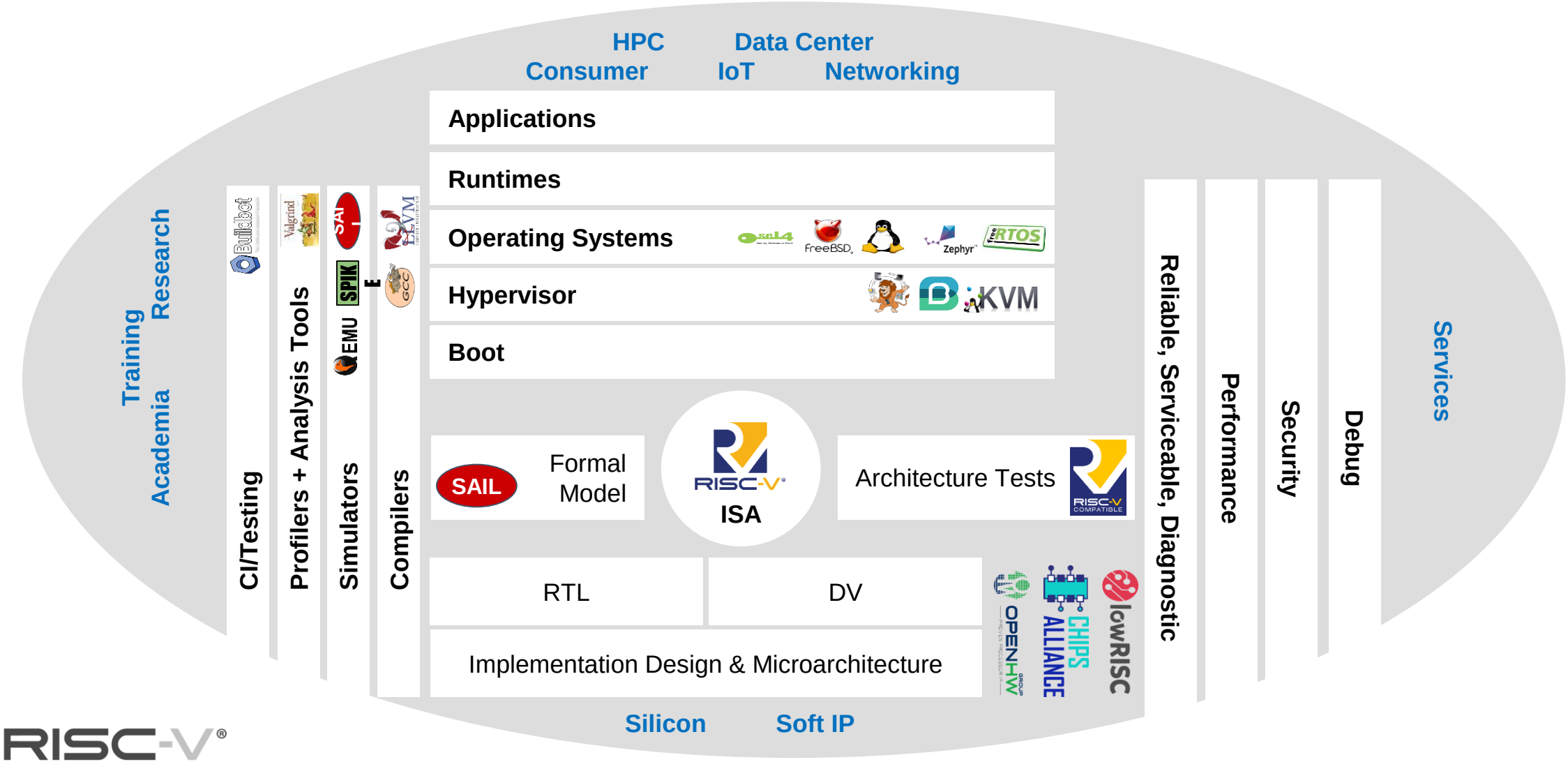
Why Open Source Hardware?

Software: Leverage a large ecosystem compatible across implementations
Security: A fully auditable collection of IPs: processors, accelerators, etc.
Safety: No black-boxes
SWaP & Customization: SW/HW co-design for exact feature match
Performance: State-of-the-art implementations
No vendor lock-in: Ecosystem to enable custom develop from SME to large enterprise
Sovereignty: Freedom of access and implementation from design to production
Open Collaboration: Faster time to market, community, leverage existing open source

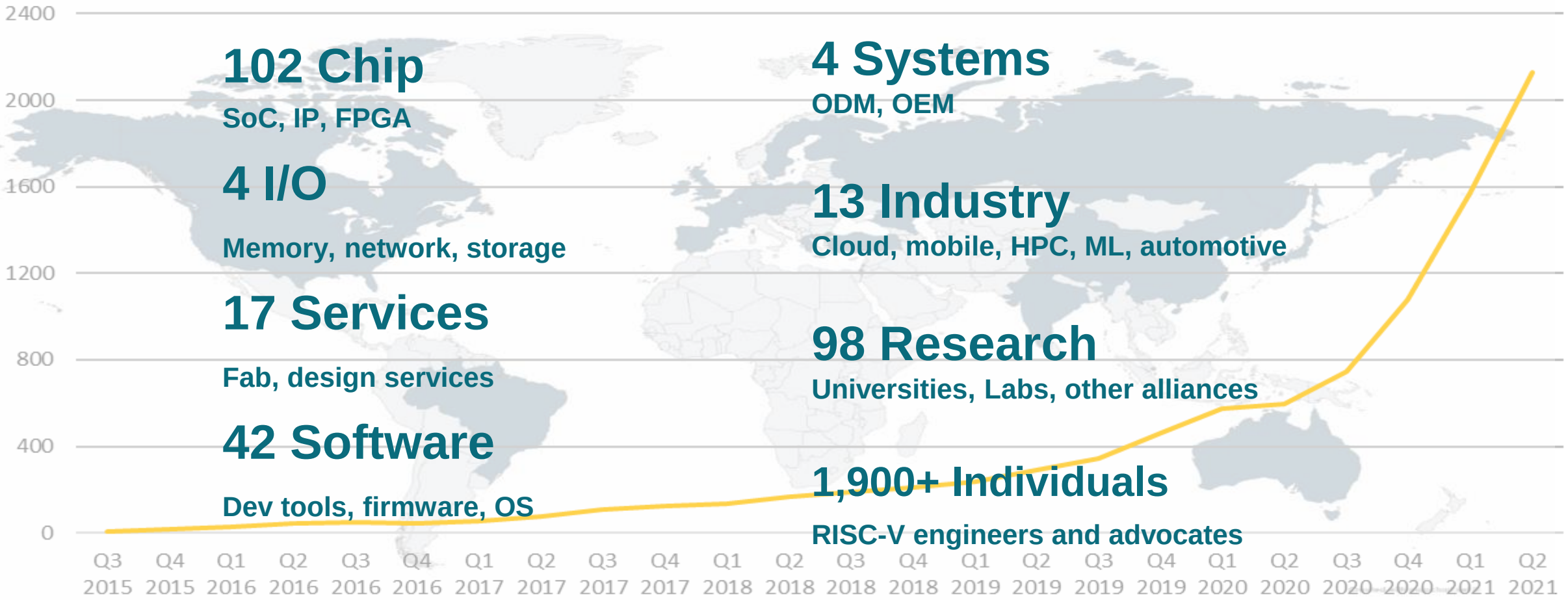
RISC-V Ecosystem



RISC-V®

More than 2,200 RISC-V Members

across 70 Countries



102 Chip

SoC, IP, FPGA

4 I/O

Memory, network, storage

17 Services

Fab, design services

42 Software

Dev tools, firmware, OS

4 Systems

ODM, OEM

13 Industry

Cloud, mobile, HPC, ML, automotive

98 Research

Universities, Labs, other alliances

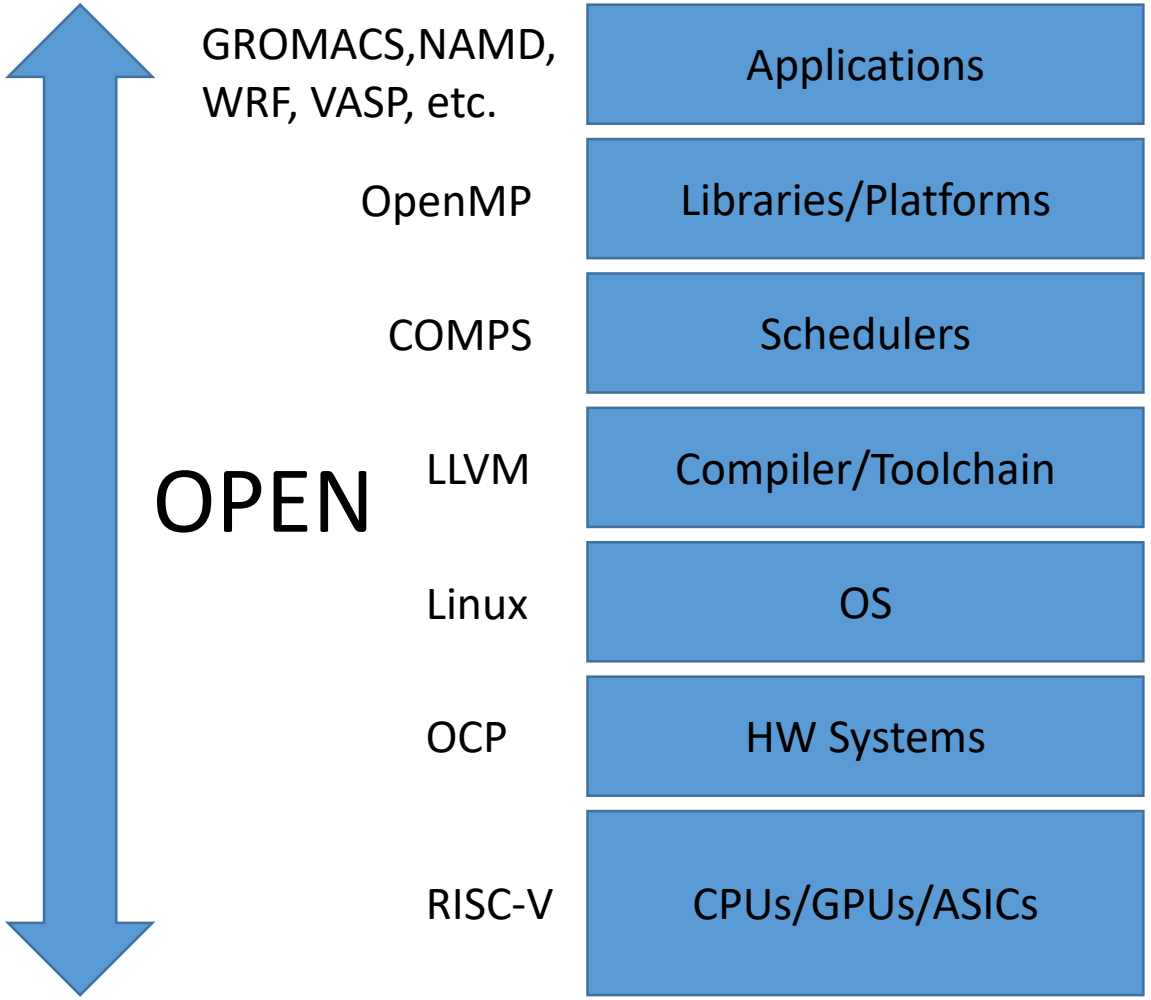
1,900+ Individuals

RISC-V engineers and advocates

RISC-V membership grew 133% in 2020.
In 2021, RISC-V membership has already doubled.

HPC Tomorrow

- Europe can lead the way to a completely **open SW/HW stack for the world**
- RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
- Europe can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- **RISC-V can unify, focus, and build a new microelectronics industry in Europe.**



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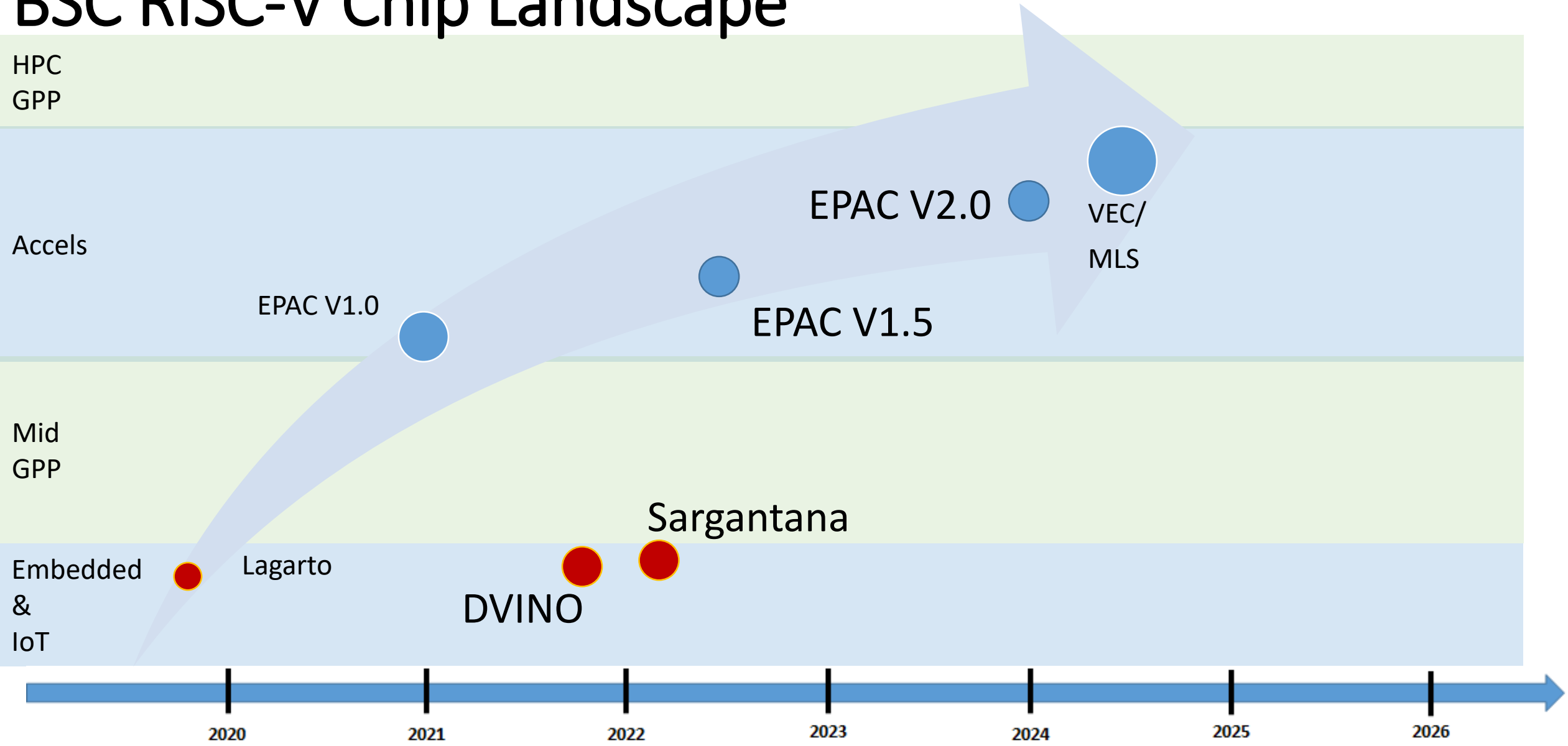
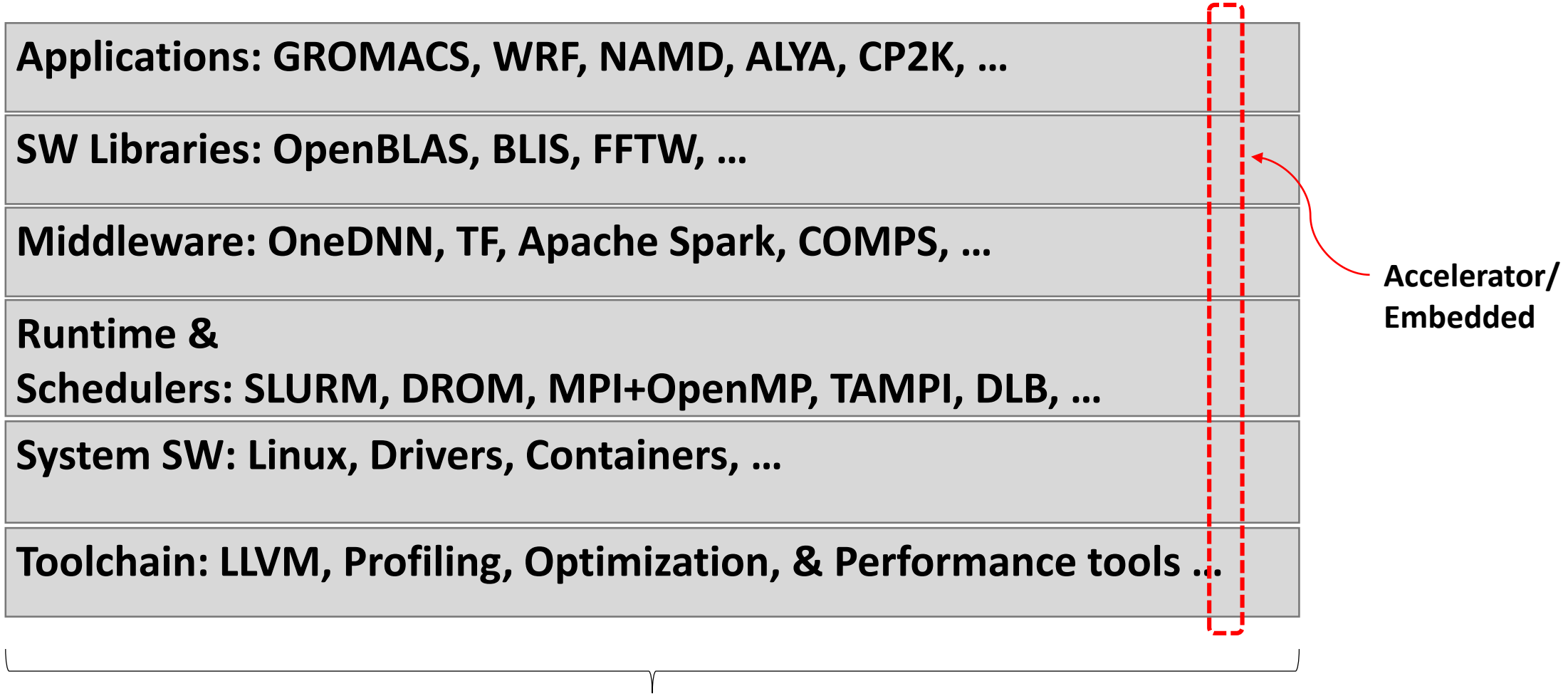
RISC-V Research in Europe

BSC RISC-V Chip Landscape



HPC Open Source Software for Open Source Hardware



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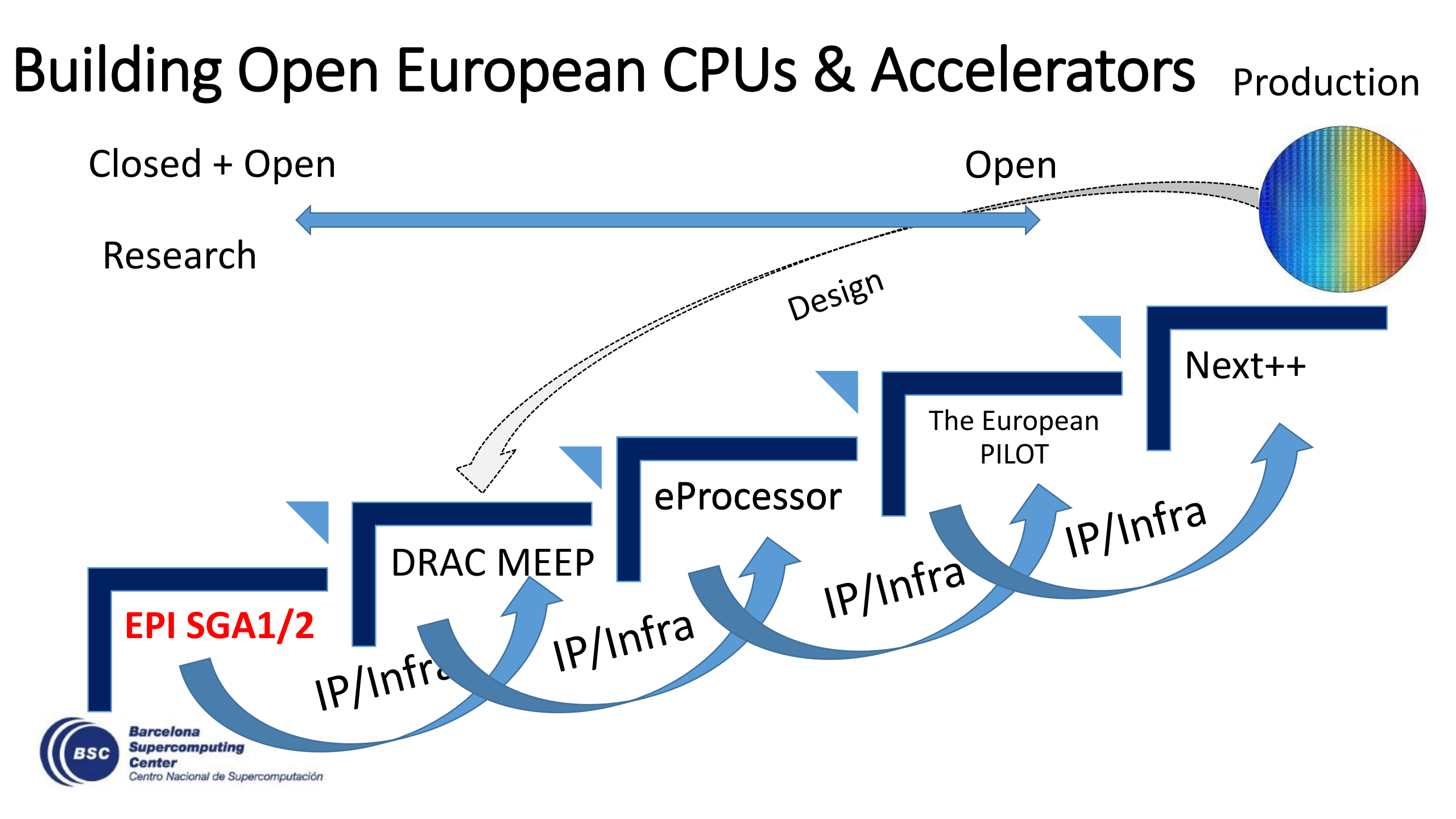
Building Open European CPUs & Accelerators



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The European Processor Initiative

The European Processor Initiative (EPI) under the SGA1 of the Framework Partnership Agreement (FPA: 800928), to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications.

- **History:** Remember MontBlanc? BSC leads the RISC-V HPC accelerator development
- **Consortium (SGA1):**

28 partners from 10 European countries to Coordinate: Bull SAS (France)

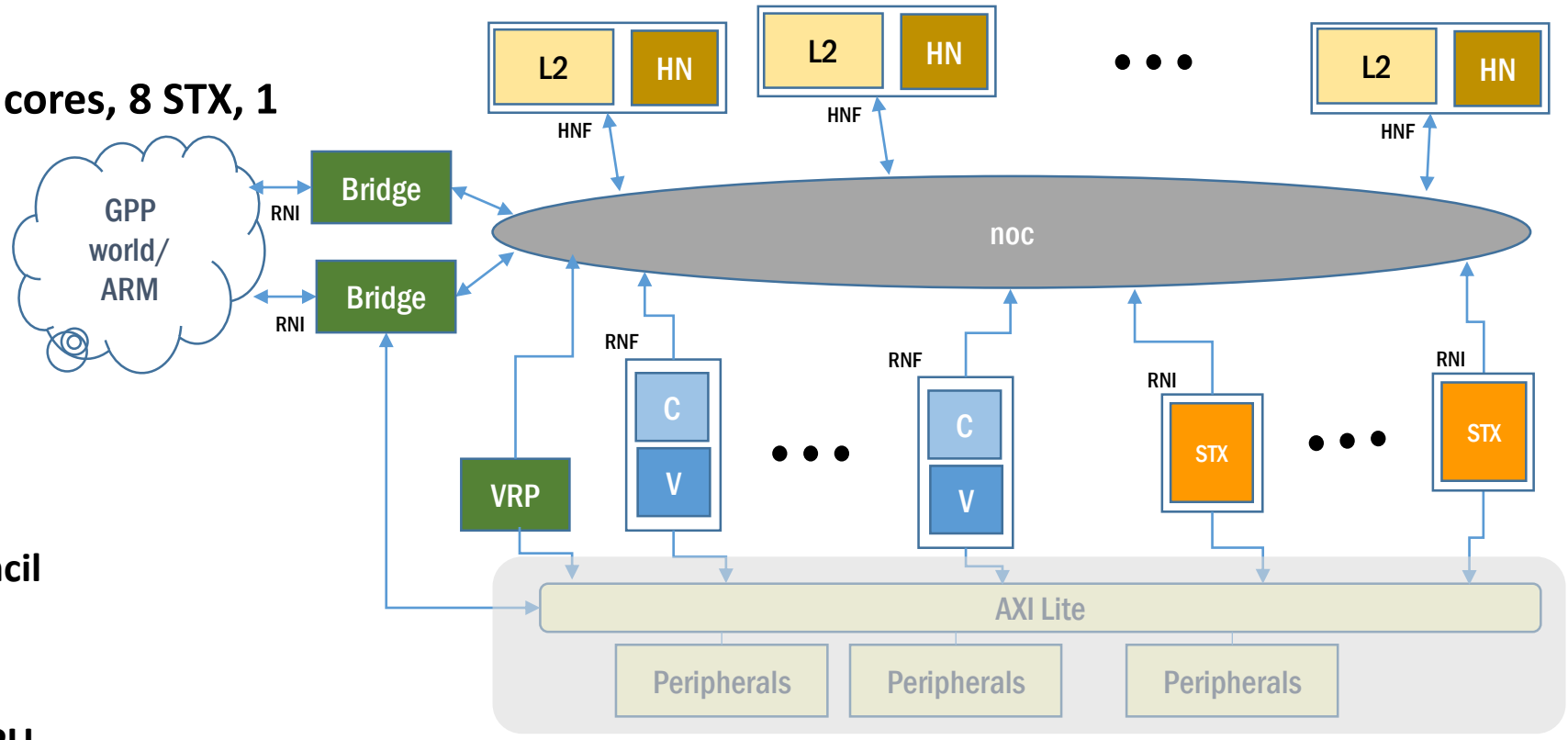
- **Budget:** €80M (100% funded)
- **Duration:** 36 months (01/12/2018-31/12/2021)
- **5 Streams** (4 Technical and 1 Management/Exploitation/C&D)

EPAC architecture

- **Objective: Develop** & demonstrate **fully European** processor IPs based on the **RISC-V ISA.** Build on existing EU IP, leverage EU background and vision
- Provide a very **low power** and high computing throughput **accelerator for HPC & Emerging -> Automotive**

Main Contributors:

- **RISC-V in the Tile: 8 Vector cores, 8 STX, 1 VRP**
- **Vector Core :**
  - **Spain + Italy + Croatia**
  - **C: RISC-V Scalar core**
  - **V: RISC-V Vector core: 8 lanes**
- **STX**
  - **Switzerland + Germany**
  - **RISC-V NTX (AI/ML/DL) + Stencil**
- **VRP**
  - **France**
  - **RISCV + Extended precision FPU**



UNIBO | IST | CEA | Chalmers | FORTH | Semidynamics | BSC +FER | ETH + FhG | EXTOLL | ETH

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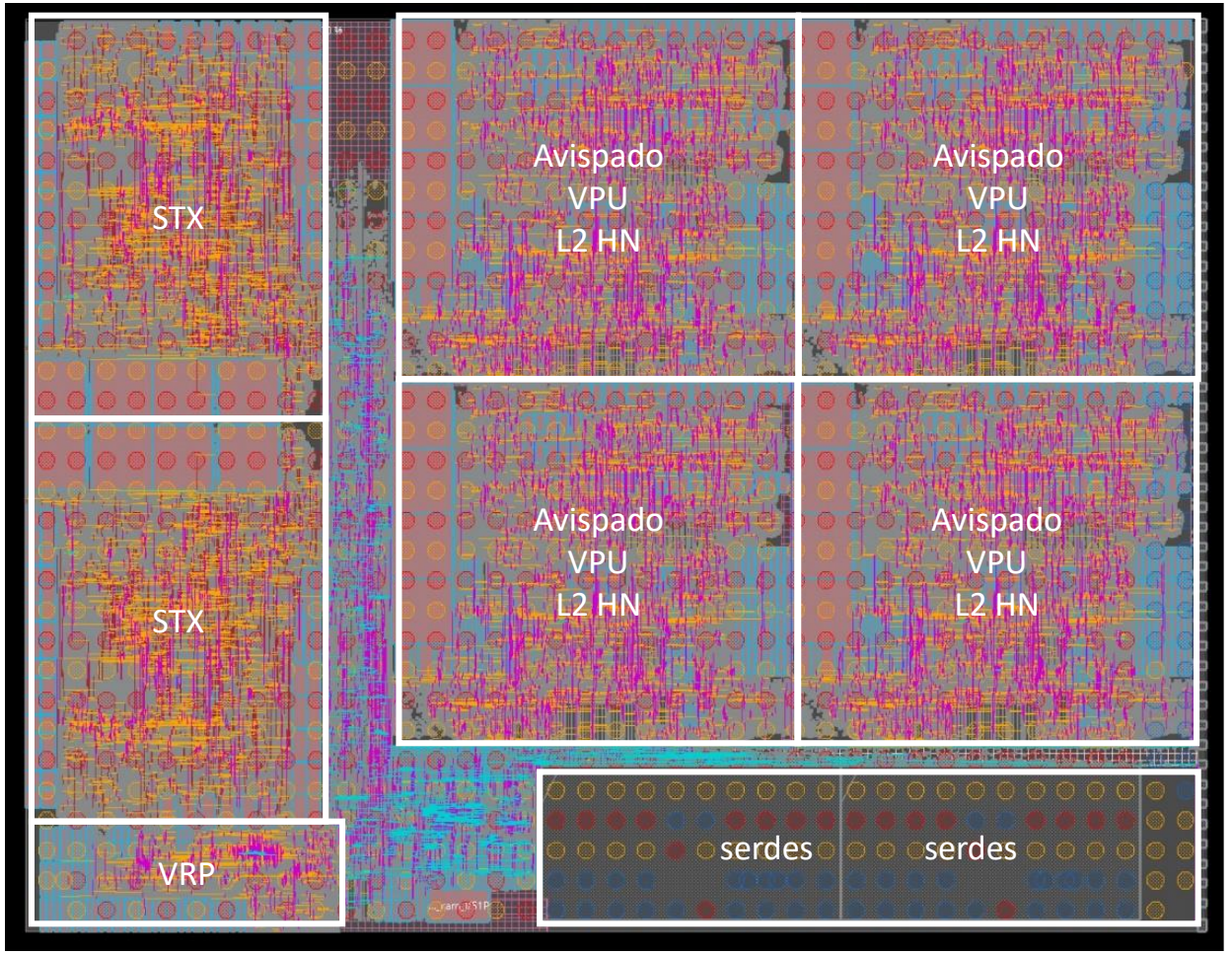
EPAC V1.0, GF22FDX

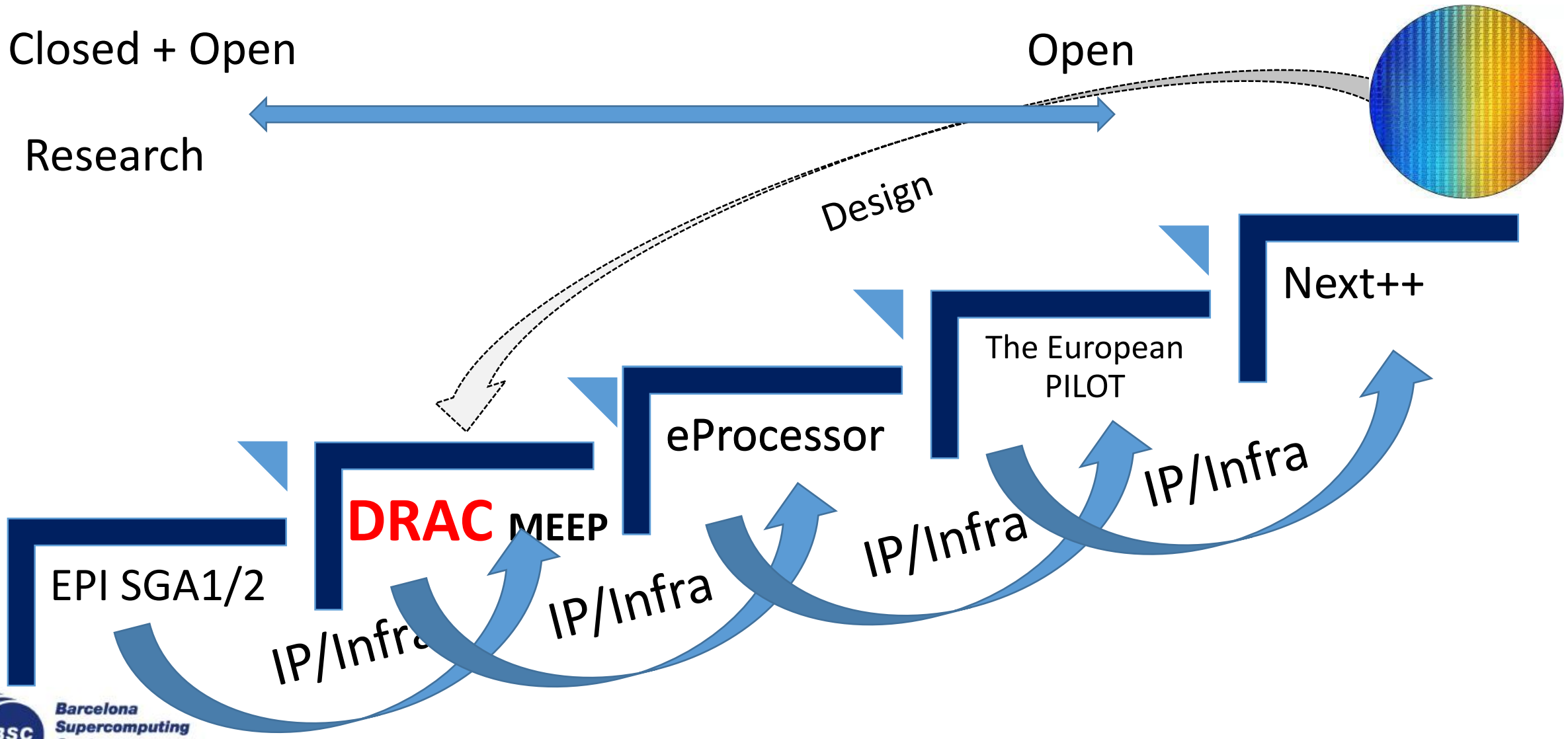
- Chip fabrication Q2 2021
- Final Top level chip floorplan
- Total area:
  - 5943 X 4593 um^2
  - (27.297 mm^2)



EPI SGA2

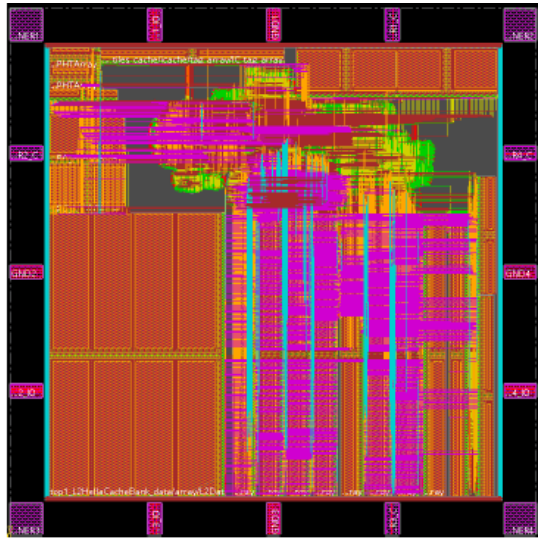
- Next generation
  - January 2022 – December 2024
  - 31 partners
  - GPP and RISC-V Accelerators
  - COMING SOON:
    - EPAC V1.5
    - EPAC V2.0

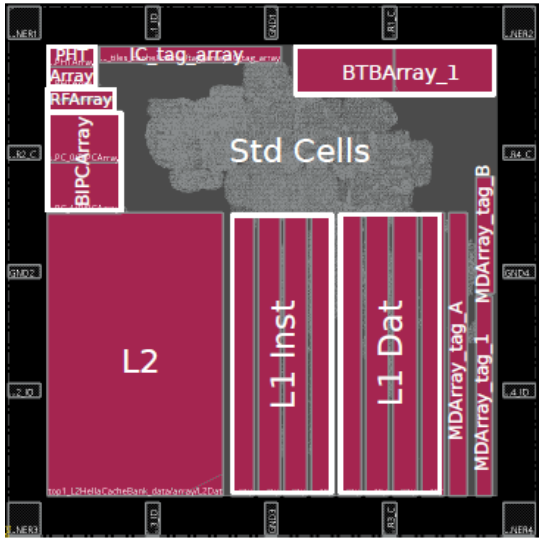
Rebuilding the European CPU Industry



Lagarto: First RISCV Tapeout (2019)

- Target design:
  - Simple in-order core with 5 stages, single issue
  - 16KB L1 caches, 64KB L2 cache, TLB
  - Memory controller on the FPGA side via packetizer
  - Debug ring via JTAG
  - Target technology: TSMC 65nm, area fits in 2.5mm2
- Fabrication and bringup
  - Submitted in May 2019
  - Samples received in Sep 2019
  - Bringup with custom PCB in Oct 2019
  - Linux boot in Dec 2019





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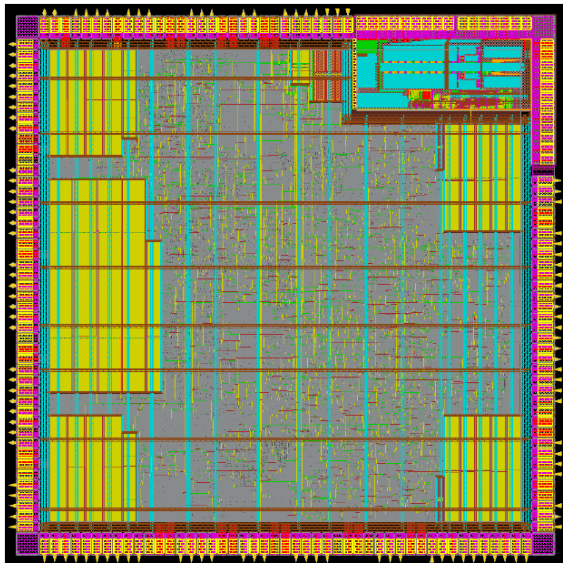
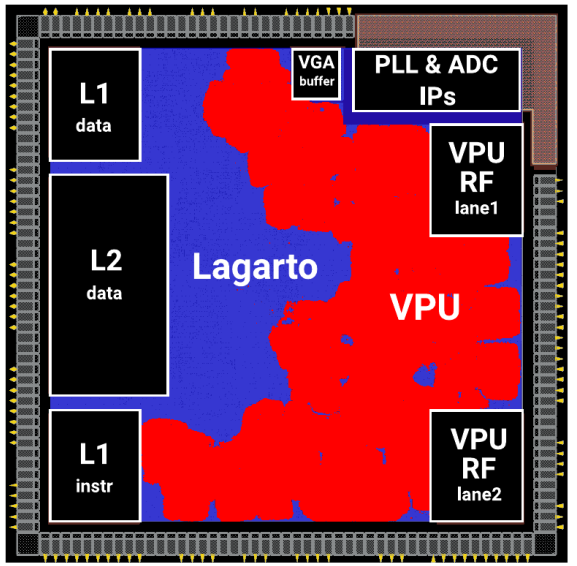
IPN

DVINO: 2nd Lagarto Tapeout (2021)

- DRAC Vector IN-Order (DVINO) processor details:
  - Lagarto M20 scalar pipeline, 5-stage, in-order, RV64IMA
  - Hydra 2-lane (VPU-DRAC-1.0), 4096-bit vector length
  - Intenal PLL. DVINO can run at 600, 400, 300 and 200MHz
  - In-house L1 instruction cache and PMU
  - L1 data and L2 caches from lowRISC 0.2
  - Multiple contr: JTAG, UART, SPI, VGA, SDRAM and Hyperram.
  - In-house JTAG-based debug-ring
  - Technology node: TSMC 65nm (Europractice)
  - Area: 8.6mm2





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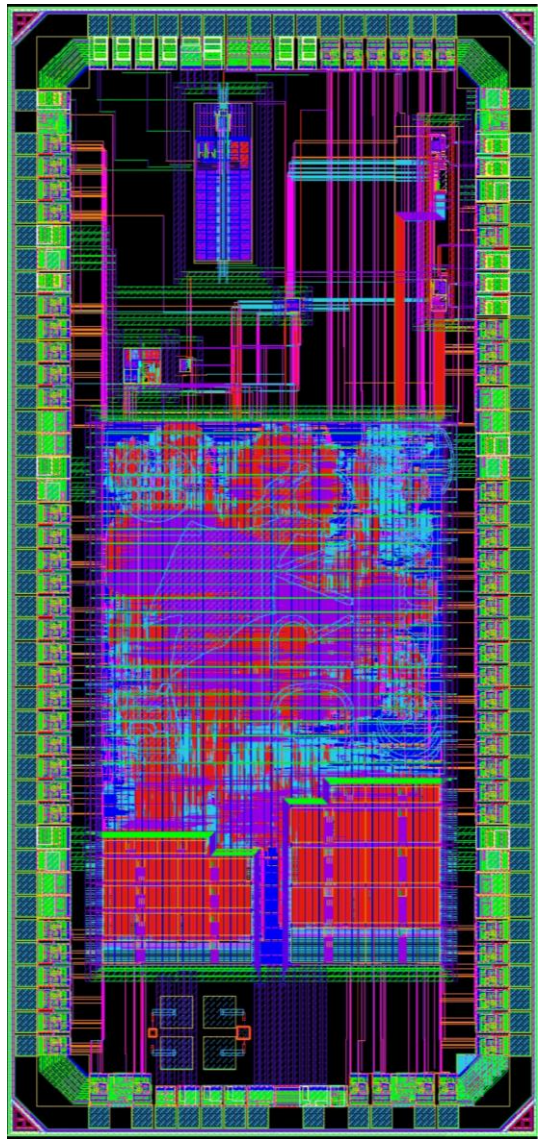
IPN

Sargantana Tapeout (Feb 2022)

- Sargantana in-order processor details:
  - Lagarto Hun pipeline, 7-stage, in-order, RV64IMAFD (RV64G)
  - Support for floating point operations (single and double precision)
  - Integer SIMD VPU, 128-bit vector length, custom instructions
  - Internal PLL. Sargantana can run above 1.3GHz
  - Multiple controllers: JTAG, UART, SPI, SerDes, and Hyperram
  - In-house L1 instruction cache and PMU
  - L1 data and L2 caches from lowRISC 0.2
  - In-house JTAG-based debug-ring
  - Technology node: GF 22nm (Europractice)
  - Area: 2.9mm2



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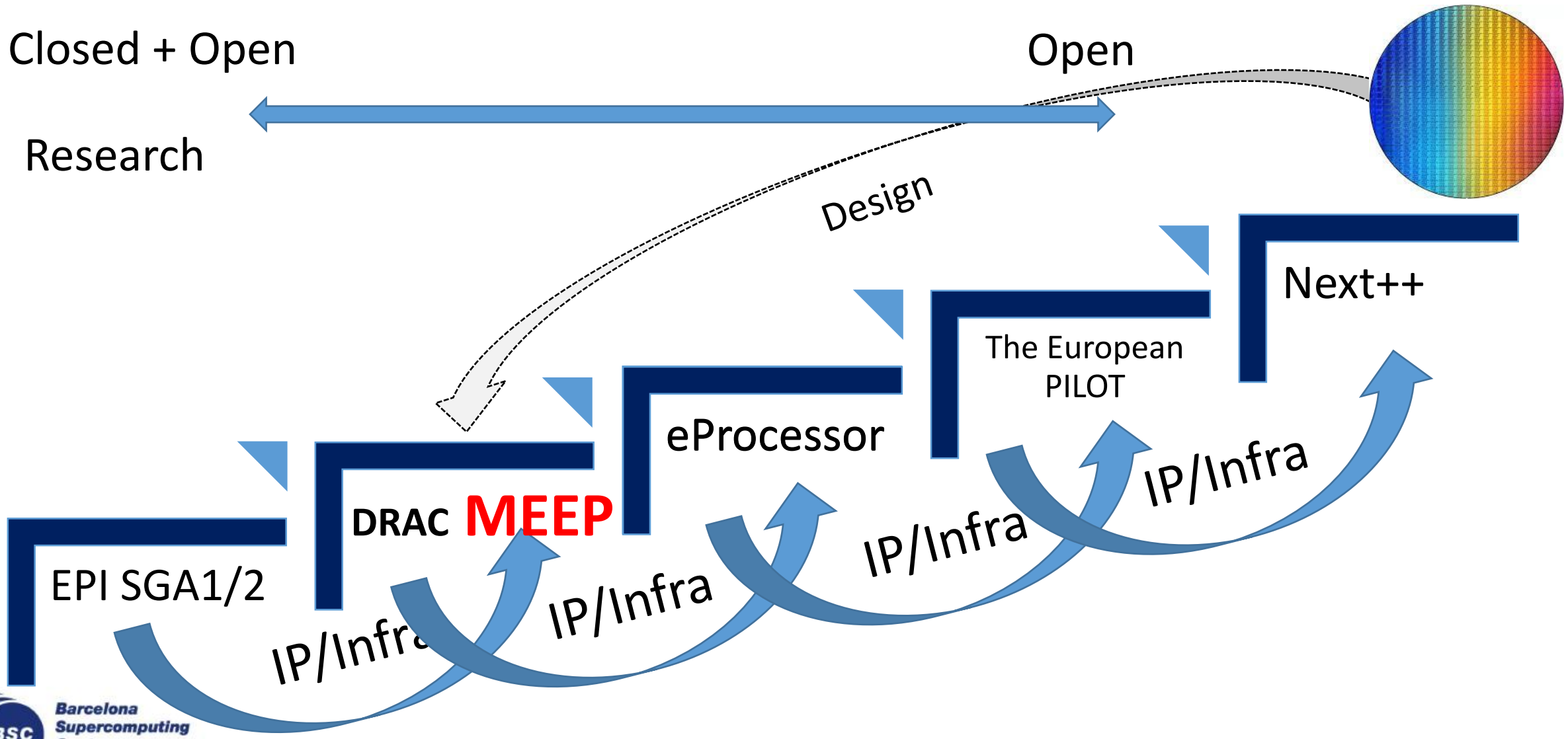
UAB Universitat Autònoma de Barcelona

UNIVERSITAT ROVIRA i VIRGILI

Rebuilding the European CPU Industry



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MEEP: MareNostrum Experiment Exascale Platform

MEEP is a flexible FPGA-based emulation platform that will explore hardware/software co-designs for Exascale Supercomputers and other hardware targets, based on European-developed IP. The project provides two functions:

An evaluation platform of pre-silicon IP and ideas, at speed and scale.

A software development and experimentation platform to enable software readiness for new hardware.

MEEP

MareNostrum Experimental Exascale Platform

The MEEP project has received funding from the European High-Performance Computing Joint Undertaking Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Croatia, Turkey.

MEEP will enable software development, accelerating software maturity, compared to the limitations of software simulation. IP can be tested and validated before moving to silicon, saving time and money.

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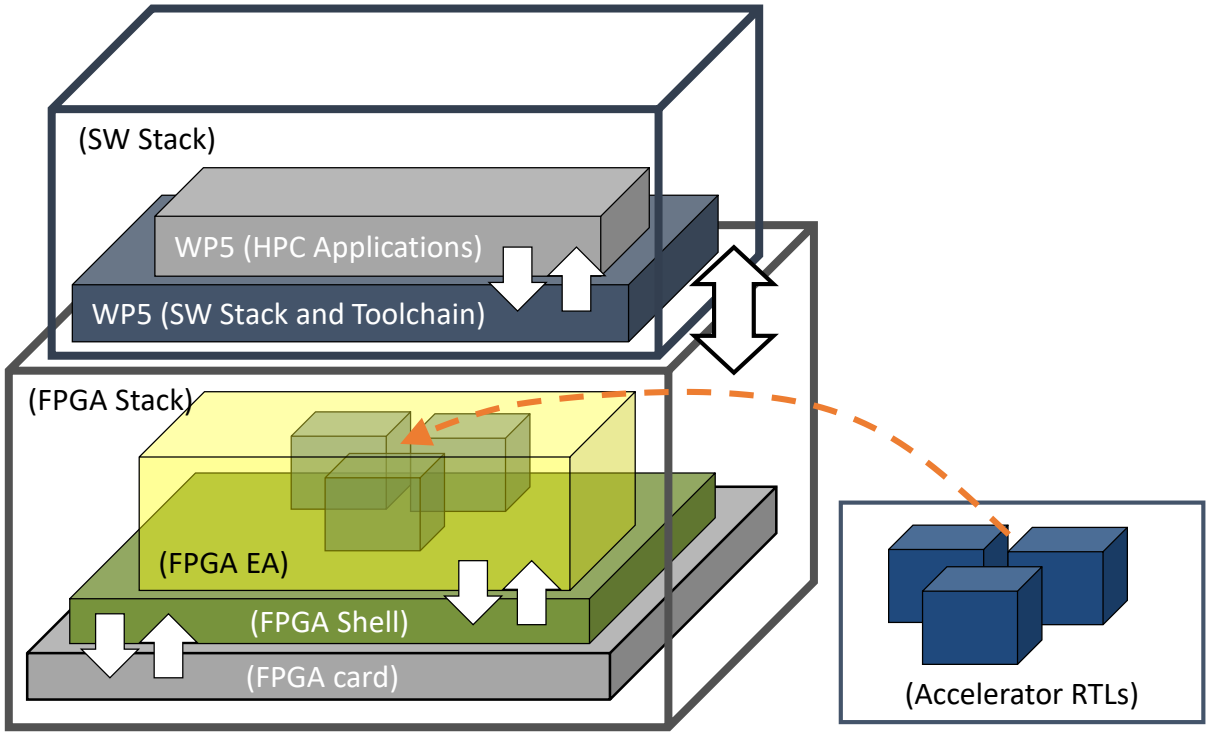
Faculty of Electrical Engineering and Computing

BİLGEM

Technical structure



Co-design laboratory

SW Stack
- HPC & HPDA apps
- Compiler, Virtualization
- Runtimes, OS

IP design (ACME)
- Design
- Development
- Verification

HW Stack
- Platform
- FPGA Shell
- EA Implementation

Pre-silicon Validation

SDV

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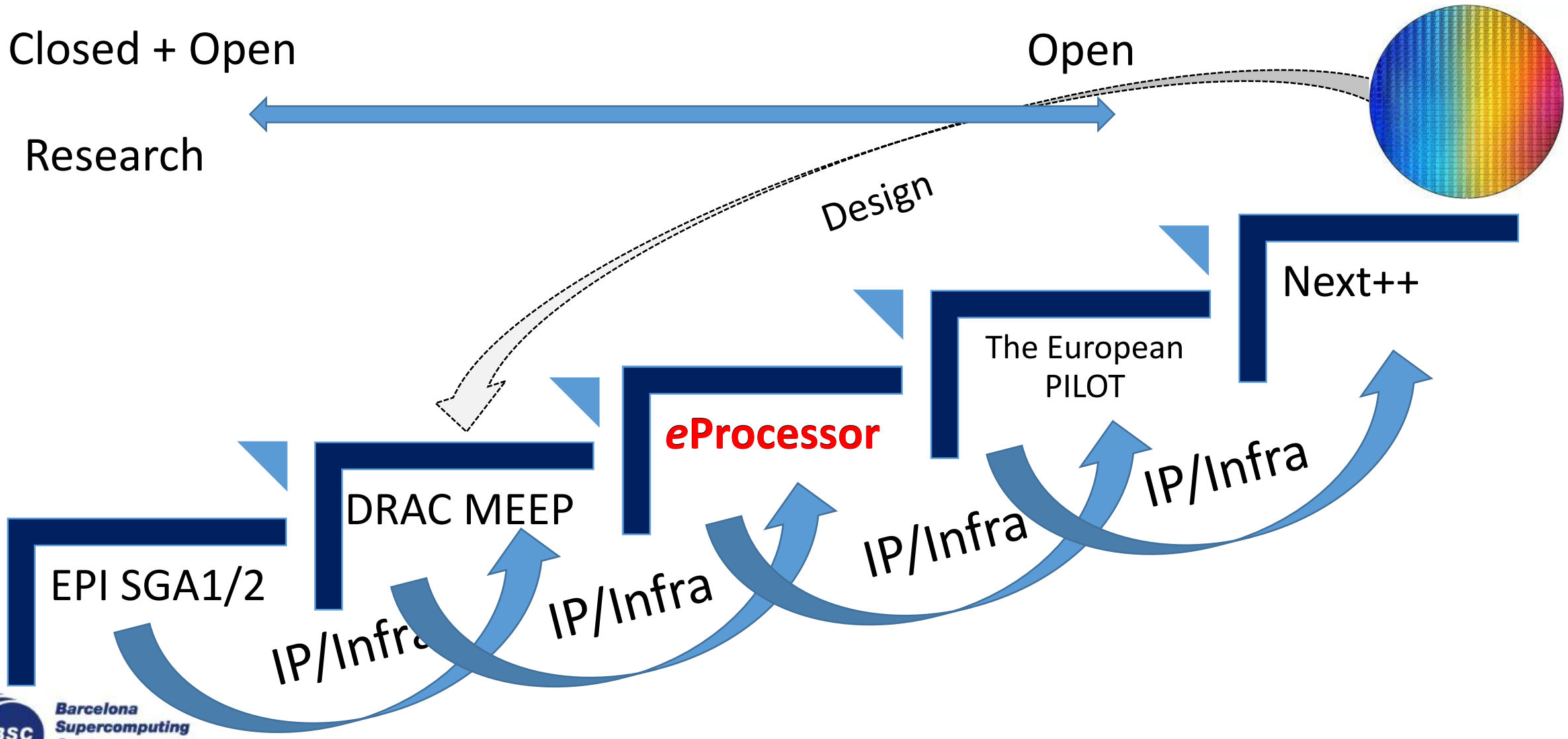
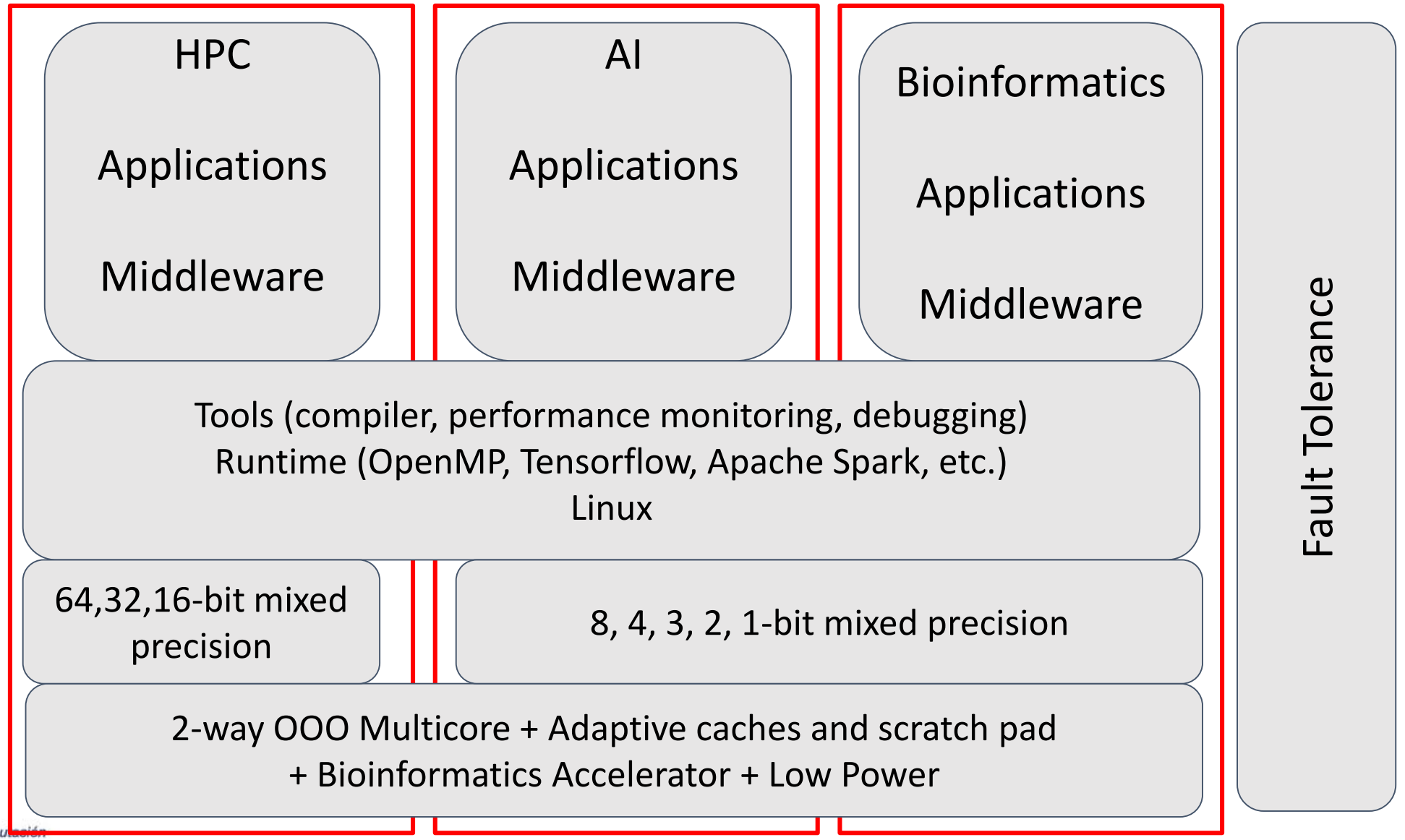
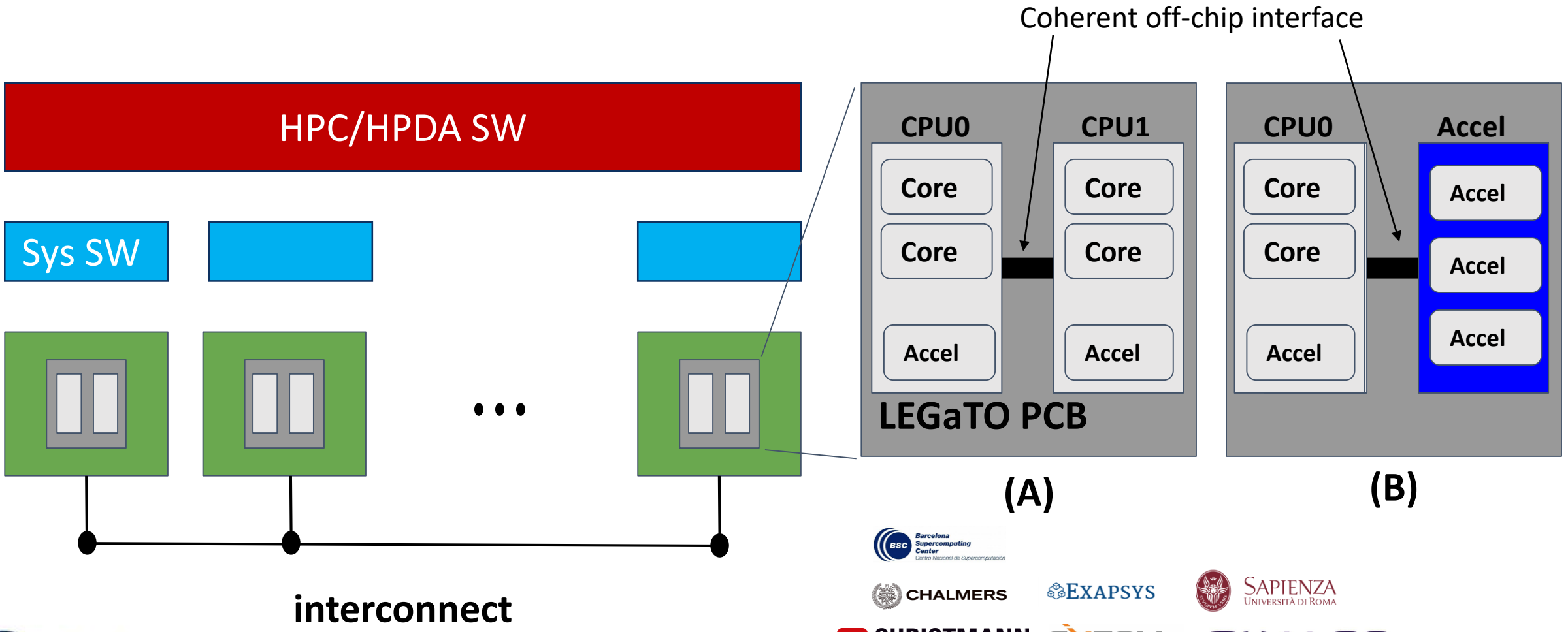


*e*Processor Stack



eProcessor System diagram



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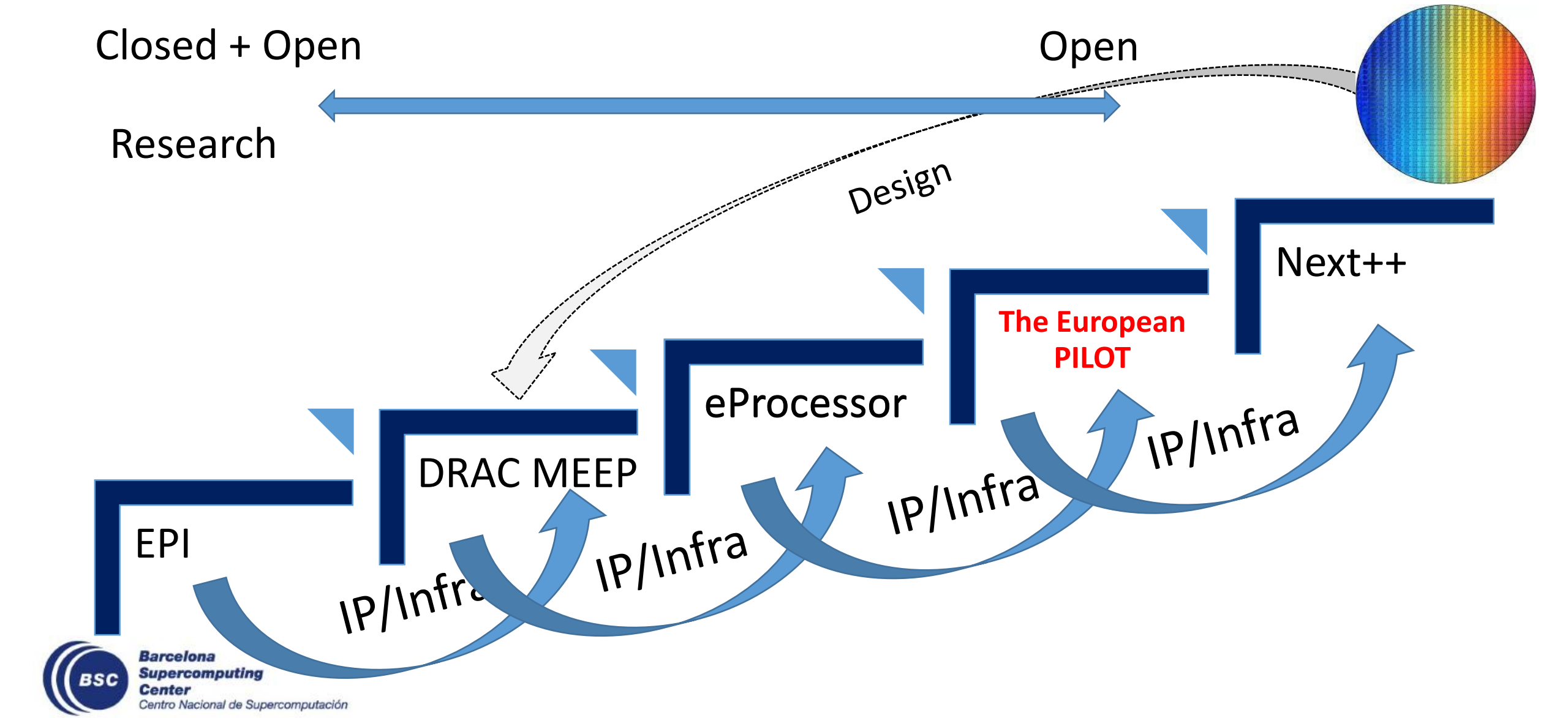
CHRISTMANN INFORMATIONSTECHNIK + MEDIEN · EXTOLL · THALES RESEARCH & TECHNOLOGY
cortus · FORTH INSTITUTE OF COMPUTER SCIENCE · UNIVERSITÄT BIELEFELD

Rebuilding the European CPU Industry



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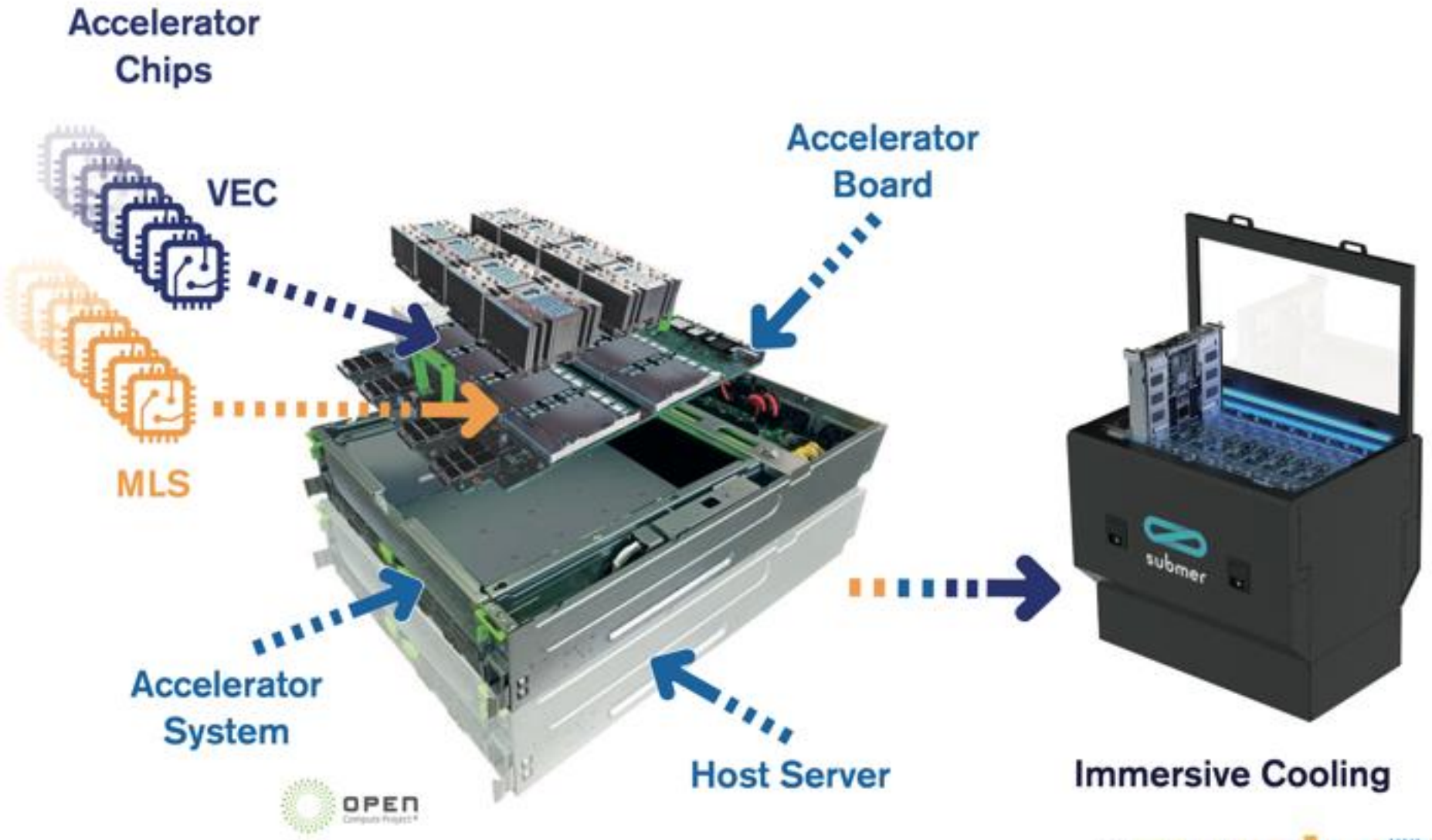
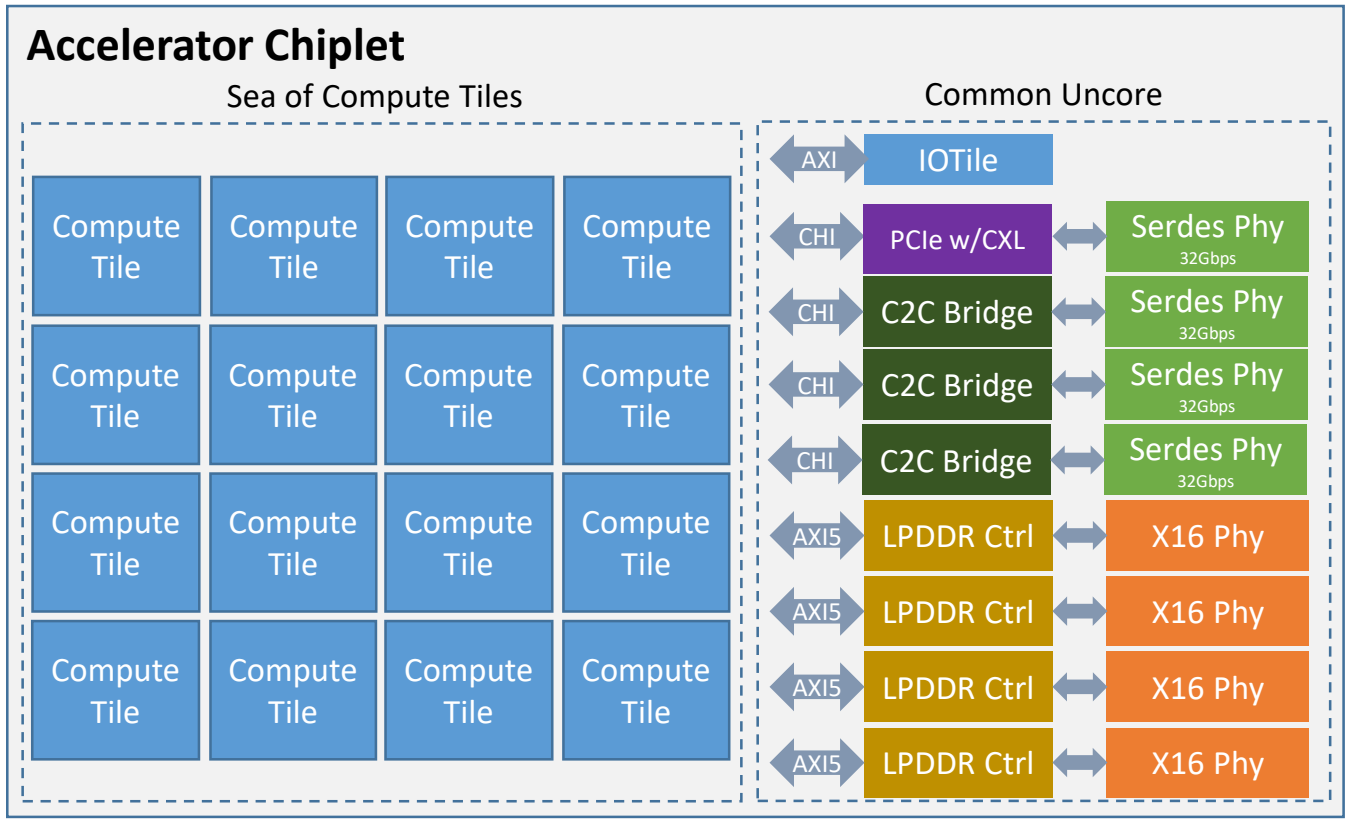
The EUPILOT at a Glance

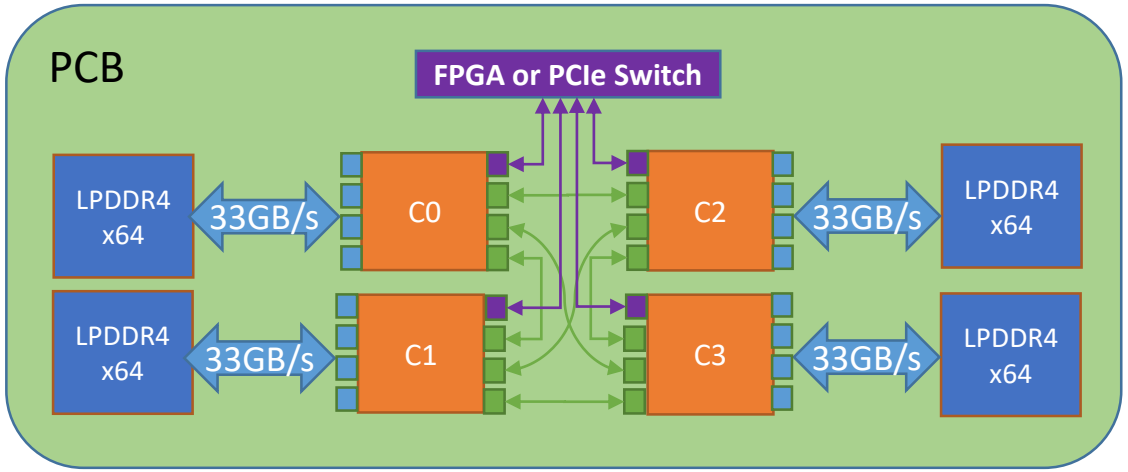
- Design, build, and validate the first EU-based pre-exascale accelerator system for HPC and ML/AI
- Maximal use of technologies with European assets, end-to-end
- Stimulate European collaboration in HPC
- Use Open Source technologies for HPC in software, systems and hardware, e.g RISC-V, Open Compute, ..
- HW/SW Co-design for greater performance and efficiency
- Three streams: Software, Hardware, Systems
- 19 Partners

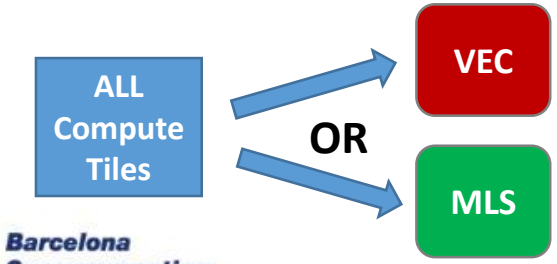
System Overview



The European PILOT Accelerator Architecture







- Accelerator Card
  - 3 C2C interfaces per chiplet, 8 lanes each
  - 1 PCIe 6.0 w/ CXL 3.0 interface per chiplet, 4 lanes
  - 4 x16 LPDDR controllers per chiplet
  - Homogeneous or Heterogeneous PCB
  - Optional FPGA/PCIe Switch

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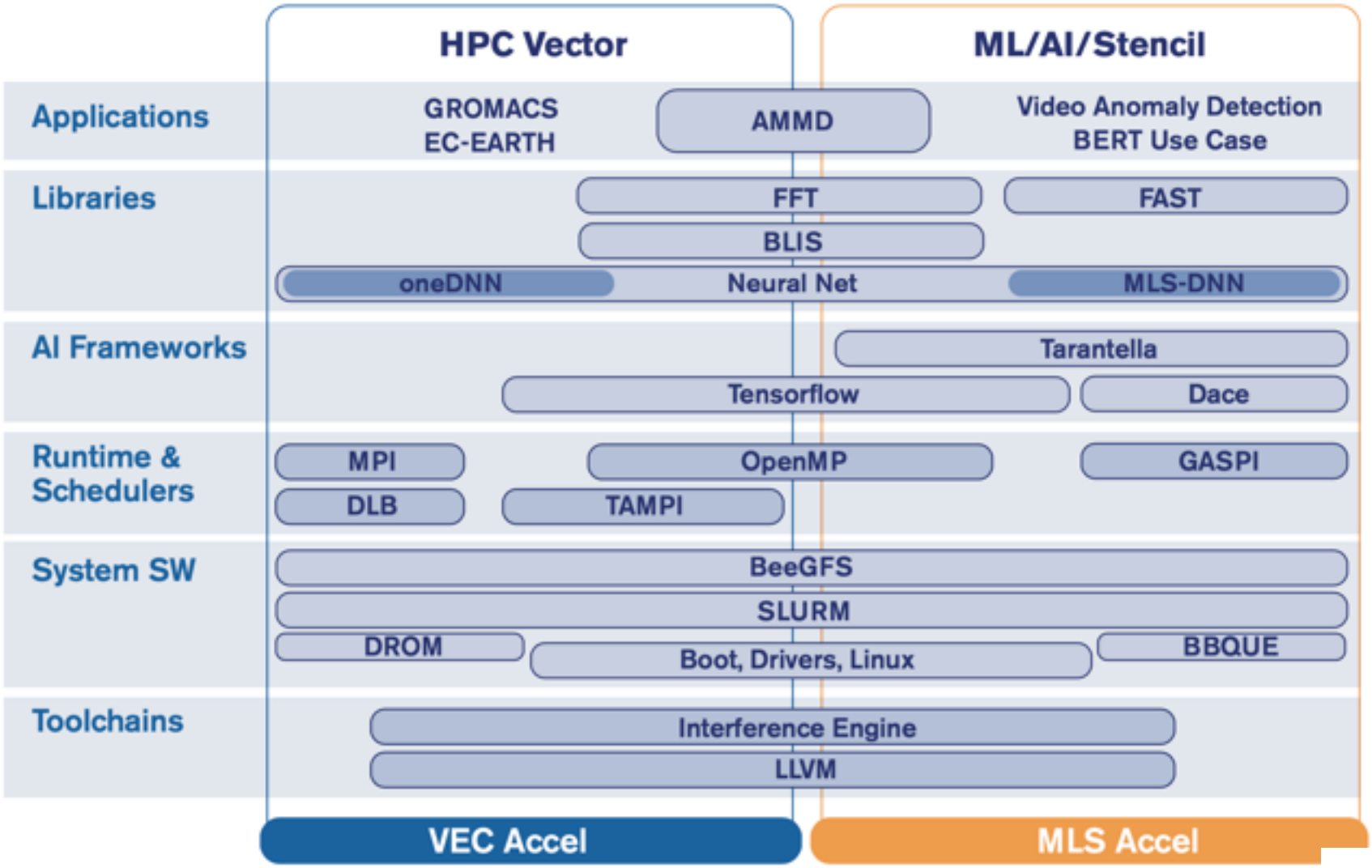
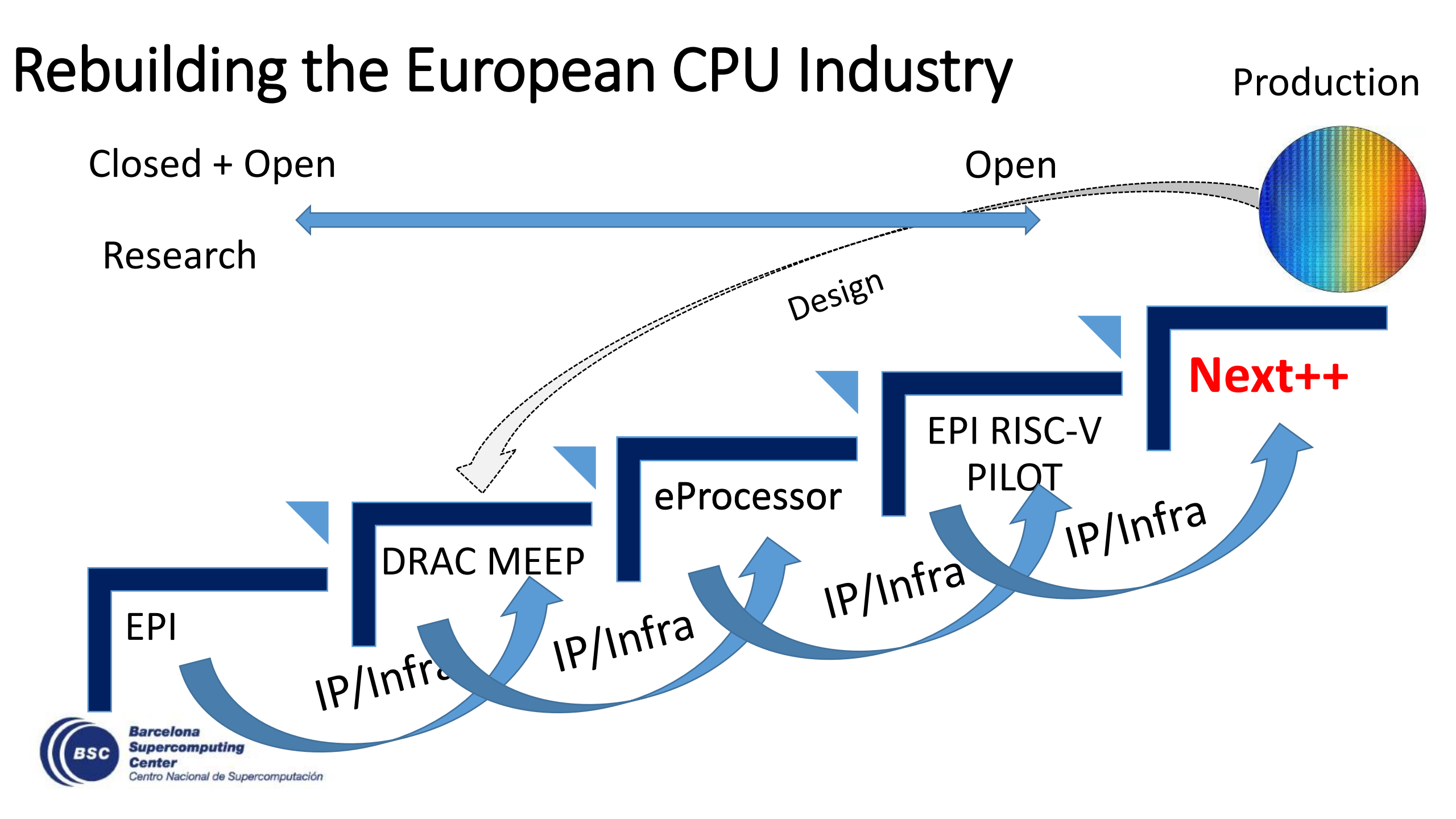
ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

THE EUPILOT

Software Stack



Rebuilding the European CPU Industry



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Recap: RISC-V in RESEARCH

- 2019: What is Open Source Hardware??
- 2020: Open Source Hardware
- 2021: RISC-V? Roadmap?
  - November roadmap report
  - Horizon Europe Work Programme 2021-22:
    - Open Source Hardware (OSH) appears 6 times
    - CSA Roadmap
- 2022: Build RISC-V!!!
  - KDT JU Work Programme 2021 v13:
    - **RISC-V appears 25 times**
    - OSH appears 2 times
- **More to come!**

Thank you

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