



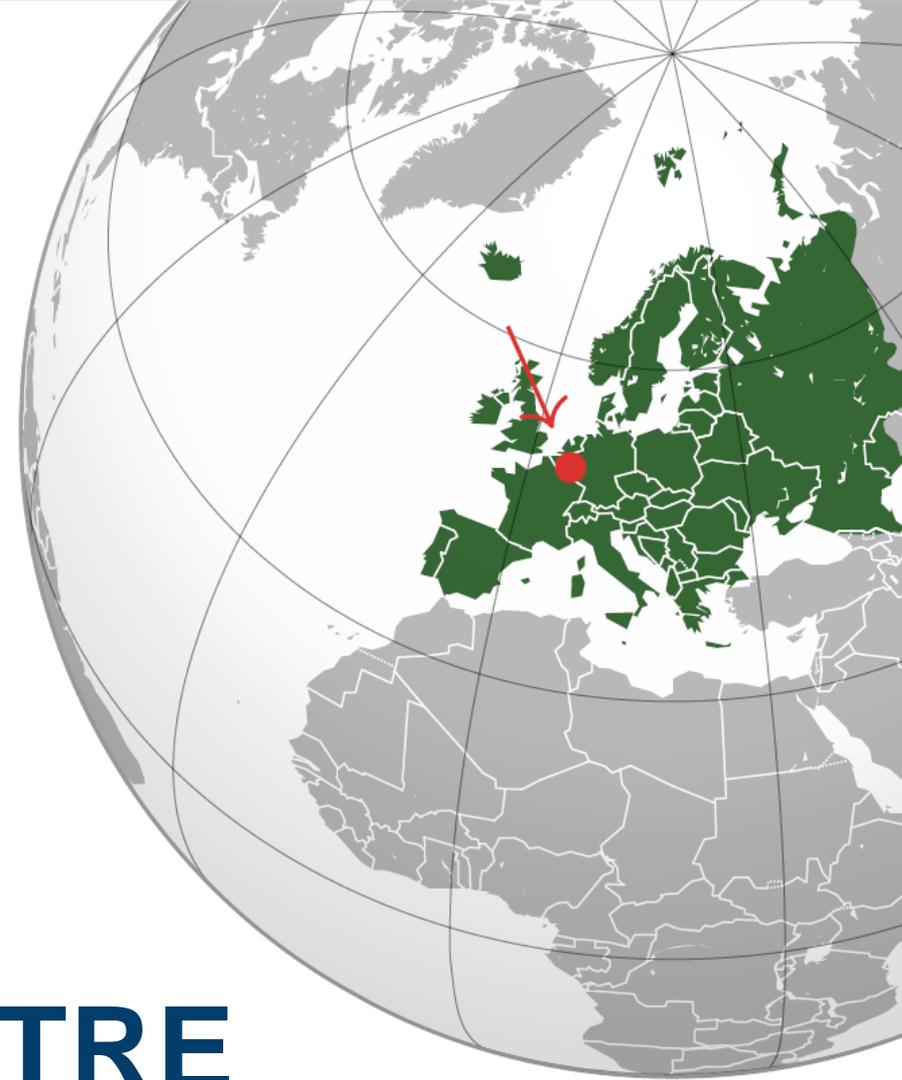
# The European Roadmap Towards HPC – From the Scientific (JSC) Perspective

SEP 22, 2021 | BERND MOHR

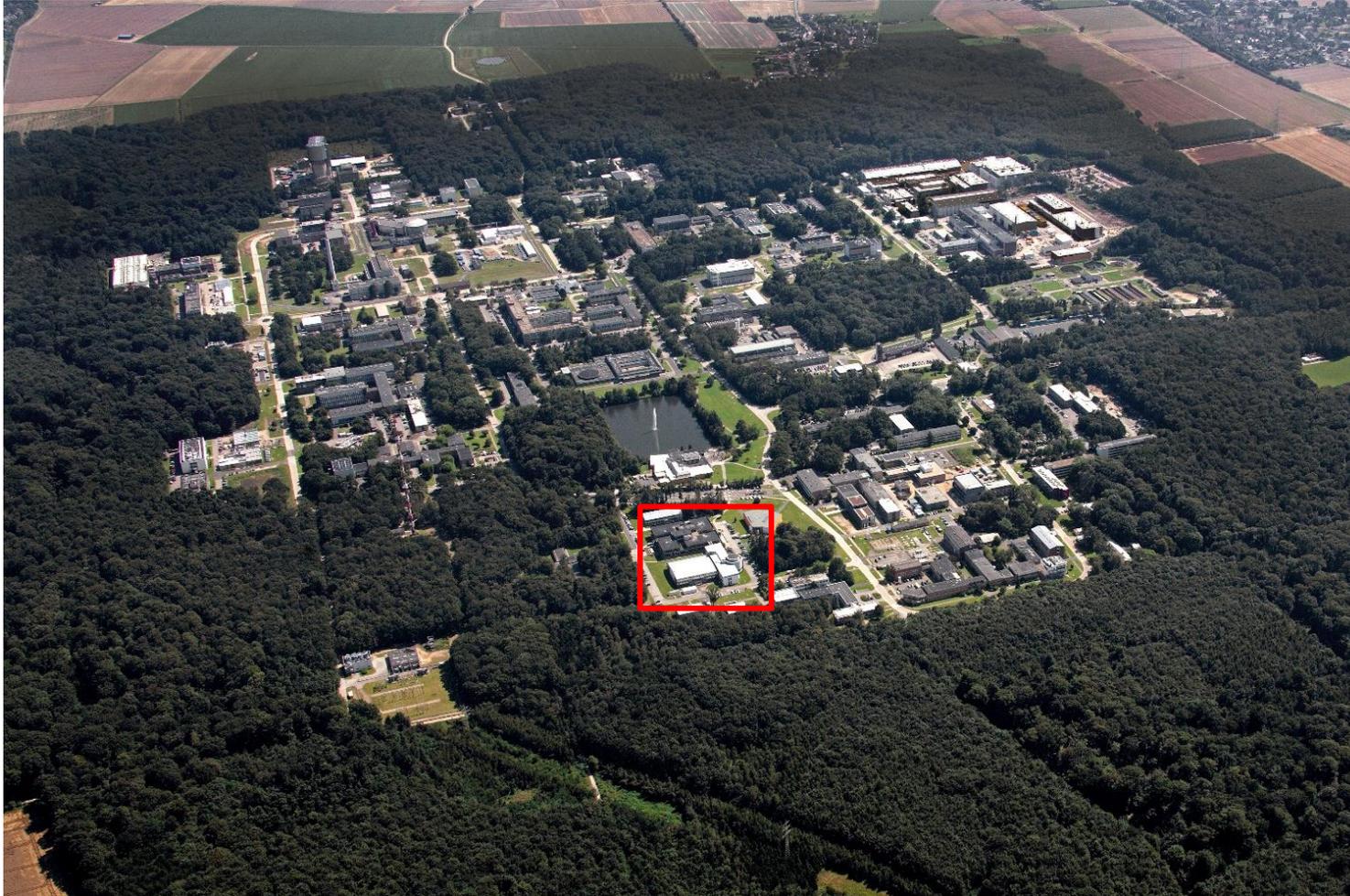
Forschungszentrum Jülich GmbH

**JÜLICH**

**SUPERCOMPUTING CENTRE**



# FORSCHUNGSZENTRUM JÜLICH GMBH



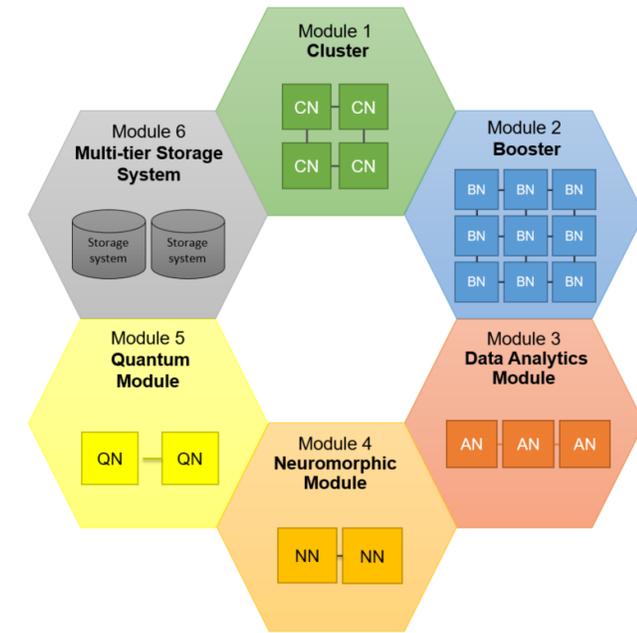
- Germany's largest national laboratory
- About 6400 employees
- Research areas
  - Information technology
  - Health (Neuroscience / brain research)
  - Energy
  - Atmosphere + Climate

# JÜLICH SUPERCOMPUTING CENTRE (JSC)



## HPC Centre for

- Forschungszentrum Jülich
- Jülich Aachen Research Alliance (JARA)
- Germany as GCS (1 of 3 German National Centres)
- Europe (1<sup>st</sup> European Centre inside PRACE)



# JSC Contribution to the European HPC Present and Future

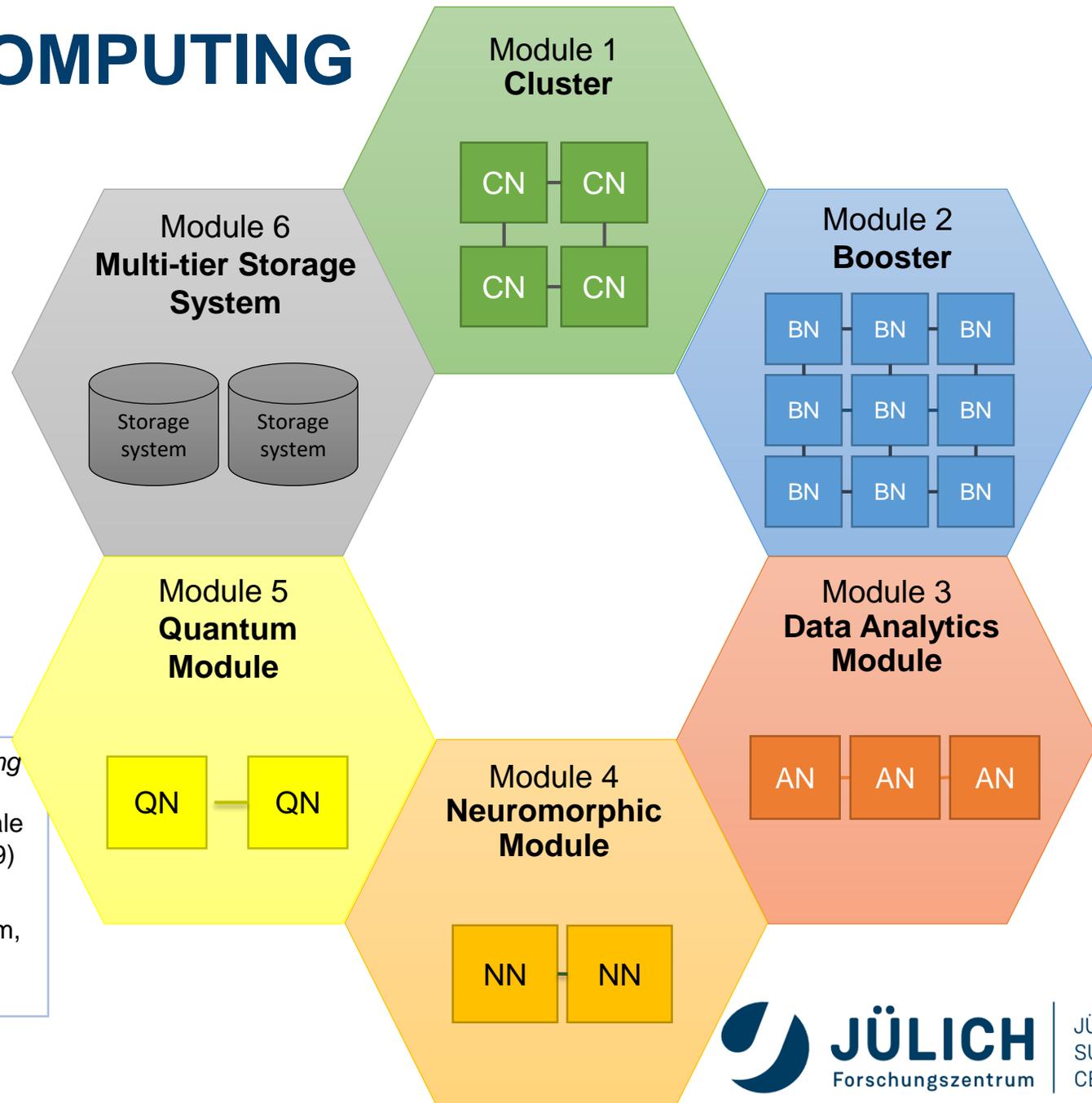
# **MODULAR SUPERCOMPUTING**

# **ARCHITECTURE (MSA)**

# MODULAR SUPERCOMPUTING

## Composability of heterogeneous resources

- Cost-efficient scaling
- Effective resource-sharing

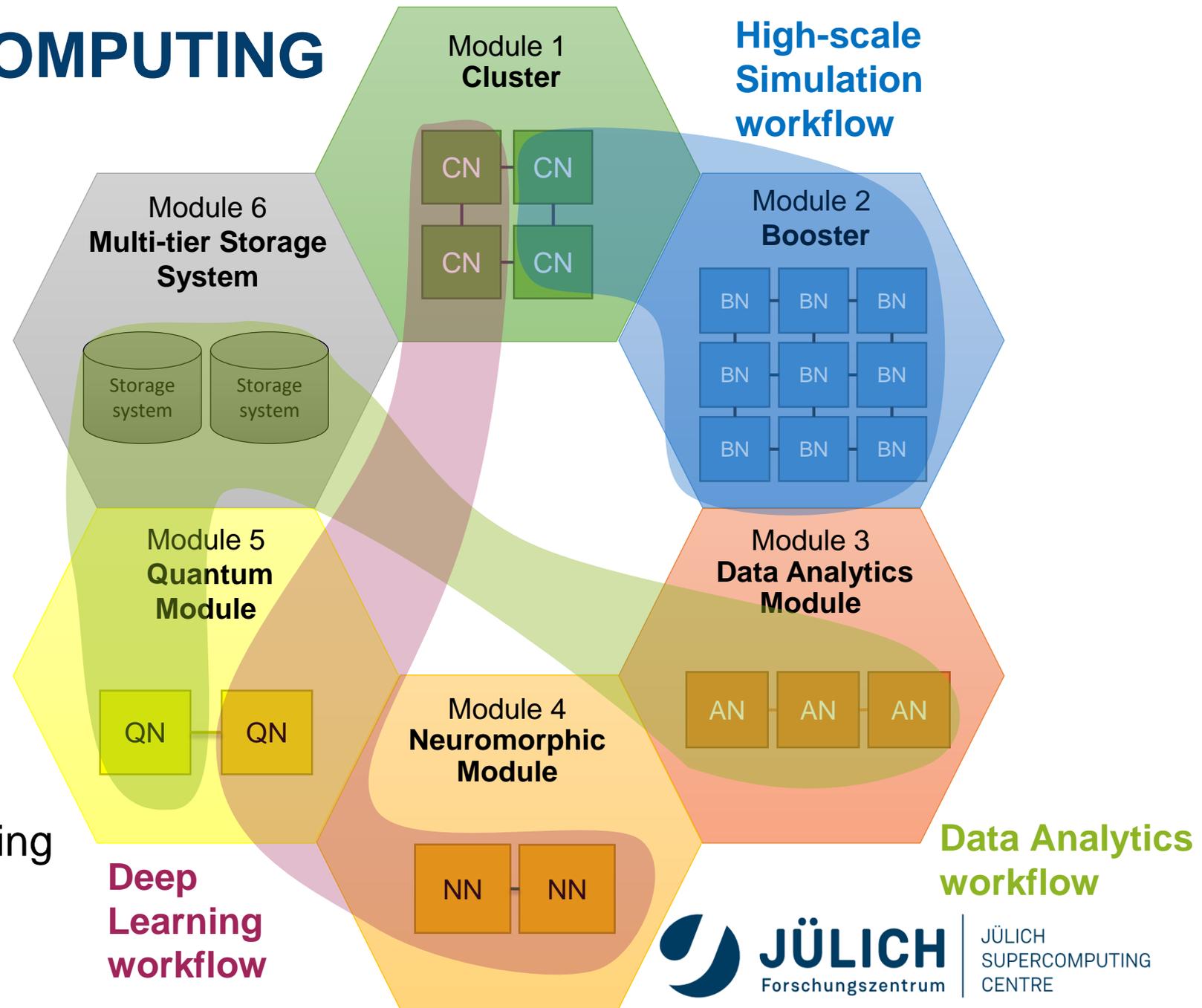


- **E. Suarez\***, N. Eicker, Th. Lippert, "*Modular Supercomputing Architecture: from idea to production*", Chapter 9 in *Contemporary High Performance Computing: from Petascale toward Exascale*, Volume 3, pp 223-251, CRC Press. (2019)
- **E. Suarez\***, N. Eicker, and Th. Lippert, "Supercomputer Evolution at JSC", *Proceedings of the 2018 NIC Symposium*, Vol.49, p.1-12, (2018) [online: <http://juser.fz-juelich.de/record/844072>].

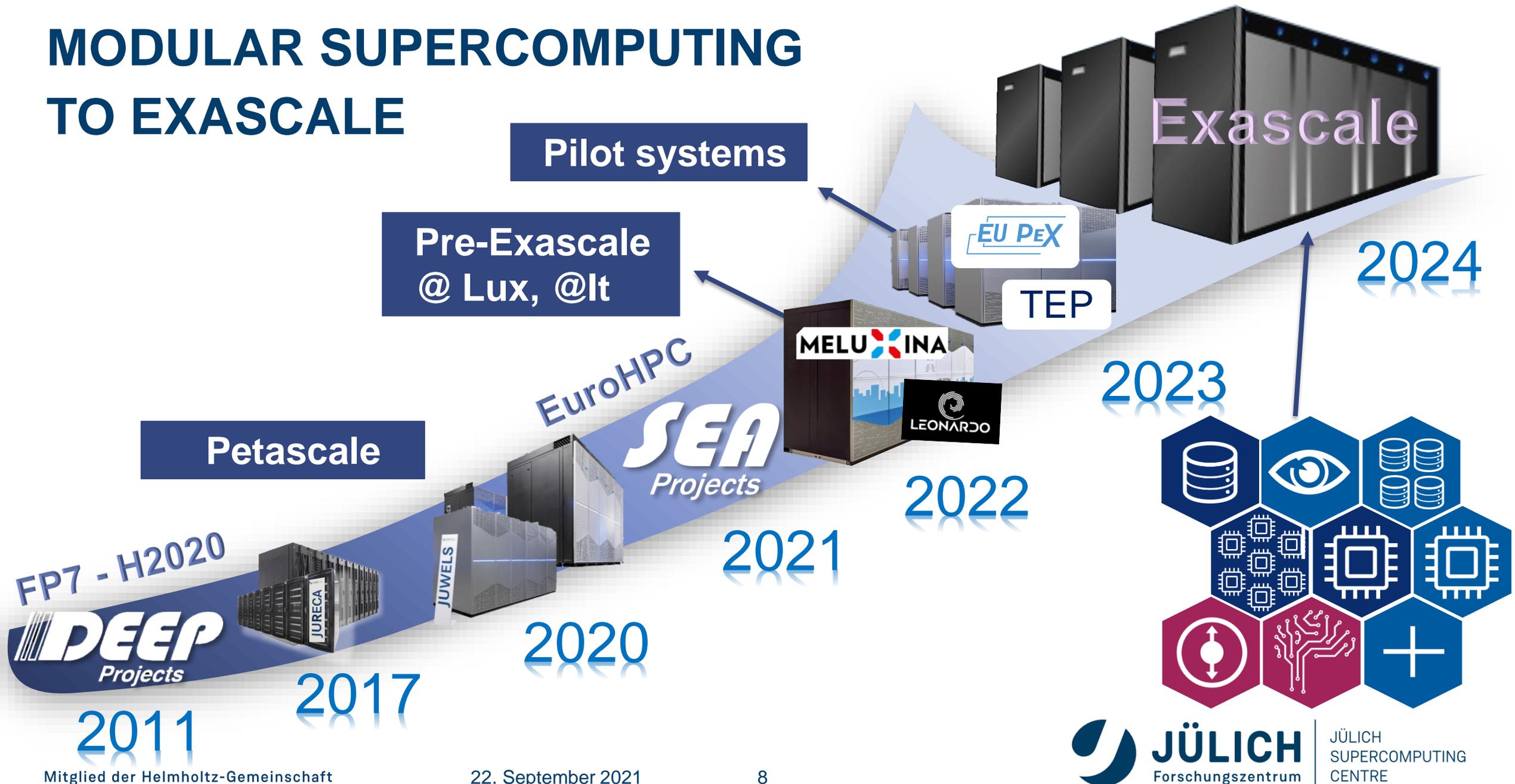
# MODULAR SUPERCOMPUTING

## Composability of heterogeneous resources

- Cost-efficient scaling
- Effective resource-sharing
- Fit application diversity
  - Large-scale simulations
  - Data analytics
  - Machine- and Deep Learning
  - Artificial Intelligence



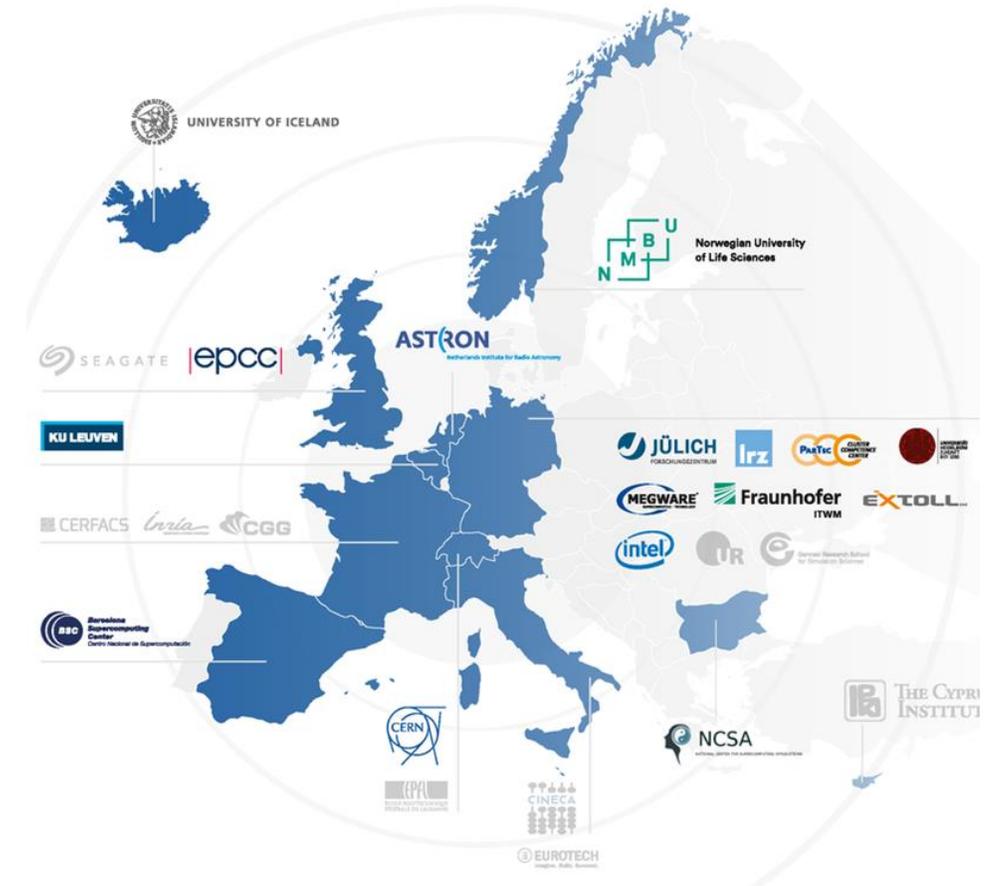
# MODULAR SUPERCOMPUTING TO EXASCALE



# BACKGROUND

## 2011-2021: The DEEP projects

- DEEP (2011 – 2015)
  - Introduced **Cluster-Booster** architecture
- DEEP-ER (2013 – 2017)
  - Added **I/O and resiliency** functionalities
- DEEP-EST (2017 – 2021)
  - **Modular Supercomputer Architecture**



# THE HARDWARE PROTOTYPES

2015



## DEEP Prototype

128 Xeon + 284 KNC nodes  
InfiniBand + 1.5Gbit Extoll  
550 TFlop/s

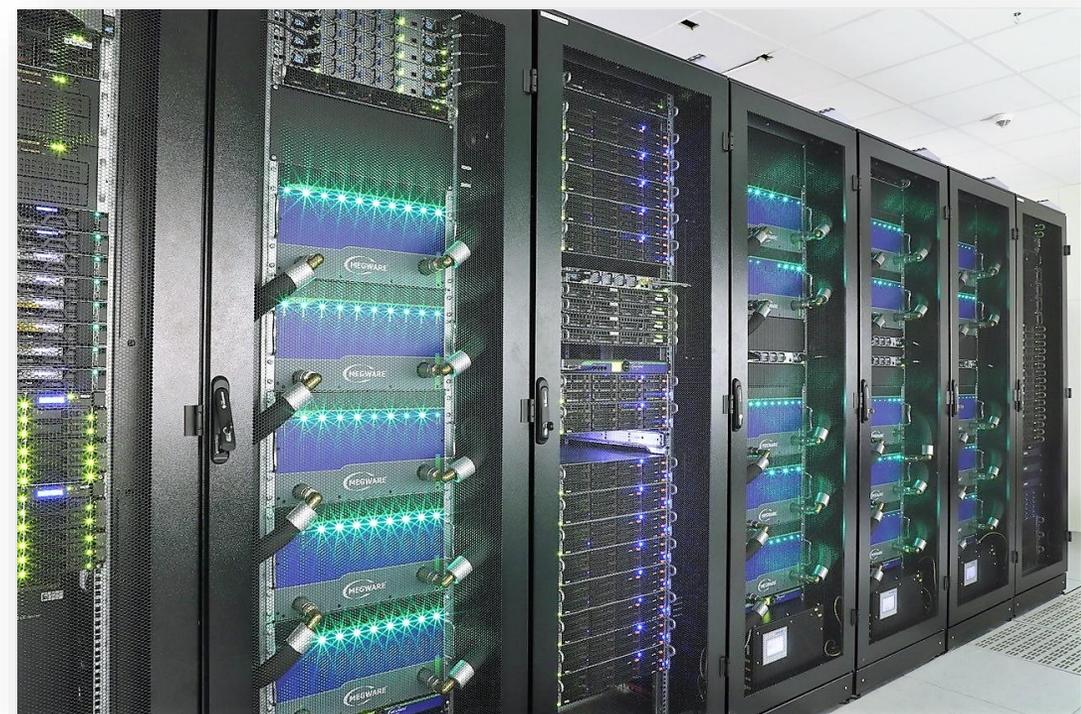
2016



## DEEP-ER Prototype

16 Xeon + 8 KNL nodes  
100Gbit Extoll  
40 TFlop/s

2020



## DEEP-EST Prototype

55 CM + 75 ESB + 16 DAM  
100 Gbit Extoll + InfiniBand + Eth  
800 TFlop/s

© FZJ

# PRODUCTION: MODULAR SUPERCOMPUTER JUWELS

## JUWELS Cluster

#65



Intel Xeon (Skylake) processor  
InfiniBand EDR network  
2,500 compute nodes  
**10 PFLOP/s peak (CPU-based)**



## JUWELS Booster

#8



AMD EPYC Rome 7402 processor  
3,700 NVIDIA A100 GPUs  
InfiniBand HDR DragonFly+  
**70 PFLOP/s peak (GPU-based)**



Funded through SiVeGCS (BMBF, MWK-NRW)

# SEA PROJECTS (EUROHPC, 2021 – 2024)



- Provide solutions for Modular Supercomputers of Exascale performance

## DEEP-SEA: DEEP Software for Exascale Architectures

- Better manage and **program compute and memory heterogeneity**
- Targets easier programming for Modular Supercomputers
- Continuation of the DEEP projects series



## IO-SEA: Input/Output Software for Exascale Architectures

- Improve **I/O and data management in large scale systems**
- Leverages results from SAGE/SAGE2 and MAESTRO projects

## RED-SEA: Network Solutions for Exascale Architectures

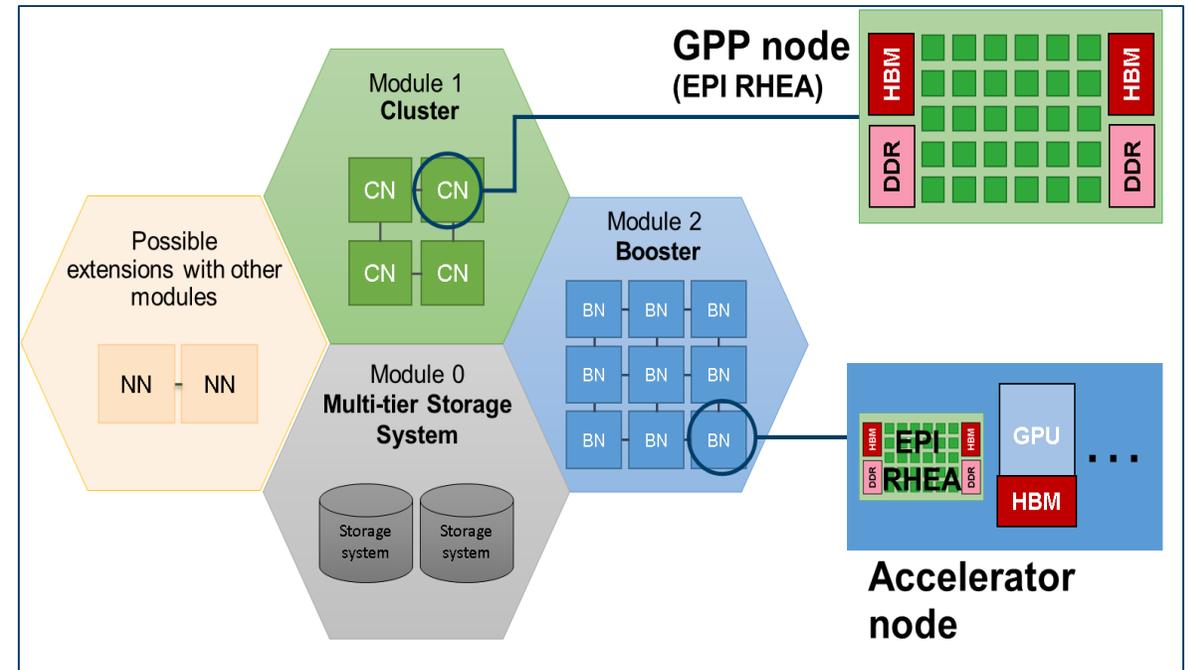
- Develops **European network** solutions
- Focus on BXI (Bull eXascale Interconnect)

# EUROPEAN PILOT FOR EXASCALE



## Towards EU Digital Sovereignty

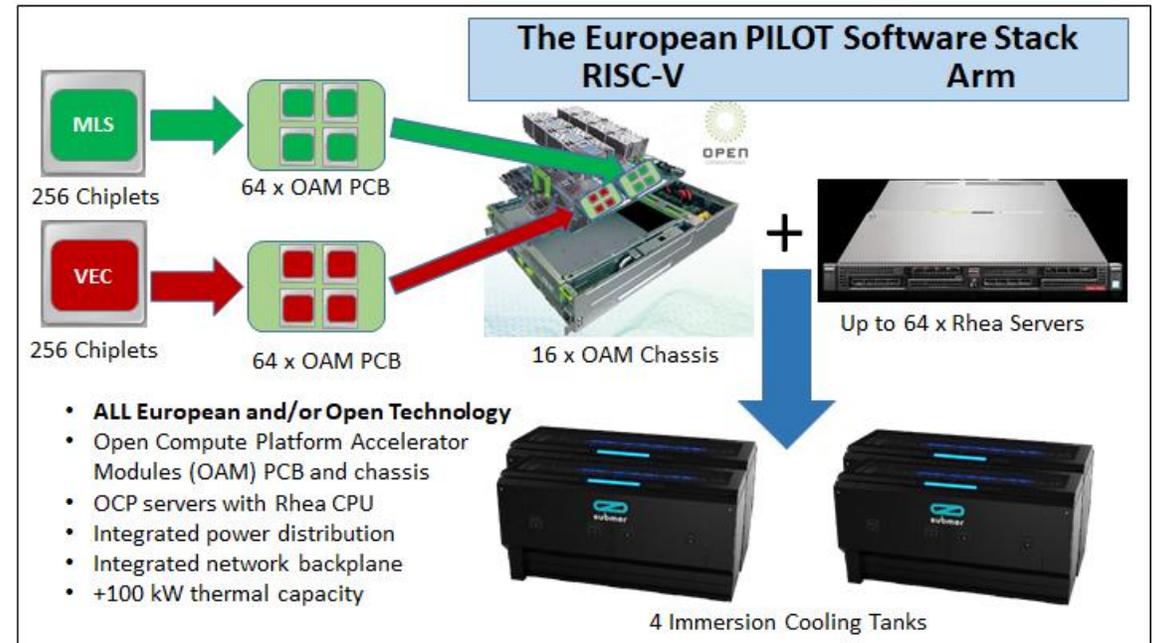
- Designing, build, and validate the first HPC platform integrating
  - European processor technology (EPI)
  - European interconnect technology (BXI)
  - and a European software stack for HPC.
- EuroHPC RIA project
  - Starting beginning of 2022
  - 19 partners all over Europe
- JSC: MSA experience, performance tools and AI applications



# THE EUROPEAN PILOT (TEP)

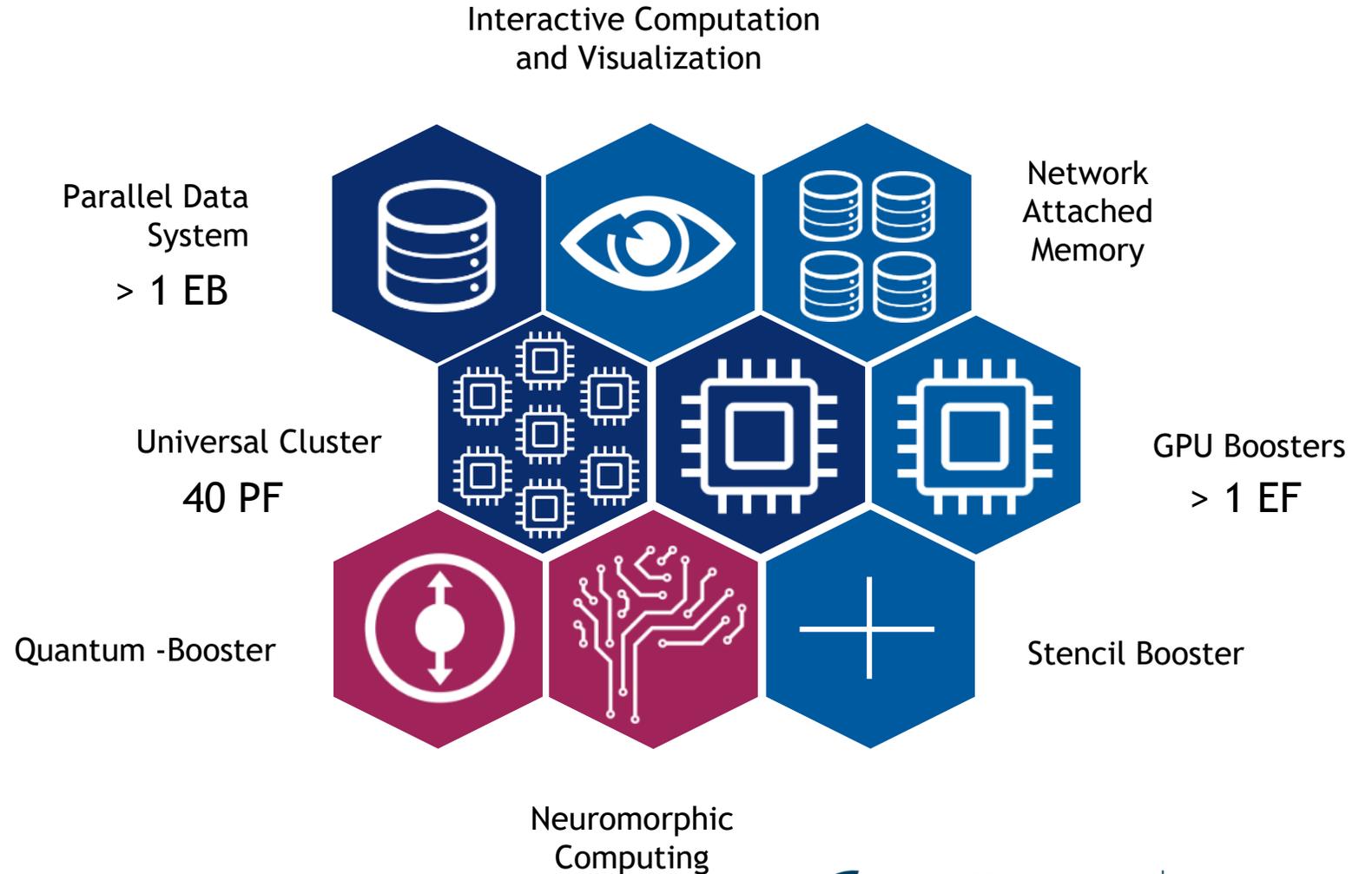
## Europe's RISC-V-based Accelerators

- Complementing ARM-based general purpose processors with specialized accelerators
- Built on Open and EU-local technologies; central: RISC-V ISA
- Two accelerators
  - *VEC*: high-performance vector accelerator
  - *MLS*: ML and stencil accelerator
- EuroHPC RIA project, starting end of 2021; 19 partners all over Europe
- JSC: numerical libraries



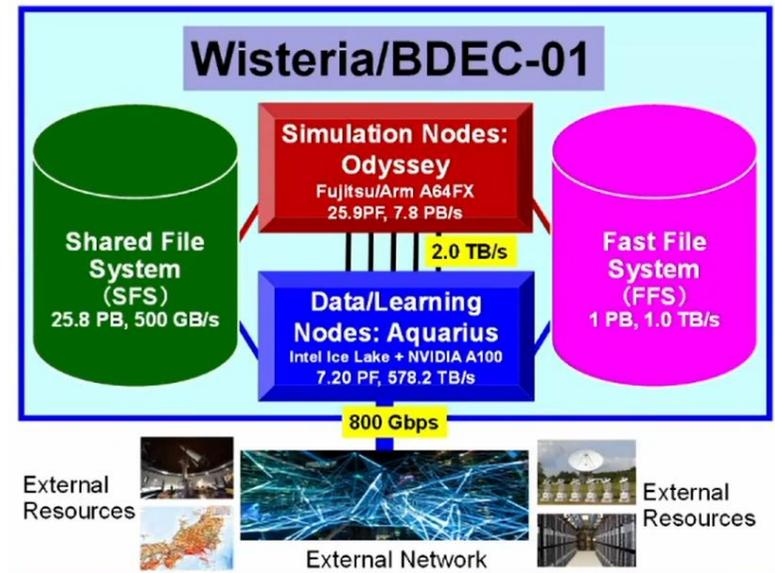
# A MODULAR EXASCALE CONCEPT

**Target: >20×**  
application performance  
compared to JUWELS  
Booster



# MODULAR SUPERCOMPUTING WORLDWIDE

- **Japan:** Wisteria/BDEC-01



The system comprises *two partitions*: a *simulation node group*, called Odyssey [Fujitsu A64Fx], and a data *analysis node group*, called Aquarius [Nvidia A100 GPUs]

<https://www.hpcwire.com/2021/02/25/japan-to-debut-integrated-fujitsu-hpc-ai-supercomputer-this-spring/>

- **USA:** Lawrence Livermore National Lab

*“We are pursuing **heterogeneous system architectures** that no longer consist of the same compute node deployed as many times as we can afford. [...] We are deploying **disaggregated systems on the same high-speed interconnect** [...], whatever overall mix of devices will best serve the workload for which we are designing the system”*

<https://www.hpcwire.com/people-to-watch-2021/>



Bronis R. de Supinski, CTO, LLNL Computing