



**9th International Workshop on
APPLications in Electronics Pervading Industry, Environment and Society
*APPLEPIES 2021***

Round Table:

**High Performance Computing Continuum:
The Italian Industry in the European Processor Initiative and Pilots**

EXASCALE: THE NEW SPACE RACE (AND AI THE NEW COLD WAR) ?

Exascale system expected to be world's most powerful computer for science and innovation

Topic: Supercomputing

May 7, 2019



Frontier (Cray/Intel + GPUs)

U.S. (2021-2023)

HPC MITC

Since 1987 - Creating the Future of Computing at the Edge and the People who Run Them

- Home
- Technologies
- Sectors
- AI/ML/DL



Aurora 21 (Cray/Intel + GPUs)

Events

retooled CORAL contract is valued at more than \$500 million; Intel is still the

**EuroHPC
(2023/2024)**



**EuroHPC
Joint Undertaking**

China (2021-2022)

Xiaomi, ShenWei, Hygon



Hygon x86 (AMD-Chinese Joint Venture) + Manycore accelerators (Matrix-2000+?)

Japan (2022)



Fugaku (Fujitsu/ARM)

THE EUROPEAN PROCESSOR INITIATIVE (EPI)

- The project aims to deliver a high-performance, low-power processor, implementing vector instructions and specific accelerators with high bandwidth memory access. The EPI processor will also meet high security and safety requirements.
- This will be achieved through intensive use of simulation, development of a complete software stack and tape-out in the most advanced semiconductor process node. SGA1 will provide a competitive chip that can effectively address the requirements of the HPC, AI, automotive and trusted IT infrastructure markets.
- Develop the roadmap for the full length of the EPI Initiative.
- Develop the first generation of technologies through a co-design approach (IPs for general-purpose HPC processors, for accelerators, for trust chips, software stacks and boards).
- Tape-out of the first-generation chip by integrating the IPs developed.
- Validate this chip in the HPC context and in the automotive context using a demonstration platform.
- Currently completing Phase 1 (EPI/SGA1).



THE EUROPEAN PROCESSOR INITIATIVE (EPI/SGA1)

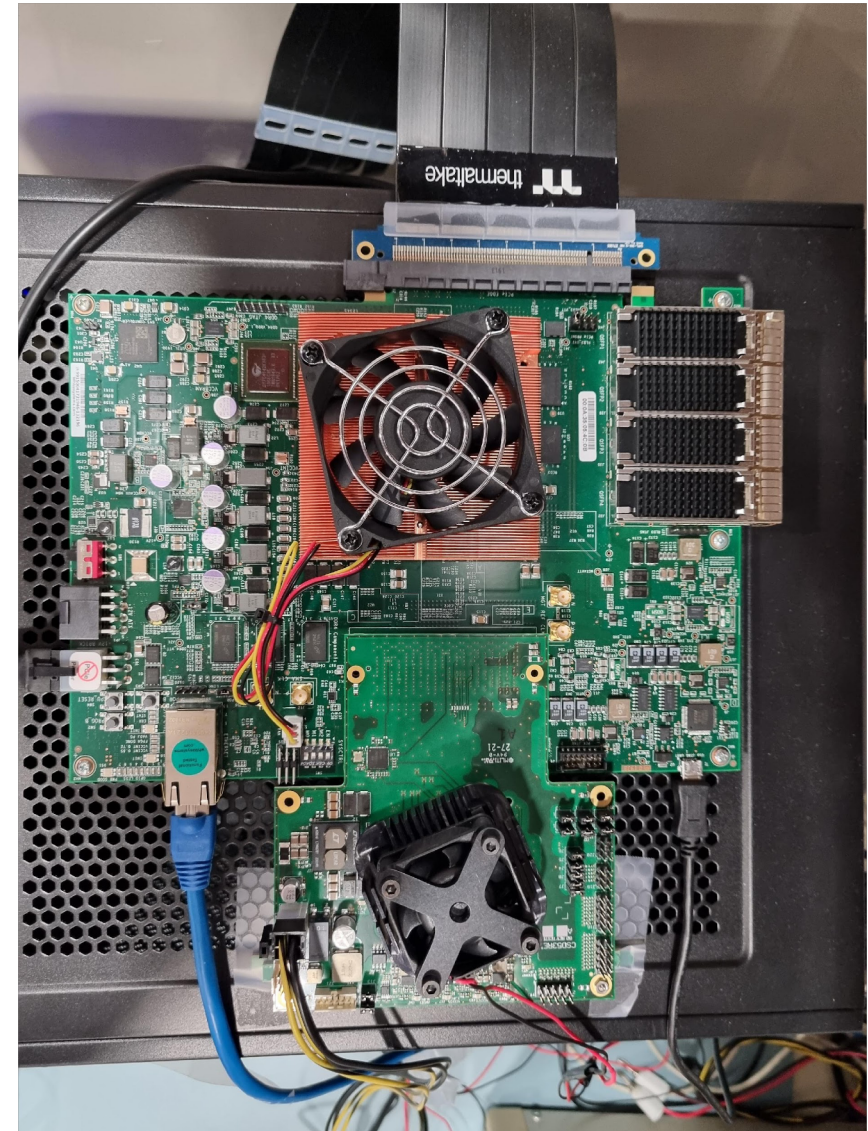


Implemented under the first stage of the Framework Partnership Agreement signed by the Consortium with the European Commission (FPA: 800928)

AS OF EARLY SEPTEMBER...



AND AS OF LAST WEEK...



AND AS OF “NOW”!

```

carv@bouklas: ~/Desktop/bringup
Read 0x00000007130 = 0x20202020230a73
Read 0x00000007138 = 0x2323232320202020
Read 0x00000007140 = 0x2320202020230a23
Read 0x00000007148 = 0x2020202020232020
Read 0x00000007150 = 0x2320202020230a23
Read 0x00000007158 = 0x2020202020202020
Read 0x00000007160 = 0x2323232323230a23
Read 0x00000007168 = 0x2323232323202023
Read 0x00000007170 = 0x202320202020200a
Read 0x00000007178 = 0x20202020200a2320
Read 0x00000007180 = 0x2020200a23202023
Read 0x00000007188 = 0x2323232020232020
Read 0x00000007190 = 0x6f540a0a23232323
Read 0x00000007198 = 0x6c637943206c6174
Read 0x000000071a0 = 0x343332203d207365
Read 0x000000071a8 = 0x0000000000a3533

Read String:
EPAC says:

Hello World!
Hola Mon!
Hallo Welt!
Bonjour Monde!
Ciao Mondo!
Geia Sou Kosme!
Hej Varlden!
Pozdrav Svijete!
Ola Mundo!
Hallo Wereld!
Hola Mundo!
Salut Lume!
Selam Dunya!
Moiien Welt!
Samubona Mhlaba!
Sulad Ambar!
Qo' vIvan!
Force Be With You World!

The answer you are looking for is:
# # # #
# # # #
#####
# #
# #
# #
#####

Total Cycles = 23435

carv@bouklas:~/Desktop/bringup_20210916/tools_new/bringup_20210916$

```

CHI_NUM_RXRSP	
CHI_NUM_RXDAT	
CHI_NUM_TXREQ	
CHI_NUM_TXRSP	
CHI_NUM_TXDAT	
CHI_NUM_TXSNP	
CHI_NUM_RXREQ_READS	
CHI_NUM_RXREQ_WRITES	
CHI_NUM_RXREQ_CLEAN_UNIQUE	
CHI_NUM_RXREQ_ATOMICS	
CHI_NUM_RXREQ_CMOS	
CHI_NUM_RXRSP_CORE	
CHI_NUM_RXRSP_REM	
CHI_NUM_RXDAT_CORE_WRITE	
CHI_NUM_RXDAT_CORE_SNPS	
CHI_NUM_RXDAT_REM	
CHI_NUM_TXREQ_READS	
CHI_NUM_TXREQ_WRITES	
CHI_NUM_TXDAT_CORE	
CHI_NUM_TXDAT_REM	
CHI_NUM_TXSNP_VALID	
CHI_NUM_TXSNP_NOT_VALID	
CHI_CREDITS	
CHI_CREDITS_OVER_UNDER	
CHI_FIFOS	
CACHE_NUM_PENDTRANS	
CACHE_NUM_PTALLOCC	
CACHE_NUM_PT1BLK	
CACHE_NUM_PT2BLK	
CACHE_NUM_HIT	
CACHE_NUM_HNR_BLK	
CACHE_NUM_HNR_UBLK	
CACHE_NUM_HNV_BLK	
CACHE_NUM_HNV_UBLK	
CACHE_NUM_PT_CNTRL_FREE_1	
CACHE_NUM_PT_CNTRL_FREE_2	
CACHE_NUM_WB_CNTRL_FREE	
CHI_SNP_ERR_ID_128_135	0x
CHI_SNP_ERR_ID_136_143	0x
CHI_SNP_ERR_ID_144_151	0x
CHI_SNP_ERR_ID_152_159	0x
CHI_SNP_ERR_ID_160_167	0x
CHI_SNP_ERR_ID_168_175	0x
CHI_SNP_ERR_ID_176_183	0x
CHI_SNP_ERR_ID_184_191	0x
CHI_SNP_ERR_ID_192_199	0x
CHI_SNP_ERR_ID_200_207	0x
CHI_SNP_ERR_ID_208_215	0x
CHI_SNP_ERR_ID_216_223	0x
CHI_SNP_ERR_ID_224_231	0x
CHI_SNP_ERR_ID_232_239	0x
CHI_SNP_ERR_ID_240_247	0x

The value of EPI for the Italian industry

- Technological leadership in a key sector
 - Create a European ecosystem for microelectronics:
 - Engineers, IP's, foundries, technologies
 - Create a European ecosystem for exascale-class applications
- Create an Italian & European ecosystem of expertise & knowledge
 - We must train, nurture and retain our talents
- Achieve the sovereignty of the Italian and European industry
 - Our industrial system faces a worldwide competition

EPI/SGA1 in Italy

- Partners:
 - CINECA
 - E4 (teaming with SECO)
 - Università di Bologna
 - Università di Pisa
 - ST-I



E4 Computer Engineering

Since 2002, E4 Computer Engineering has been innovating and actively encouraging the adoption of new computing and storage technologies. Because new ideas are so important, we invest heavily in research and hence in our future. Thanks to our comprehensive range of hardware, software and services, we are able to offer our customers complete solutions for their most demanding workloads in: HPC, Big-Data, AI, Deep Learning, Data Analytics, Cognitive Computing and for any challenging Storage and Computing requirements.

E4 Computer Engineering



Member of the Steering
Board
<http://www.etp4hpc.eu>



**ANDREAS: Artificial intelligence
trainiNg scheDuler foR
disaggrEgAted resource clusters
Value Chain Oriented and
Interdisciplinary Technology
Transfer EXperiments (TTX)**



Member of the Consortium
<http://european-processor-initiative.com>

Open  FOAM® Partnership Programme
<https://www.openfoam.com/>



Member of CERN
openlab
<https://openlab.cern/>



Member of the OEHI (Open
Edge and HPC Initiative)
<http://www.open-edge-hpc-initiative.org/>



Member of the MaX
Center of Excellence
<http://www.max-centre.eu/>



Member of HiPEAC
<https://www.hipeac.net/>

E4 Computer Engineering/EuroHPC Programs



Member of the Consortium
<http://european-processor-initiative.com>

{ SGA1
SGA2 }



<https://www.maelstrom-eurohpc.eu/>

<https://www.ligateproject.eu/>

<https://textarossa.eu/>



<https://www.admire-eurohpc.eu/>

<https://exafoam.eu/>

E4 forward-looking vision



<https://ecs-org.eu/working-groups/transcontinuum-initiative>

SECO AT A GLANCE

A GLOBAL LEADER IN THE IOT SPACE



Listed on Borsa Italiana
MTA-STAR



450+
People



5 R&D centers
3 production plants



Global
Commercial Presence

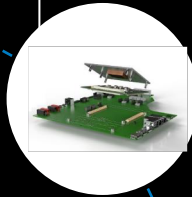


Direct Presence in
9 countries

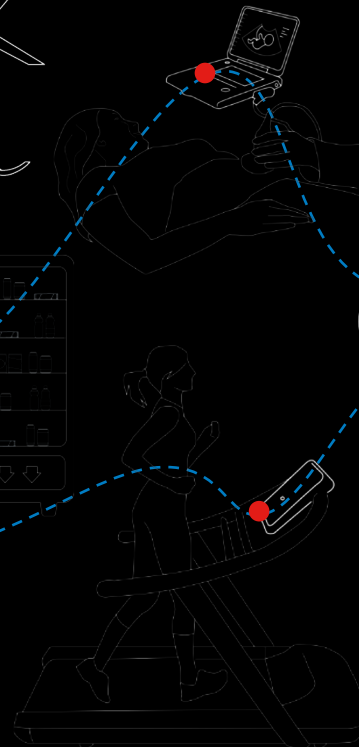
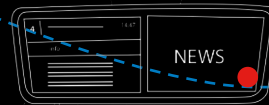
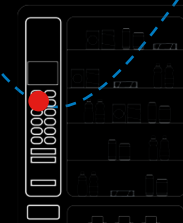
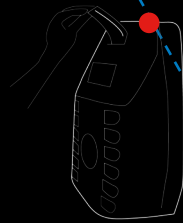
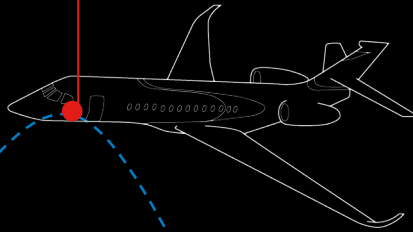


Worldwide Distribution

Edge computing
(Edge platforms,
Semi-custom, Full Custom)



Our Edge embedded on customers' products extract data



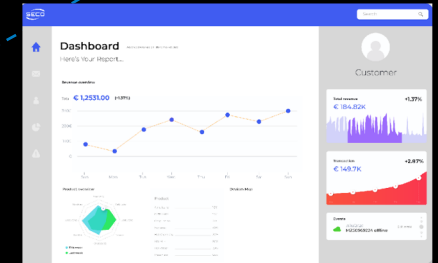
All-in-one software platform



Real-time Insights
Optimizing Decision Making

Data transfer on the Cloud

Artificial Intelligence



Data Orchestration

Real time Analytics



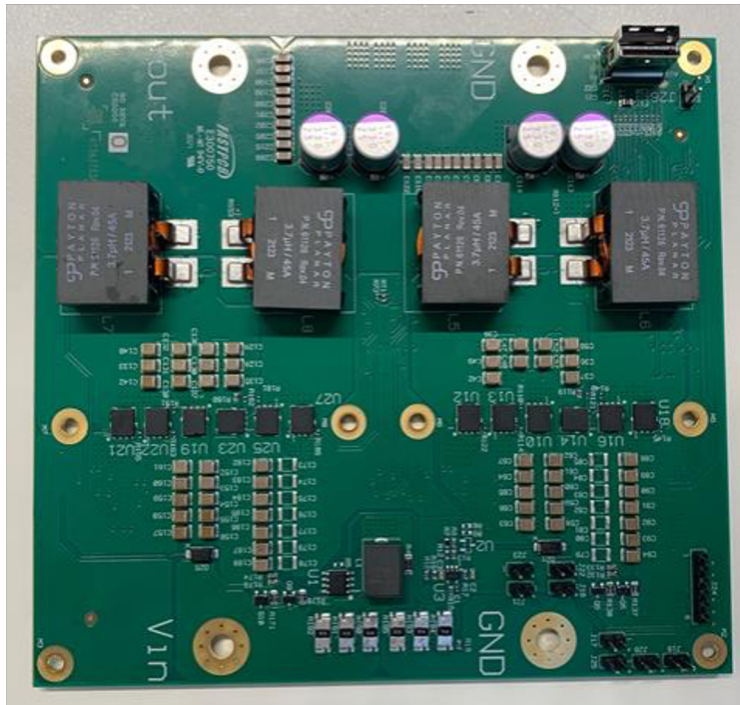
E4/SECO CONTRIBUTION TO EPI: DAUGHTER CARD FOR THE TEST CHIP



Being EPACrI an IP designed from scratch, to minimize risks, it was necessary to have the IP implemented and validated on a physical device, the Test Chip (EPACtc or TC).

SECO, thanks to its expertise on HSD design, designed and manufactured the Daughter Card, that is the adapting board to connect the TC to a FPGA. FPGA that is dedicated to give to the TC the on-chip missed features mandatory for the validation.

E4/SECO CONTRIBUTION TO EPI: INTERMEDIATE BUS CONVERTER



IBC has been introduced as the main power input stage for Rhea Lite Reference Platform designed by Atos. Being a module, it will be reused for Sequana blade, object of development in EUPEX Pilot I project, and also for the Cronos Reference Platform in EPI-SGA2.

EPI/SGA2 and Pilots in Italy

- Partners:
 - CINECA
 - E4 (teaming with SECO)
 - UniBO
 - UniPI
 - ST-I
 - LEONARDO (teaming with UniTO)
 - CINI (Consorzio Interuniversitario Nazionale per l'Informatica)
 - INGV (Istituto Nazionale di Geofisica e Vulcanologia)



EUROHPC EPI/SGA2

Objectives:

- Finalize the development and the bring-up of the first generation of low-power processor units developed in SGA1
- Develop the second generation of the General Purpose Processor (GPP) applying technological enhancements targeting the European Exascale machines with respect to the GPP (Rhea) of EPI/SG A1
- Develop the second generation of low-power accelerator test chips, usable by the HPC community for tests
- Develop sound and realistic industrialisation & commercialisation paths and Enable the long-term economical sustainability with an industrialization path in the edge computing area, demonstrated in a few well-chosen proof of concepts like video surveillance.

EUROHPC/EUPEX

Objectives:

- Designing, building, and validating the first EU platform for HPC, covering end-to-end the spectrum of required technologies with European assets: from the architecture, processor, system software, development tools to the applications.
- Featuring openness, scalability and flexibility, including the modular OpenSequana- compliant platform and the corresponding HPC software ecosystem for the Modular Supercomputing Architecture.
- Preparing HPC, AI, and Big Data processing communities for upcoming European Exascale systems and technologies.
- Representing a proof of concept for a modular architecture relying on European technologies in general and on European Processor Technology (EPI) in particular.
- First of its kind, aims at gathering, distilling and integrating European technologies that the scientific and industrial partners use to build a production-grade prototype.

EUROHPC/The European Pilot (TEP)

logo LEO

Objectives:

- The consortium in TEP, lead by BSC, and involving for Italy Leonardo and the Universities of Bologna, Pisa, Torino, Roma La Sapienza, Milano (4 are federated as third linked parties of CINI) aims at designing, building, and validating EU accelerator blades, based on VEC (vector processing) and MLS (machine learning nd stencils) chiplets
- Both VEC and MLS are RISC-V based and represents an evolution of EPAC accelerator family in EPI; the accelerator blades will be companions of host GPP units in exascale HPC machines.
- TEP will develop also a complete vertical pilot from applications to SW libraries and tools, down to HPC hardware and immersive cooling system
- Italian partners role is in applications, SW libraries and orchestration tools for AI and Big Data processing plus MLS design, FPGA-based verification of both VEC and MLS, and signal integrity HPC boards simulation
- TEP represents proof of concept for a modular architecture relying on European technologies in general and on European Processor Technology (EPI) in particular.
- TEP aims at gathering, distilling and integrating European technologies that the scientific and industrial partners use to build a production-grade prototype.

HOW E4 IS LEVERAGING EPI AND EUPEX

EPI/SGA1:

- Developing prototypes based on Rhea
- Designing products featuring Rhea
- Supporting the porting, optimization and deployment of applications on Rhea

EUPEX:

- Integrating and making available to end-users the prototype server powered by Rhea

EPI/SGA2:

- Designing products based on CRONOS
- Building and maintaining the Rhea-based cluster

Addressing the needs of emerging markets

- Designing optimized solutions for AI/ML/DL based on the Rhea
- Addressing the needs of the smart edge market

Expanding the skills of its workforce

HOW SECO IS LEVERAGING EPI AND EUPEX

EPI/SGA1:

- Designing and Manufacturing prototypes Rhea power supply
- Designing and Manufacturing prototypes for EPAC Test Chip

EUPEX:

- Designing and Manufacturing prototypes for discrete GPU blade server powered by Rhea

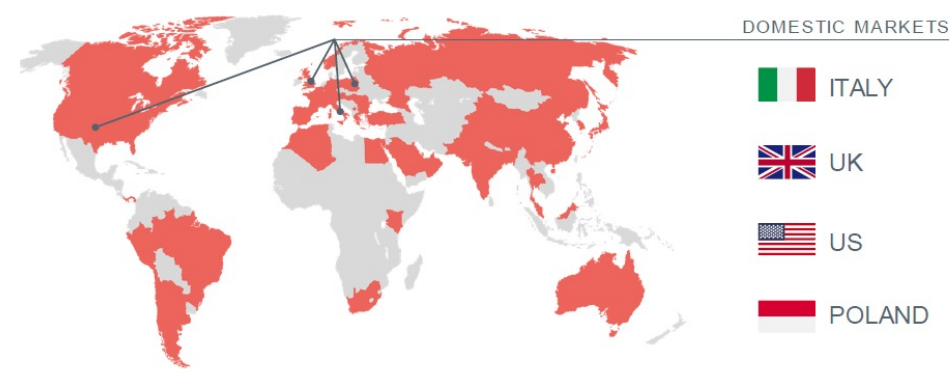
EPI/SGA2:

- Designing and Manufacturing the Rhea-based Prototype
- Evangelizing emerging markets through the adoption of the European technologies to create a new value chain, a sort of European electronics districts that can face future challenges such as independence from the Asian and US supply chain, and data protection, an increasingly strategic asset of European Governments.
- Adopting new and more efficient high performing solutions to the far edge in different verticals as industrial, security & defense, automotive, railway, medical.



Leonardo is a global company in the Aerospace, Defence, Digital and Security sector with an integrated offer of high tech solutions for military and civil applications.

WORLDWIDE FOOTPRINT



PEOPLE

TOTAL WORKFORCE

	49,882
ITALY:	31,052
UK:	7,387
US:	7,299
POLAND:	2,586
REST OF THE WORLD:	1,558

Air A wide range of aircraft, helicopters and avionics for commercial, public services, security and defence applications, as well as advanced solutions for training and simulation and safe air traffic management.	Space An integrated offer that covers the complete value chain of space industry, from satellite services for geo-information, communication and navigation, to space manufacturing, as well as equipment and payloads for exploration missions.
Land A complete portfolio of platforms and systems to provide Armed Forces with integrated capabilities for ground superiority, in any conventional and asymmetric scenario.	Cyber & Security Integrated solutions for safety and security of territories, critical national infrastructures, citizens and enterprises, with the highest level of protection, situational awareness and information superiority.
Sea Integrated solutions for total naval dominance that meet all the requirements of any type of modern ship, from the smallest units through to the largest aircraft carriers, enabling them to carry out any kind of mission.	Unmanned Systems End-to-end Unmanned Systems with high interoperability with other platforms and a flexible multi-role capability, to fulfil a wide spectrum of missions.

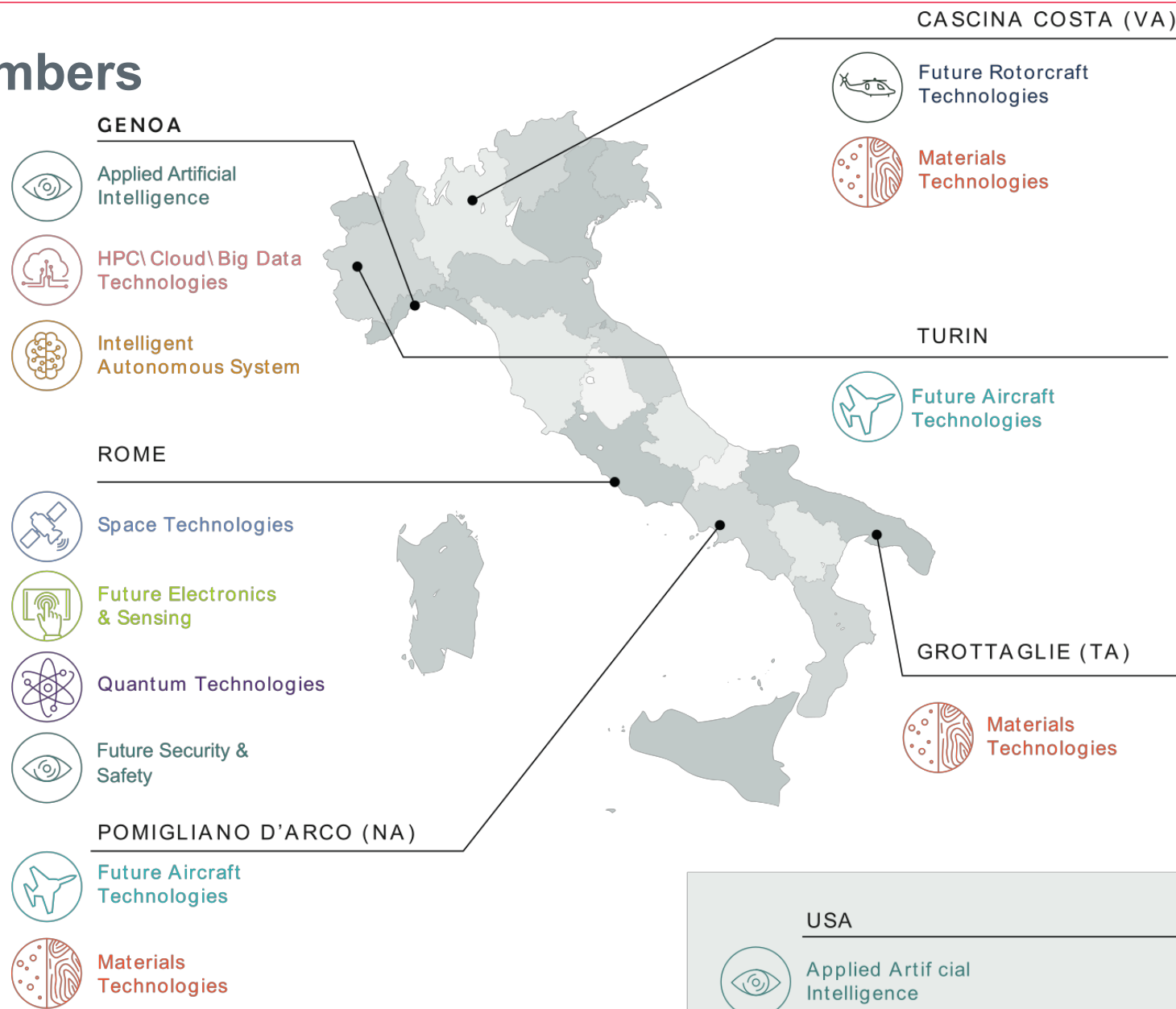
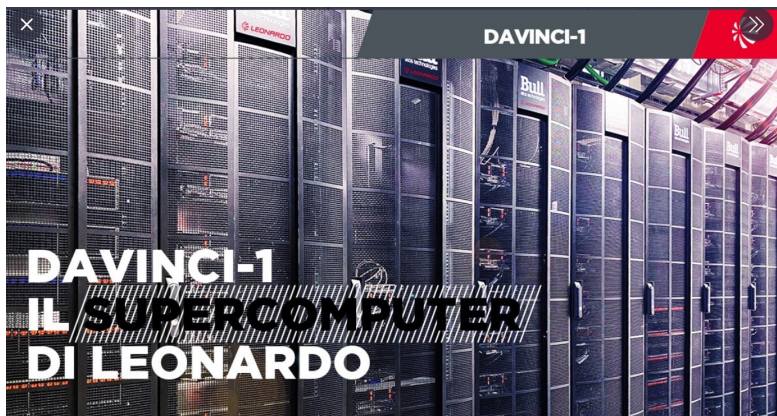
In Leonardo Masterplan 2030, our Group has defined an innovation strategy to support digital transformation initiatives, through the adoption of HPC, Cloud Computing, innovative electronic components and communication equipment as next generation IoT devices supporting portability of cybersecurity, AI applications and processes in our reference market sectors of Aerospace, Defense and Professional communication with an additional focus on Energy efficiency and environment sustainability and Healthcare, enlarging Leonardo business strategy.

€ 13.4 BN REVENUES	€ 13.8 BN NEW ORDERS	€ 35.5 BN ORDER BACKLOG	€ 1.6 BN R&D 12% OF REVENUES	
SMALL & MEDIUM ENTERPRISES' PERCENTAGE IN DOMESTIC SUPPLY CHAINS	86%  ITALY	71%  UK	71%  US	87%  POLAND



The Leonardo Labs - Numbers

- The main Leonardo Labs numbers are:
 - 10 Leonardo Labs (1 in USA)
 - 30 research units,
 - 4 joint external laboratories
 - 80+ research fellows
 - 30+ PhD
- Davinci-1 supercomputer for the Labs R&D
 - 5 Pflops of computing power
 - 20 PByte of storage capacity





Leonardo within the European Innovation ecosystem

Leonardo is actively involved in many **European Initiatives** and projects on **AI, HPC, Cloud/Edge Computing** and participates to many **H2020/HE, EDIDP, EDF** projects on **HPC, AI, Cybersecurity** and **Advanced Digital Skills**, like:



HOW LEONARDO IS LEVERAGING EPI

- Leonardo is involved in the second phase of EPI (EPI SGA 2), having closely monitored Phase I
- Use case: Massive Video Surveillance for smart cities and infrastructures
- Target application: Autonomous HPC use cases (i.e. deployment on the edge).
- Target platforms: RHEA, CRONOS and RISC-V Accelerators, respectively
- Main Tasks:
 - Identification of non-functional Requirements & Constraints (*Energy, Performance, Costs, Dimensions, Computing, Confidentiality,....*)
 - Analysis to verify to what extent they are met by EPI architecture, suggesting areas of potential improvements
 - Development and Testing of SW libraries, together with the University of Torino, to support federated/distributed training and inference of DNNs and feature extraction algorithms for video-based applications for massive surveillance

HOW LEONARDO IS LEVERAGING EPI

- Goals:
 - Find and optimize the HPC scaling path to fit with the compelling constraints of the (high volume) embedded applications and market
 - Evaluation of Trusted Platform Modules (TPMs), Trusted Execution Environment (TEE), and other technologies for enhanced hardware-based encryption and isolation
 - Steering of the specs of the EPI processor to meet the needs of the embedded/edge computing for Aerospace, Defence & Security applications
 - Evaluation of the EPI processor to be included in Leonardo Aerospace, Defence and Security products

HOW LEONARDO IS LEVERAGING TEP



- Use case: A real-time distributed AI surveillance at a large scale (smart cities, smart landscapes) involving, but not limited to, people/vehicle counting and their distance/motion analysis, body/face recognition, plate readings, for a safe and secure society
- TEP architecture main focus: AI kernels of RISC V accelerator
- Main tasks:
 - Provider of Use Case Data and Testing Infrastructure (DAVINCI-1)
 - Co-design of AI instructions of RISCV for EDGE applications to support the definition of Derivative HW and SW Architectures of MLS and VEC chiplets for Edge Computing
 - Development of AI application, together with CINI, to process hundreds of video streams in real-time applying concurrently different algorithms for multiple feature detection threads and then implementing DNN-based classifications.

HOW LEONARDO IS LEVERAGING TEP

- Goals:
 - Evaluation of TEP architecture in EDGE computing applications, and in the context of Deep Learning as solution for the HPC facility towards exascale as an engine for hyperparameters optimization and training
 - Evaluation of the European Pilot architecture and EPI accelerators to meet the needs of Aerospace and Defence and Security applications
 - Evaluation of the European Pilot architecture to be adopted in Leonardo Aerospace, Defence and Security products

Round Table: High Performance Computing Continuum: The Italian Industry in the European Processor Initiative

Sergio Saponara
Daniela Ghezzi
Fabio Ottonelli/Gianluca Venere
Fabrizio Magugliani

UniPisa
Leonardo
SECO
E4

