EPI EPAC1.0 RISC-V Test Chip Samples Delivered

Another step closer to demonstrate the capabilities of a RISC-V based European microprocessor

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The European Processor Initiative (EPI) https://www.european-processor-initiative.eu/, a project with 28 partners from 10 European countries, with the goal of making EU achieve independence in HPC chip technologies and HPC infrastructure, is proud to announce that EPAC1.0 RISC-V Test Chip samples were delivered to EPI and initial tests of their operation were successful.

One key segment of EPI activities is to develop and demonstrate fully European-grown processor IPs based on the RISC-V Instruction Set Architecture, providing power-efficient and high-throughput accelerator cores named EPAC (European Processor Accelerators).

EPAC combines several accelerator technologies specialized for different application areas. The test chip, shown in the figure below, contains four vector processing micro-tiles (VPU) composed of an Avispado RISC-V core designed by SemiDynamics and a vector processing unit designed by Barcelona Supercomputing Center and the University of Zagreb. Each tile also contains a Home Node and L2 cache, designed respectively by Chalmers and FORTH, that provide a coherent view of the memory subsystem. The chip also includes two additional accelerators: the Stencil and Tensor accelerator (STX) designed by Fraunhofer IIS, ITWM and ETH Zürich, and the variable precision processor (VRP) by CEA LIST. All accelerators on the chip are connected with a very high-speed network on chip and SERDES technology from EXTOLL.

The 143 packaged EPAC test chip samples were fabricated in GLOBALFOUDNRIES 22FDX low-power technology, have an area of 26.97mm^2, 14 million placeable instances (93M Gate Equivalent) including 991 memory instances, are packaged in FCBGA with 22x22 balls and have a target frequency of 1GHz.

Figure 1 EPAC test samples

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 826647

Initial bring-up was successful and EPAC executed its first bare metal program sending the traditional "Hello World!" greetings in different languages to EPI consortia and the world!

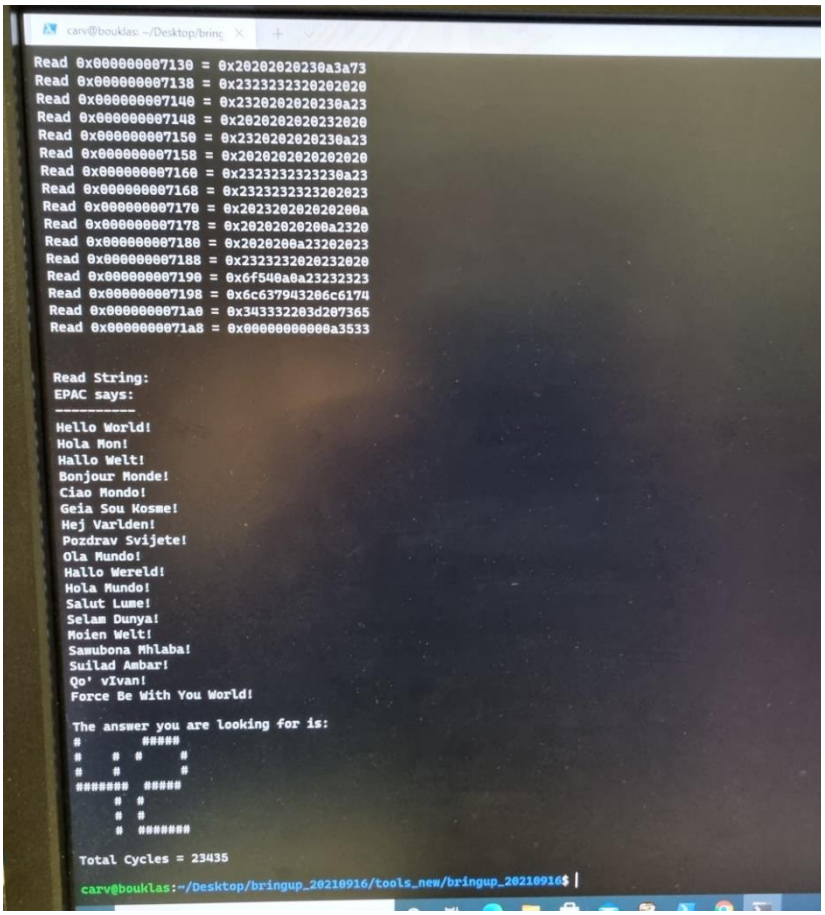

Figure 2 Hello World! screenshot

The outlook

EPI will continue to develop, optimize and validate different IP blocks and demonstrate features and performance of those thus creating an EU HPC IP ecosystem and make it available to the processor and accelerator industry and academia to create globally competitive production class building blocks for the next generation HPC systems.

About EPI

The European Processor Initiative (EPI) is a project currently implemented under the first stage of the Framework Partnership Agreement signed by the Consortium with the European Commission (FPA: 800928), whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications.

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