

EPI EPAC1.0 RISC-V Test Chip Samples Delivered

Another step closer to demonstrate the capabilities of a RISC-V based European microprocessor

EU, 22.09.2021.

The European Processor Initiative (EPI) <u>https://www.european-processor-initiative.eu/</u>, a project with 28 partners from 10 European countries, with the goal of making EU achieve independence in HPC chip technologies and HPC infrastructure, is proud to announce that EPAC1.0 RISC-V Test Chip samples were delivered to EPI and initial tests of their operation were successful.

One key segment of EPI activities is to develop and demonstrate fully European-grown processor IPs based on the RISC-V Instruction Set Architecture, providing power-efficient and high-throughput accelerator cores named EPAC (European Processor Accelerators).

EPAC combines several accelerator technologies specialized for different application areas. The test chip, shown in the figure below, contains four vector processing micro-tiles (VPU) composed of an Avispado RISC-V core designed by SemiDynamics and a vector processing unit designed by Barcelona Supercomputing Center and the University of Zagreb. Each tile also contains a Home Node and L2 cache, designed respectively by Chalmers and FORTH, that provide a coherent view of the memory subsystem. The chip also includes two additional accelerators: the Stencil and Tensor accelerator (STX) designed by Fraunhofer IIS, ITWM and ETH Zürich, and the variable precision processor (VRP) by CEA LIST. All accelerators on the chip are connected with a very high-speed network on chip and SERDES technology from EXTOLL.

The 143 packaged EPAC test chip samples were fabricated in GLOBALFOUDNRIES 22FDX lowpower technology, have an area of 26.97mm², 14 million placeable instances (93M Gate Equivalent) including 991 memory instances, are packaged in FCBGA with 22x22 balls and have a target frequency of 1GHz.



Figure 1 EPAC test samples

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Initial bring-up was successful and EPAC executed its first bare metal program sending the traditional "Hello World!" greetings in different languages to EPI consortia and the world!

carv@bouklas: -/Desktop/bring X + V
ad 0x00000007130 = 0x202020230a3a73
ad 0x000000007138 = 0x2323232320202020
ad 8x888888887148 = 8x232828282828238a23
ad 6x868686867148 = 6x2828282828282828
ad 0x00000007150 = 0x2320202020230a23
ead 0x00000007158 = 0x20202020202020
ead 0x000000007160 = 0x23232323230a23
ead 0x00000007168 = 0x2323232323202023
ead 0x000000007170 = 0x2023202020200a
ead 0x000000001178 = 0x2020200200ea2320
ead 0x00000000188 = 0x2020200123202023
Eau 0x0000000188 = 0x1513132820232820
kau 0.00000000109 = 00005040023232323
Read String:
EPAC says:
Hello World!
Hola non:
Ratio Wett: Banjour Hondel
Ciao Mondol
Geia Sou Kosme!
Hej Varlden!
Pozdrav Svijete!
Ota nundol
Hola Mundoi
Salut Lume!
Selam Dunya!
Hoien Welt!
Sawubona mhladai Guilad Ambari
Oc' Vivani
Force Be With You World!
The second s
The answer you are cooking for is.

A CONTRACT AND A CONTRACT
Total Cycles = 23435
(notice /boingue 20210016/tools new/bringue 20210916\$
carv@bouklas:~/Desktop/bringup_20210910/coots_new/oringup_control

Figure 2 Hello World! screenshot

The outlook

EPI will continue to develop, optimize and validate different IP blocks and demonstrate features and performance of those thus creating an EU HPC IP ecosystem and make it available to the processor and accelerator industry and academia to create globally competitive production class building blocks for the next generation HPC systems.

About EPI

The European Processor Initiative (EPI) is a project currently implemented under the first stage of the Framework Partnership Agreement signed by the Consortium with the European Commission (FPA: 800928), whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications.

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