European Processor Initiative

Open Edge and HPC Initiative

June 22, 2021 16:00-18:00 CEST

EPI
THE PLACE WHERE ARM AND RISC-V LIVE IN PEACE

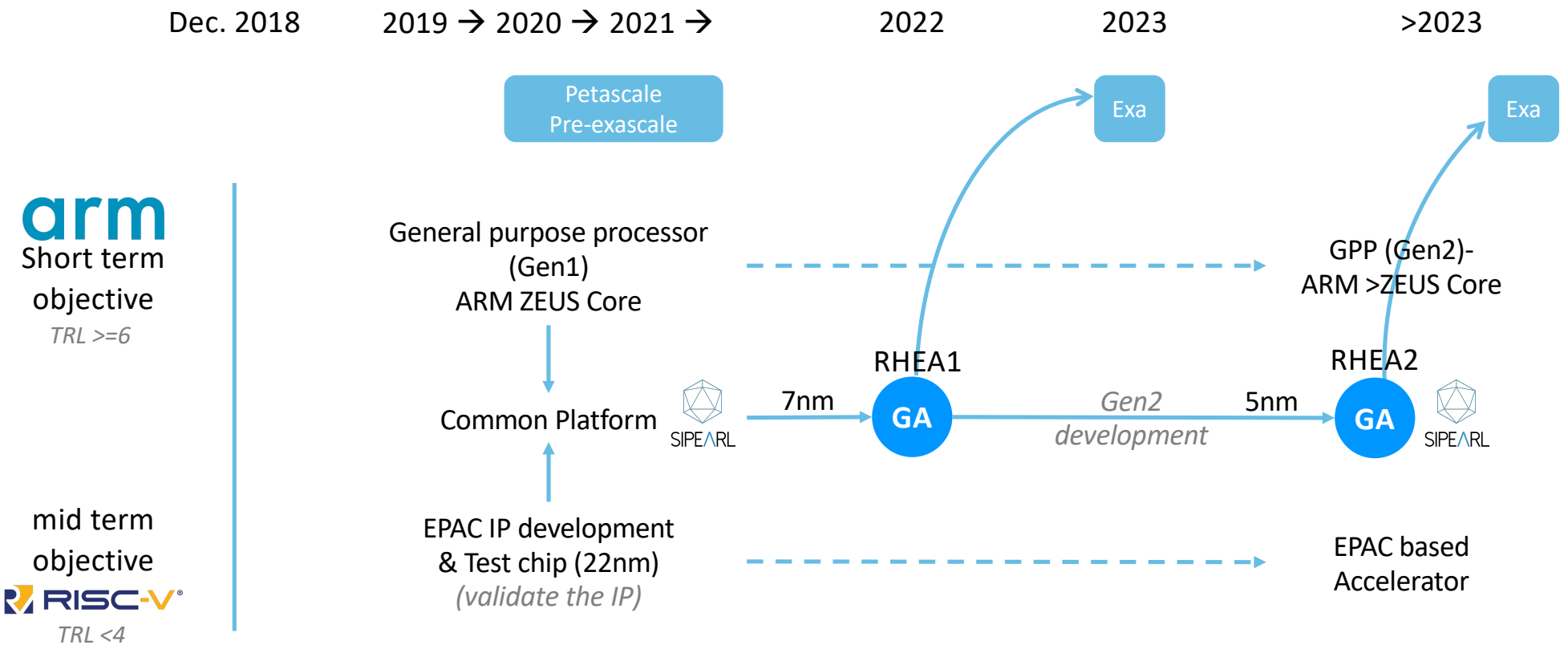
THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION'S HORIZON 2020 RESEARCH AND INNOVATION PROGRAM UNDER GRANT AGREEMENT NO 826647

EPI objectives

- **Overall: Develop a complete EU designed high-end microproce**
  Supercomputing and edge-HPC segments.
- Short-term objective
  - supply the EU-designed microprocessor to empower the EU Exasca
- Long-term objective
  - Europe needs a sovereign (=not at risk of limitation or embargo by
    access to high-performance, low-power microprocessors, from IP to
- EPI has been set to fulfil this objective
- EPI has to cover all Technical Readiness levels (TRL)
  - TRL 1-5 are for long-term objectives (EU IP)

    and
  - TRL 6-9 are for short to mid-term objectives (decade) with products design

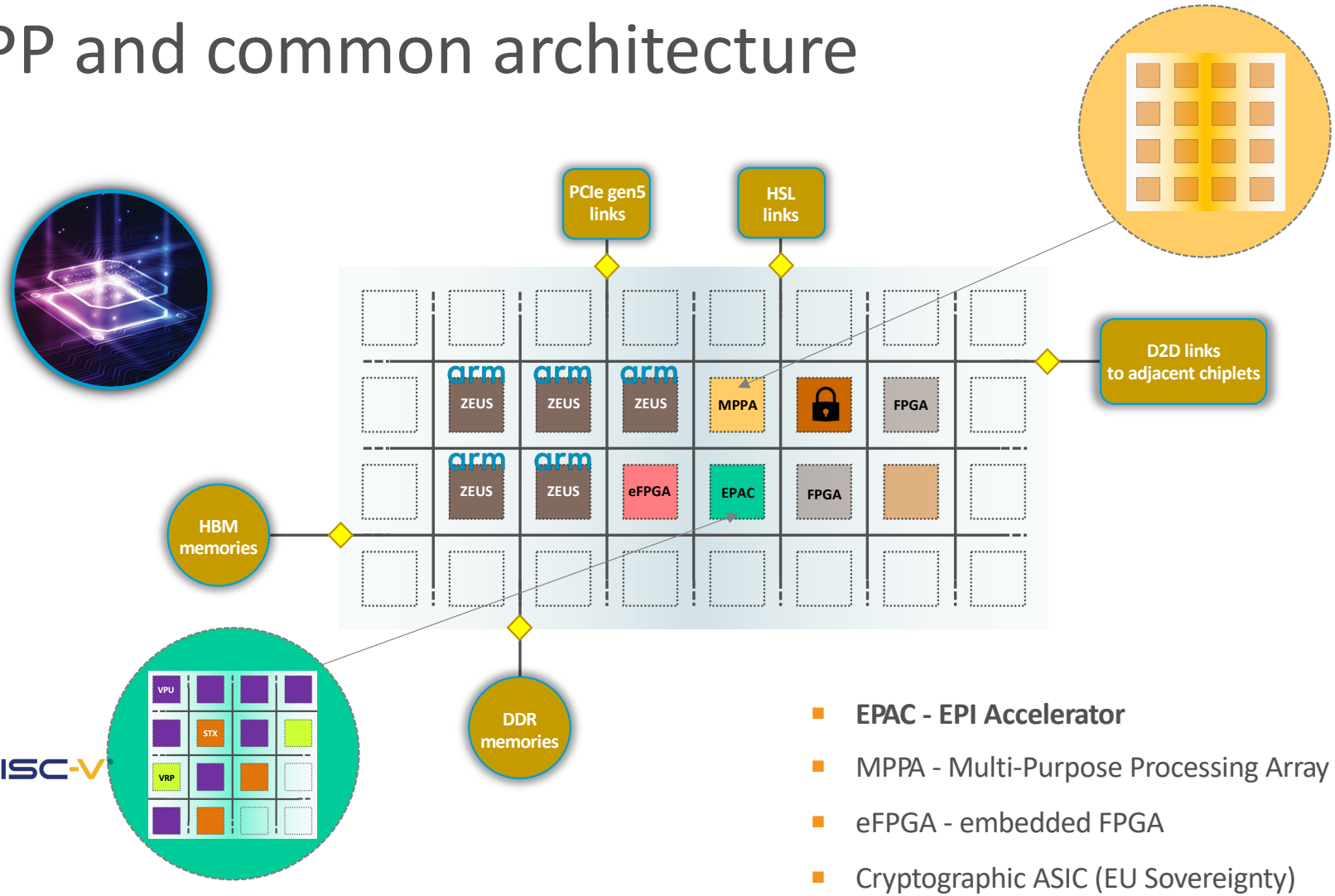
Overall roadmap



EPI (RHEA PROCESSOR)

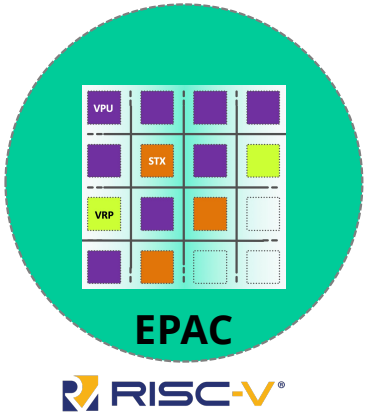
ARM – RISC-V ECOSYSTEM

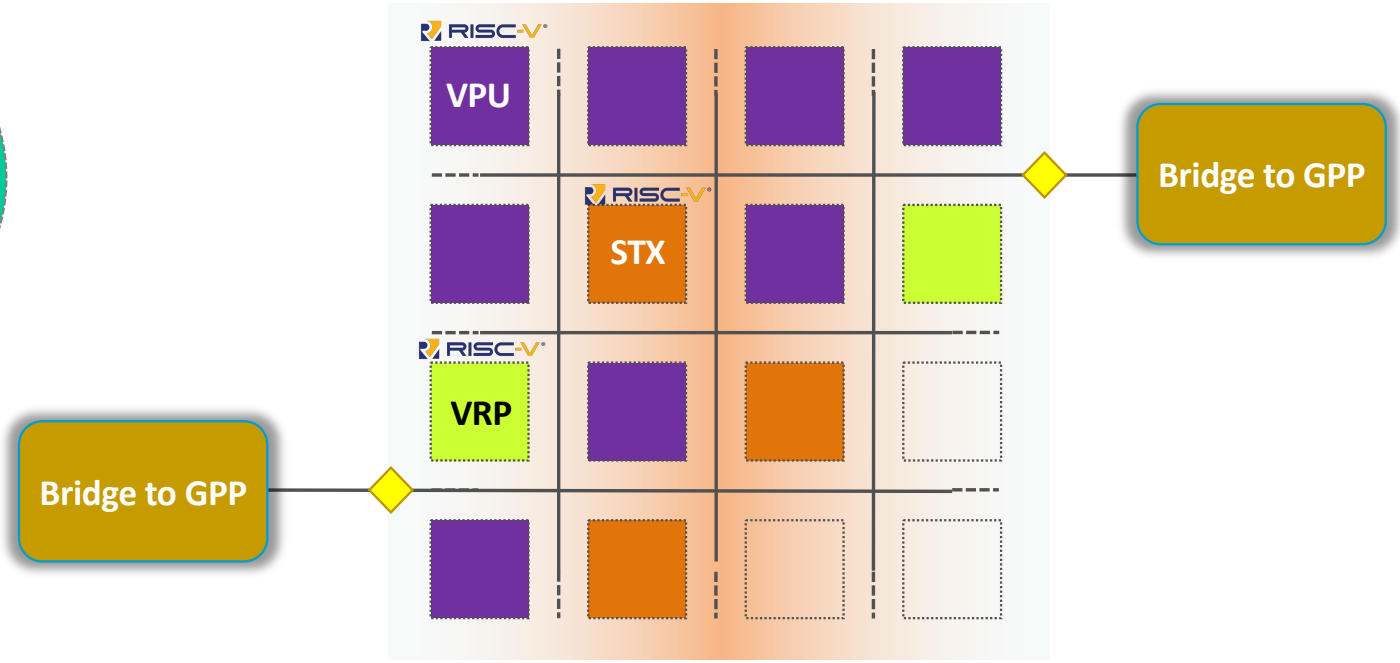
GPP and common architecture



- **EPAC - EPI Accelerator**
- MPPA - Multi-Purpose Processing Array
- eFPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)

EPAC – RISC-V Accelerator





- VPU – Vector Processing Unit
- STX – Stencil & Tensor accelerator
- VRP – Variable precision Unit

WRAP-UP

EPI smartly combines ARM and RISC-V

- With ARM
  - We fulfil short term EuroHPC objectives with a competitive product available no later than 2023
  - We (re) learn how to design high-end microprocessor
  - We take advantage of ARM momentum in HPC, cloud and Datacenter
- With RISC-V
  - We prepare the future
  - We develop all fundamental IPs we need for high-endHPC accelerators and CPUs
  - We prove it works with the most advanced manufacturing processes
- We proves that ARM and RISC-V are complementary

THANK YOU FOR YOUR ATTENTION

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