EUROPEAN PROCESSOR INITIATIVE

European
Processor
Initiative

European Processor Initiative

FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES

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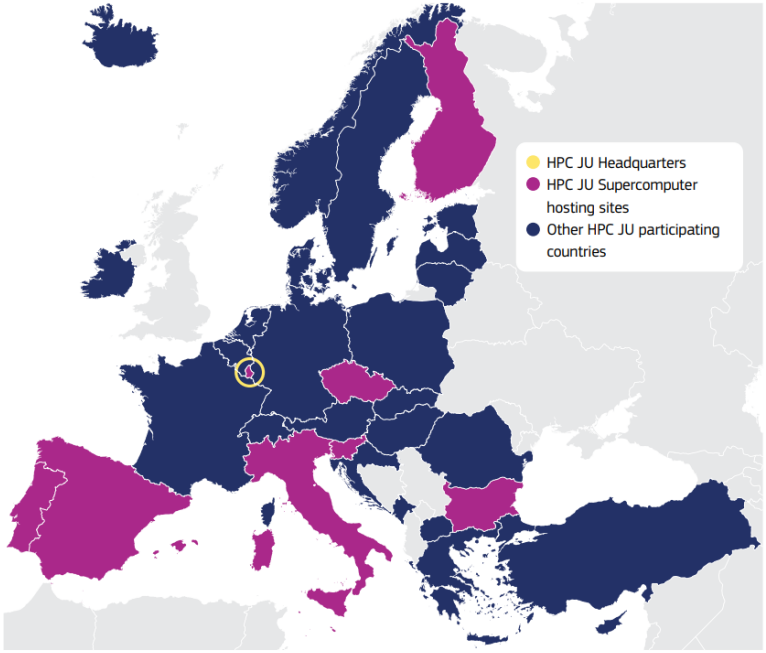
EPI OVERVIEW AND INTRODUCTION

FABRIZIO MAGUGLIANI (E4 COMPUTER ENGINEERING) ON BEHALF OF THE WHOLE AWESOME EPI TEAM

EU EXASCALE HPC STRATEGY

- March 2017, Rome: EC launched the *EuroHPC declaration*
- November 2018, EuroHPC Joint Undertaking, a 1 billion Euro joint initiative between the EU and European countries to develop a World Class Supercomputing Ecosystem in Europe
- Oct 2020: 32 participating countries



EUROPE'S AMBITION: EUROHPC JU

- Developing a new European supercomputing ecosystem: HPC systems, network, software, applications, access through the cloud
- Making HPC resources available to public and private users, including SMEs.
- Stimulating a technology supply industry

28 PARTNERS FROM 10 EU COUNTRIES

HTTPS://WWW.EUROPEAN-PROCESSOR-INITIATIVE.EU/

EPI OBJECTIVES

- Overall: Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments
- Short-term objective
  - supply the EU-designed microprocessor to empower the EU Exascale machines
- Long-term objective
  - Europe needs a sovereign (=not at risk of limitation or embargo by non-EU countries) access to high-performance, low-power microprocessors, from IP to products
- EPI has been set to fulfil this objective
- EPI has to cover all Technical Readiness levels (TRL)
  - TRL 1-3 are for long-term objectives (EU IP)

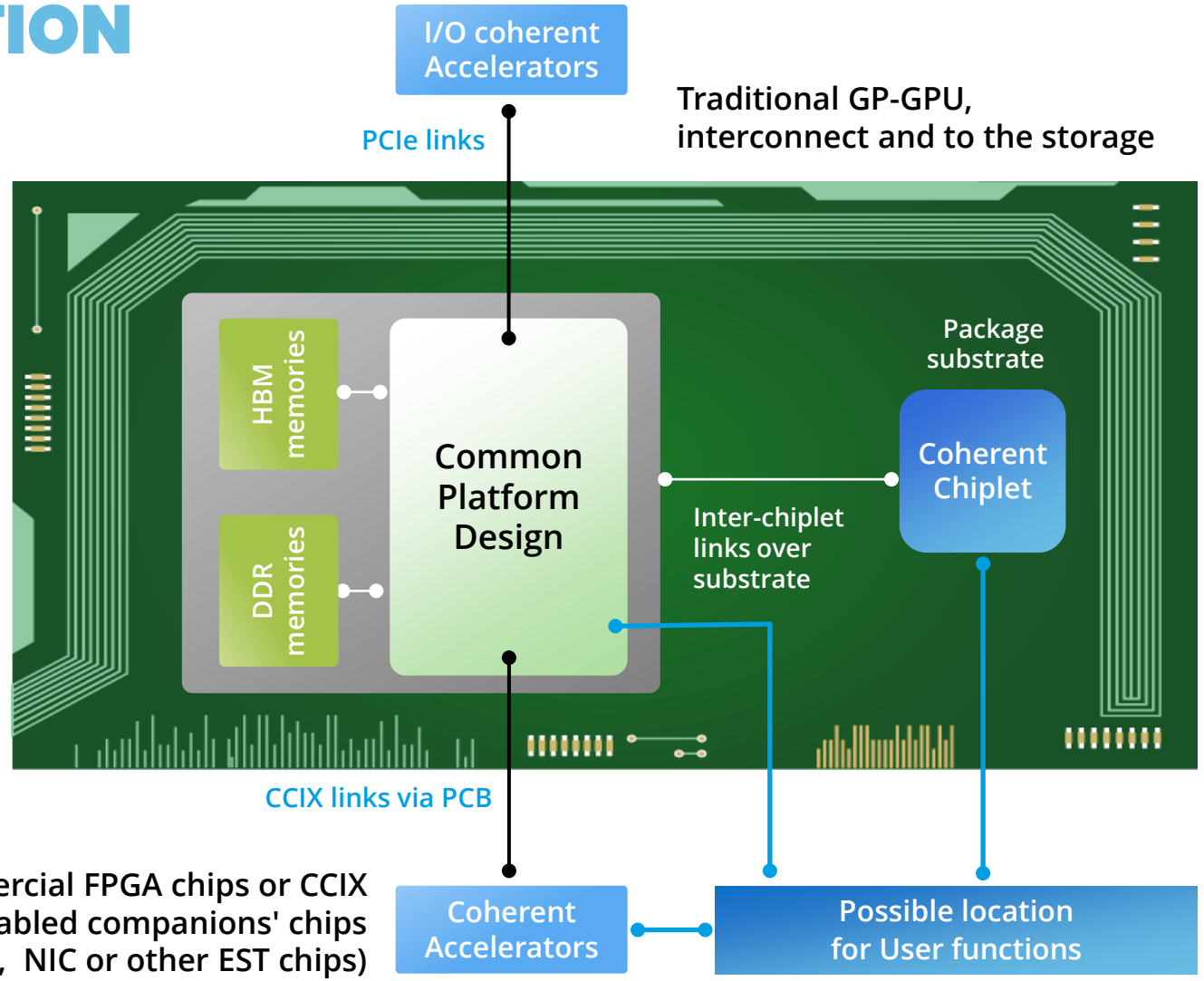
and

  - TRL 4-9 are for short to mid-term objectives (decade) with products designed in EU

EPI COMMON PLATFORM

HETEROGENEOUS INTEGRATION

- Allows integration of customized functions in chip, in package, on board, or over PCIe or network link
- EPI Accelerators work in I/O coherent mode and share the same memory view. Single or dual chiplet package for power efficient sizing
- Designing for high Byte/FLOP ratio
- HBM2e, DDR5 and PCIe gen5
- Coherent NoC with system level cache to keep data local
- D2D interface open to EPI (and beyond)



COMMON PLATFORM TO HARMONIZE THE HETEROGENEOUS COMPUTING ENVIRONMENT

Computing Units

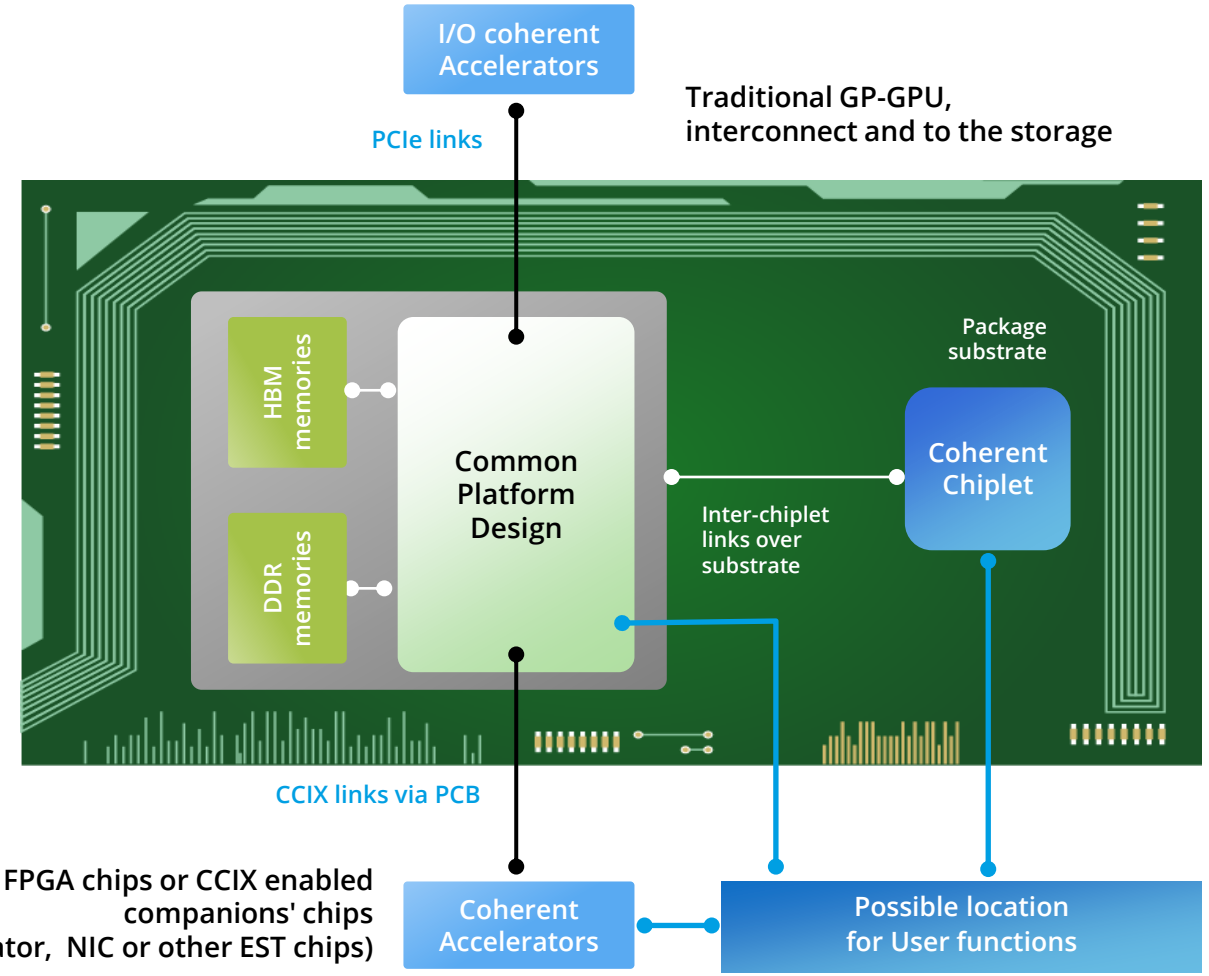
- Arm – Scalable Vector Extension
- MPPA - Multi-Purpose Processing Array
- EPAC – RISC-V based Accelerators
- eFPGA - embedded FPGA

METHODOLOGY

Architects + Model and simulation ⟷ Co-design ⟷ Application Experts

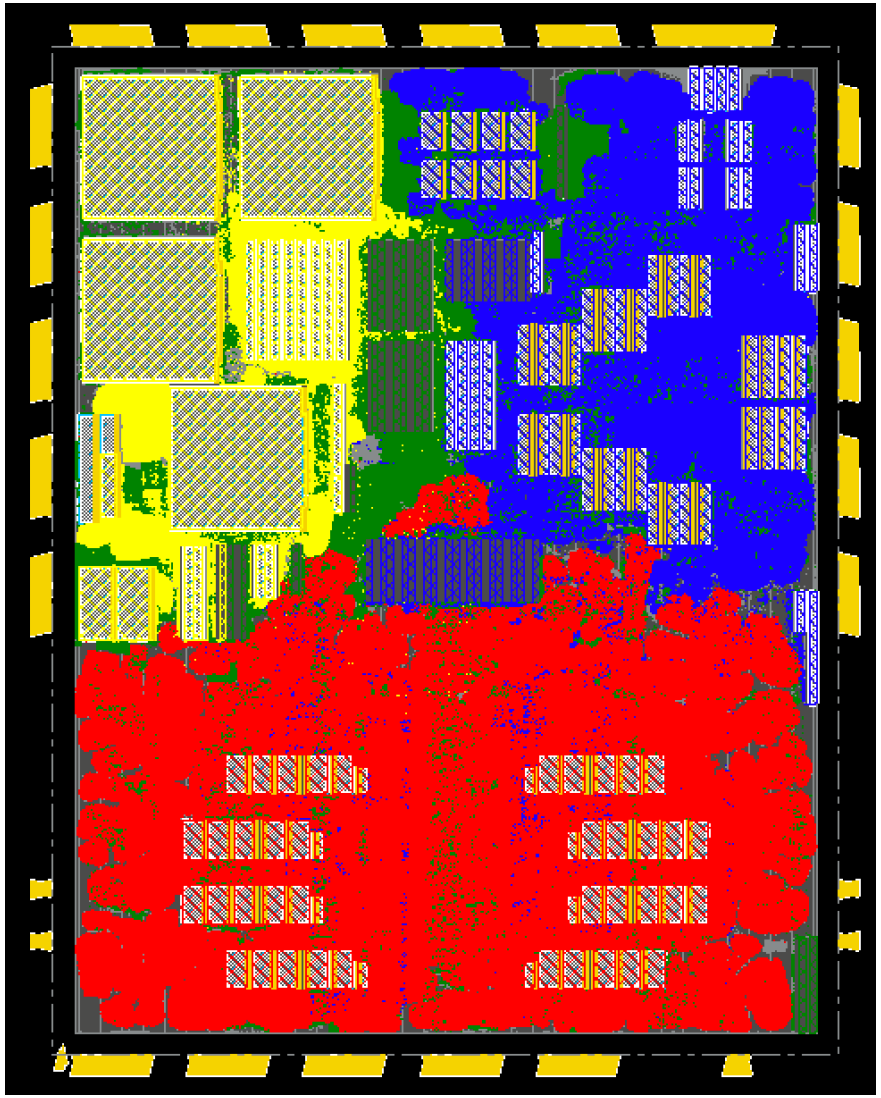
SOFTWARE

Automotive eHPC software support	Programming tools & Libraries
Low-level Software, Security, Power Management	
Linux Operating System	
EPI Processor and Reference Hardware	

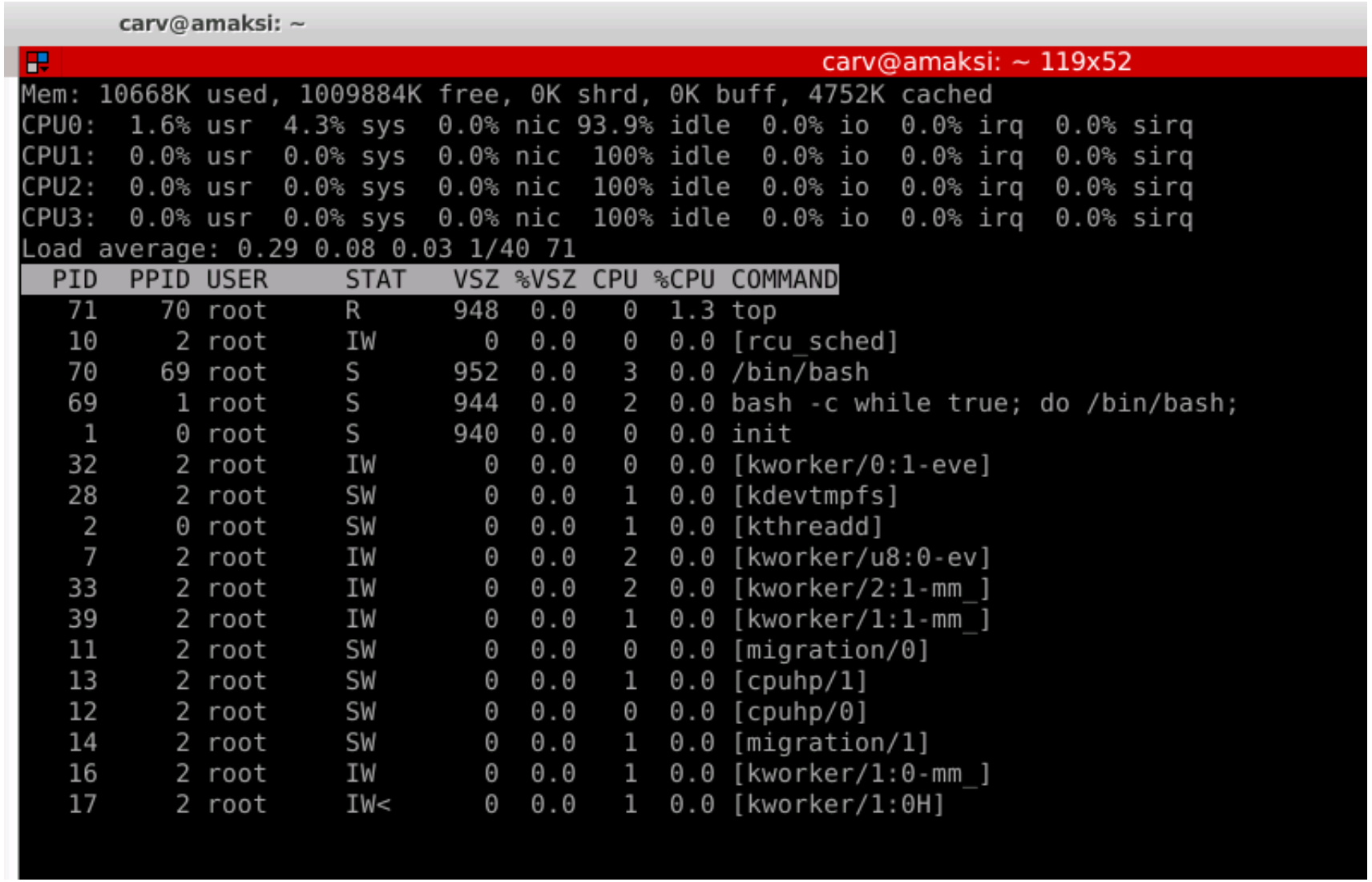


EPAC TEST CHIP

- Avispado processor core
- Vector Processing Unit (VPU)
- L2 cache and home node
- AMBA CHI cross-point



MULTICORE LINUX BOOT



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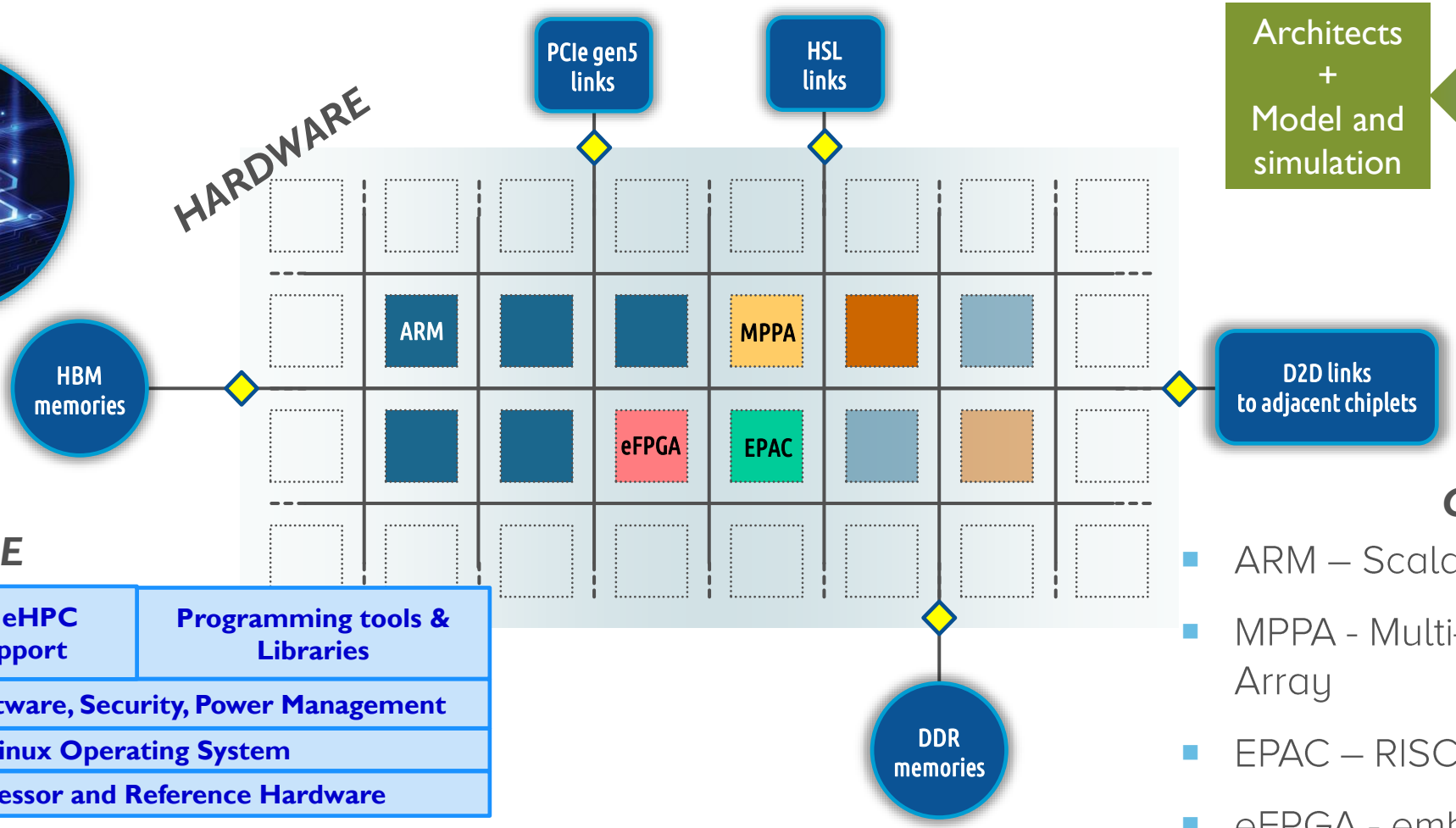
HARDWARE



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SDV & SYSTEM SOFTWARE PROGRESS

- SDV3.1
  - Run of a benchmark suite on top of Linux
  - Setup of a Continuous Integration environment to allow further RTL development
  - Run of STREAM and HPCG in preparation to the review
  - Refinement of a performance model to be integrated in MUSA to emulate SDV3.1 and EPAC
  - First touch with performance counters @ Avispado

EPI ROADMAP

EPI ROADMAP

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CONCLUSION

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- Future science, technologies and applications require processing of vast amount of data and there is a large need for efficient HPC
- HPC provides needed competitiveness for industry and society
- The expertise for developing high-end and complex processing units in Europe, after decades of dis-investment
- The European Processor Initiative aims to provide an EU HPC processor, accelerators and system/application design for exascale HPC systems in Europe and around the globe

www.european-processor-initiative.eu

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THANK YOU