SemiDynamics High Bandwidth Vector-capable RISC-V Cores

Roger Espasa, PhD

CEO

SemiDynamics

- European Based RISC-V IP Provider
  - HQ in Barcelona
  - Founded 2016
- Proud participant in the European Processor Initiative (EPI)
  - RISC-V Acceleration core supplied by SemiDynamics

Introducing 2 new RISC-V IP Cores

AVISPADO 220 

2-wide In-Order

Gazzillion Misses™

RISC-V Vector Support

ATREVIDO 220 

2-wide Out-of-Order

Gazzillion Misses™

RISC-V Vector Support

Available for licensing

What's a high bandwidth core?

A core with lots of outstanding memory requests

A core with Gazzillion Misses™

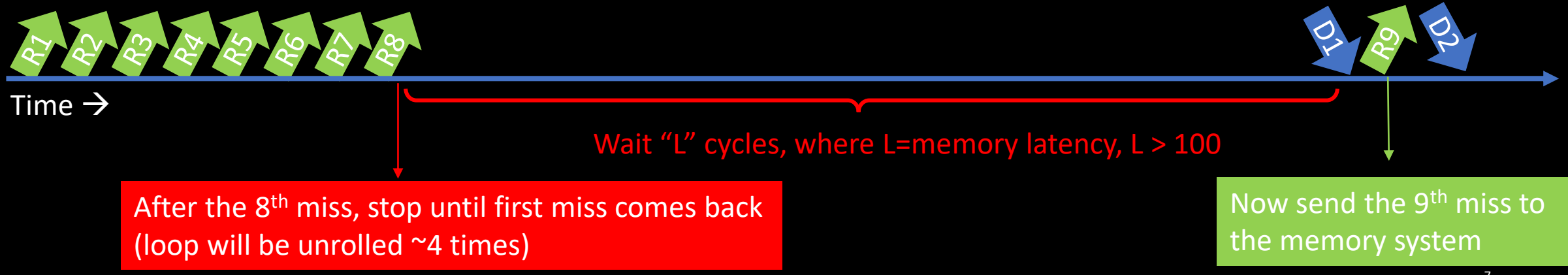
Example: Gathering Sparse Data with 8 outstanding requests

Original Program

```
while ( condition )
    load  a[index[i]]
    load  b[i]
    compute
    store c[i]
```

Stylized Assembly Code

```
top:
    load  index[i] -> x5
    load  (x5) -> x6
    load  b[i] -> x7
    compute x6, x7 -> x8
    store x8 -> c[i]
    loop to top
```



Example: Gathering Sparse Data with *Gazzillion Misses™*

Original Program

```
while ( condition )
    load  a[index[i]]
    load  b[i]
    compute
    store c[i]
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Stylized Assembly Code

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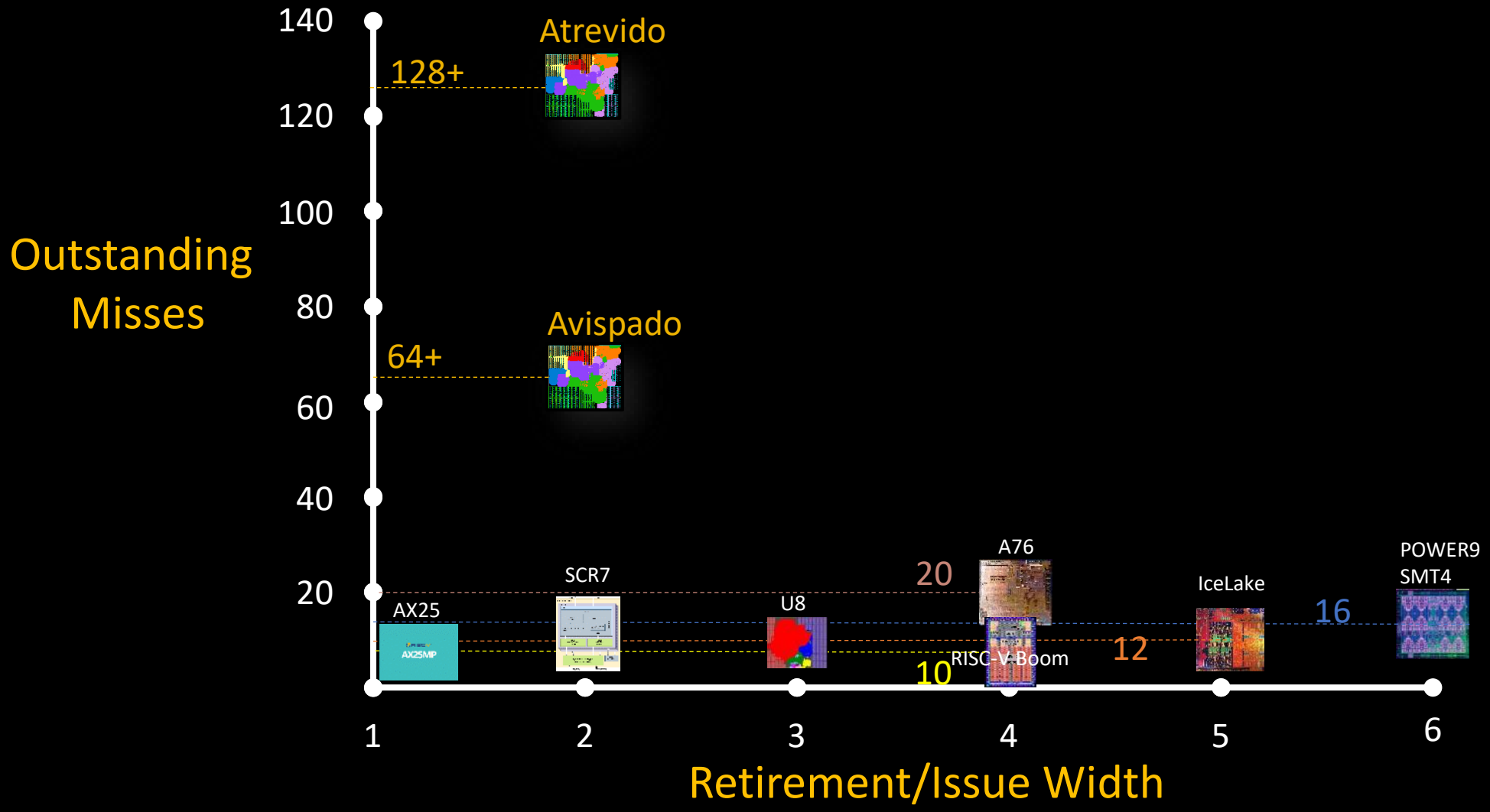
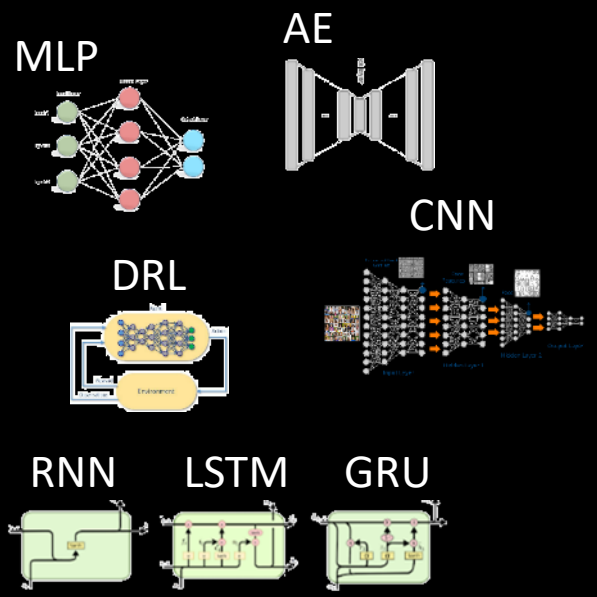
Comparison to other cores



Gazzillion Misses™ good for…

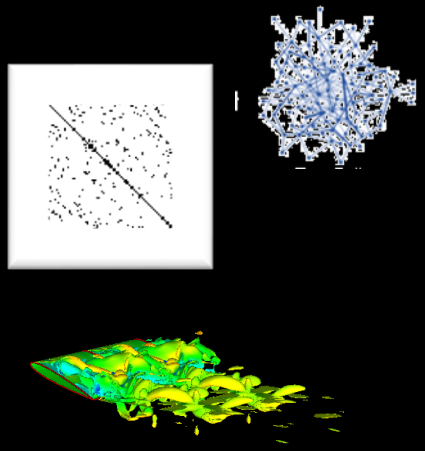
Machine Learning

Recommendation Systems



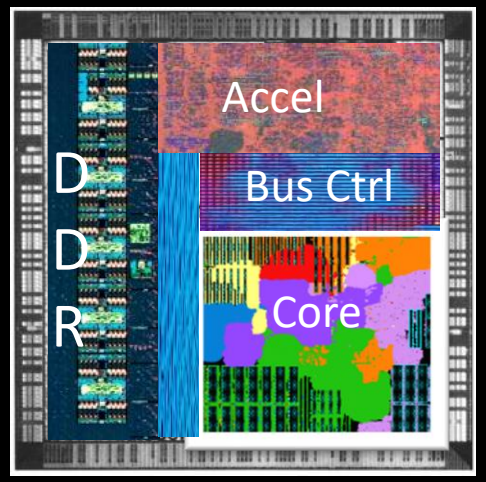
Key-Value Stores

Sparse Data / HPC

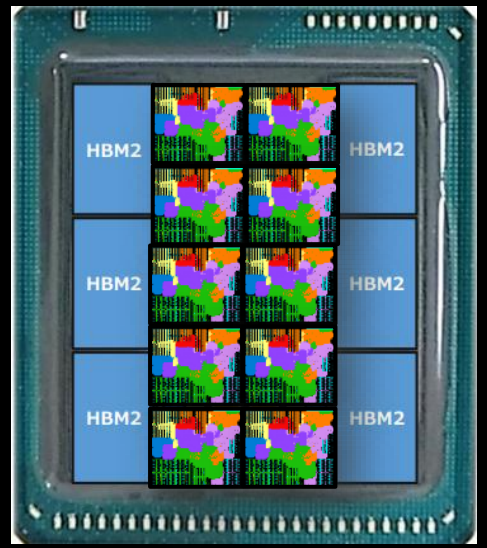


Gazzillion Misses™ good for SoCs...

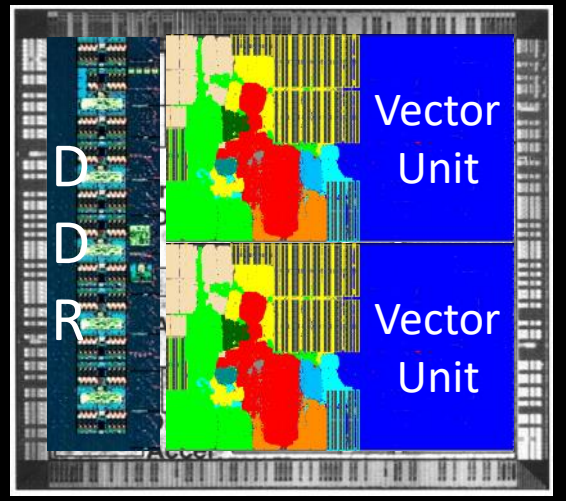
With Limited SRAM/Cache



High Bandwidth/ Streaming



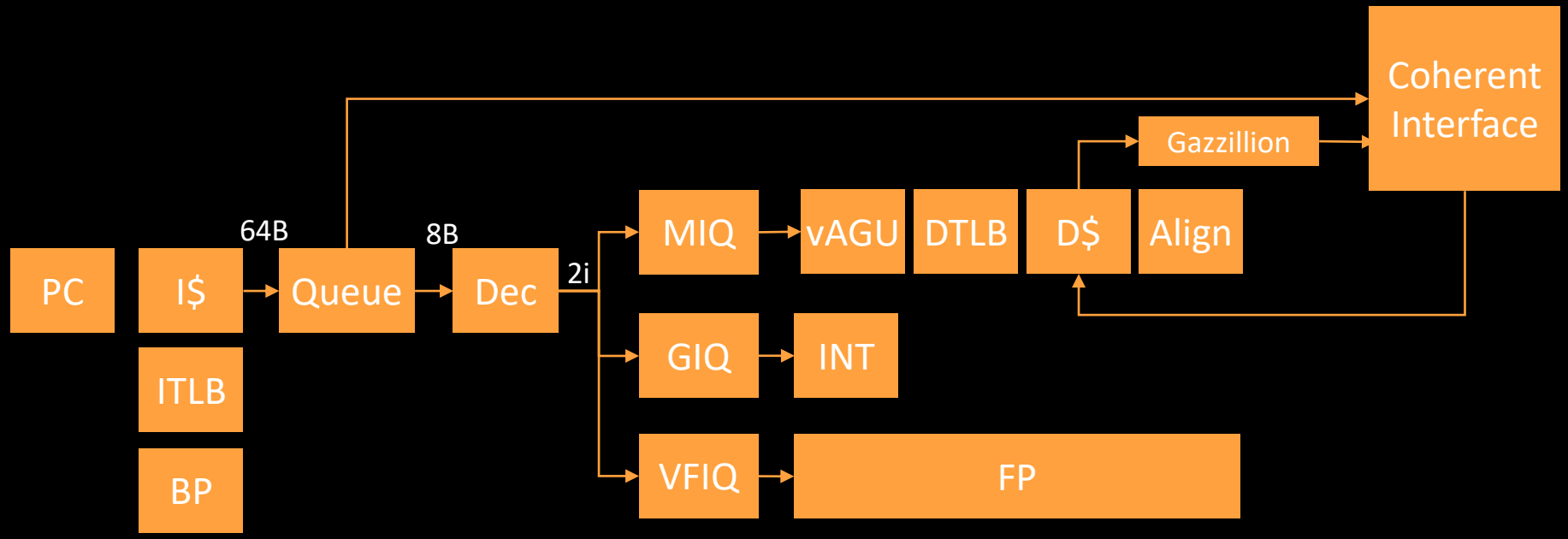
With Vector Units



Avispado Core Details

AVISPADO 220

RISCV64GCV



- SV48
- 16KB I$
- Decodes upcoming V1.0 vector spec
- 32KB D$
- Full hardware support for unaligned accesses
- Coherent (TL, ACE, CHI)

Available for licensing

Customizable upon request

- Cache Size / Associativity
- Coherent Interface
- In-flight instructions

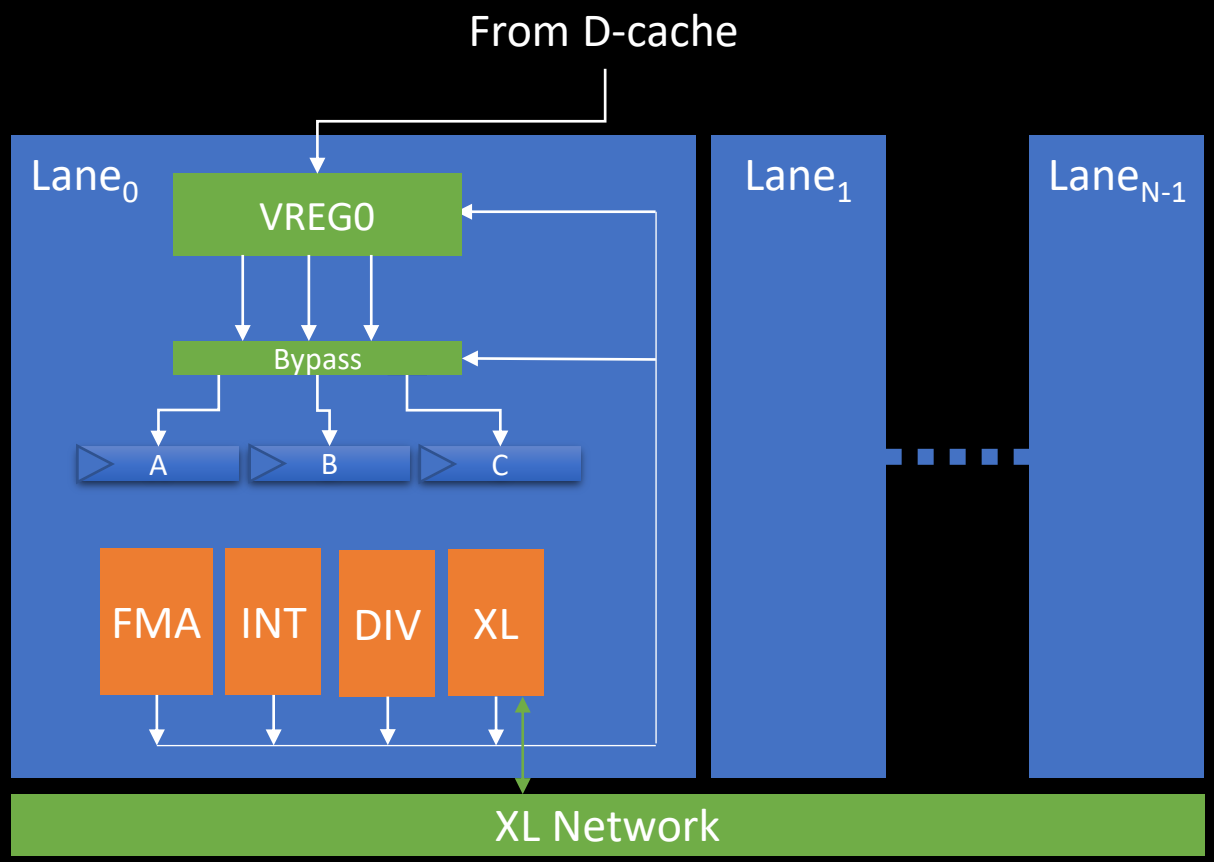
Introducing SemiDynamics' RISC-V Vector Processing Unit

SemiDynamics' VPU

- Implements the RISC-V Vector 1.0 Specification
  - Including lmul, segmented loads
  - No vector atomics currently
- Ready for OOO support
  - Renaming
- Customizable settings
  - VLEN = vreg size = from 128b to 4096b
  - Data path width = from 128b to 512b
  - Fast cross-lane network for slide/rgather/compress/expand

Available for licensing 3 months after V-spec freeze

VPU Block Diagram

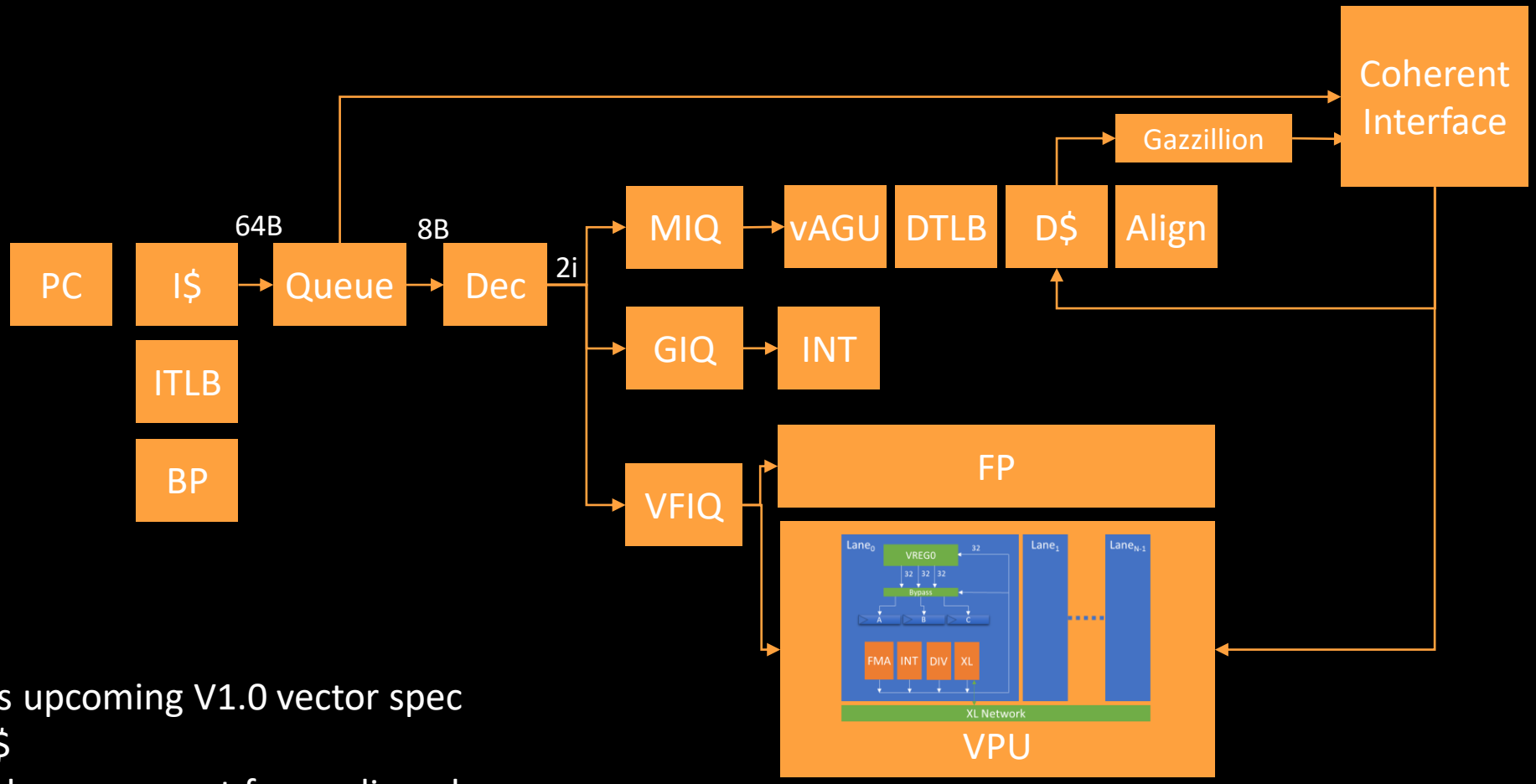


- Lane based organization
- Full cache-line bus from D-cache
- Units per lane
  - FMA
  - INT
  - DIV
  - XL: Cross-lane (rgather, …)
- Full masking support

Available for licensing 3 months after V-spec freeze

AVISPADO 220 with VPU

RISCV64GCV



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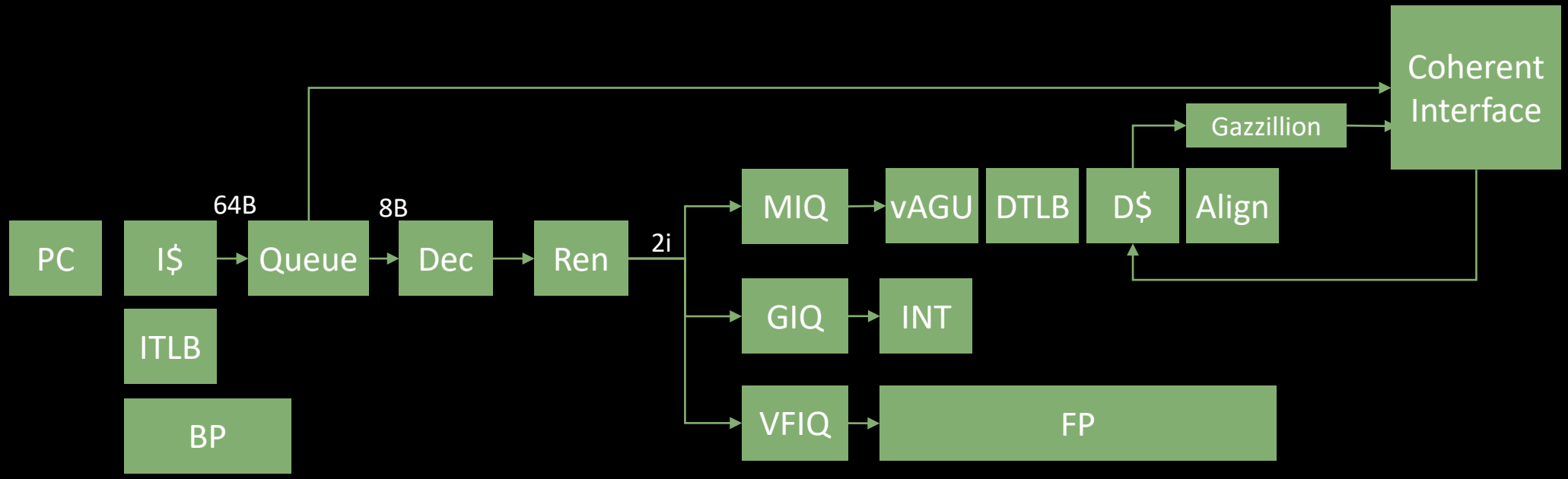
- Coherent (TL, ACE, CHI)
- Vector Memory (vle, vlse, vlxe, vse, …) processed by MIQ/LSU

Available for licensing 3 months after V-spec freeze

Atrevido Core Details

ATREVIDO 220

RISCV64GCV



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- 32KB D$
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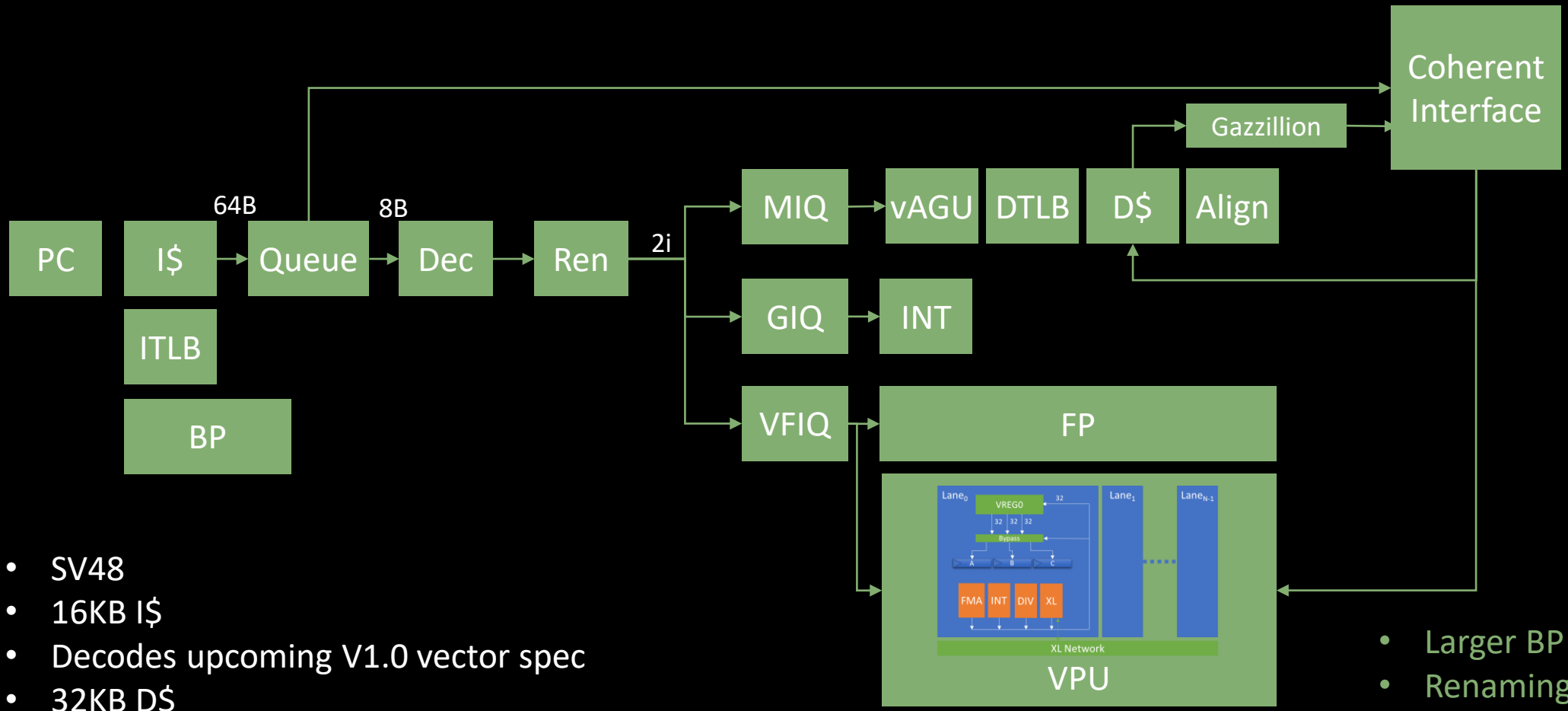
- Coherent (TL, ACE, CHI)

- Larger BP
- Renaming
- Retirement Logic

Available for licensing

ATREVIDO 220 with VPU

RISCV64GCV



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Summary

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VPU 1.0

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2-wide Out-of-Order

Gazzillion Misses™

VPU 1.0

IP cores available for licensing

Thank you!

www.semidynamics.com

info@semidynamics.com