RISC-V at Barcelona Supercomputing Center

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Outline

1. European Processor Initiative (EPI)
    - RISC-V vector processor design, LLVM compiler, test chip
2. MareNostrum Experimental Exascale Platform (MEEP)
    - Multi-FPGA architecture evaluation, software stack development
3. Cavatools
    - Open-source software RISC-V simulator for large applications

There are more projects not covered in this talk

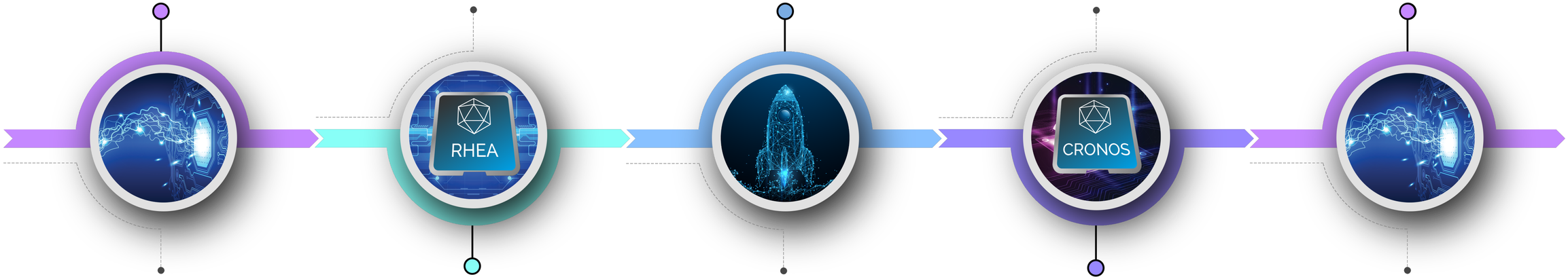
EPI Program Roadmap

EPI Phase 1

EPAC RISC-V Test Chip
EPAC Test Platform

Automotive PoC

2021



2022

Rhea Family - Gen1 GPP

EPI Common Platform
Arm & RISC-V
V1 Core – N6
External IPs

Rhea Platform

EPI IPs Launch Pad

2022-2023

2023-2024

Cronos Family - Gen2 GPP

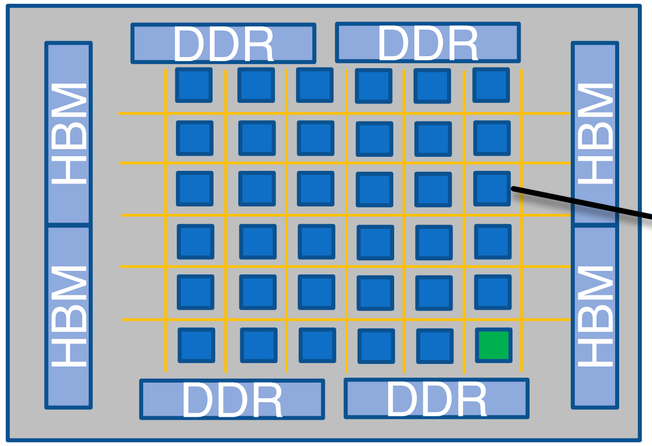
EPI Common Platform
Arm & RISC-V
Titan Acc

EU Advanced HPC Pilots

Gen3 GPP Family

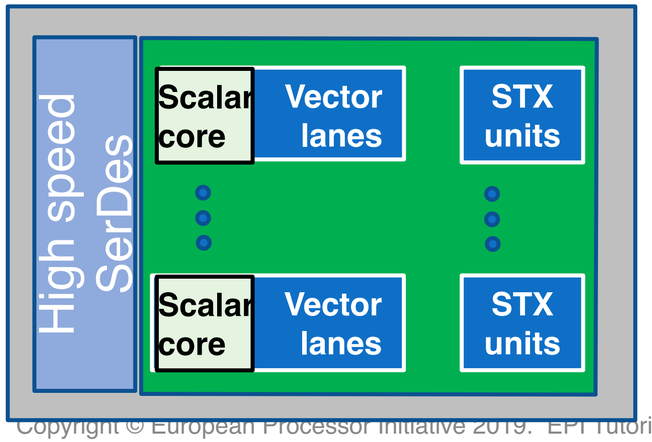
2024-...

1ST GENERATION EPI CHIPS



General Purpose Processor (GPP) chip

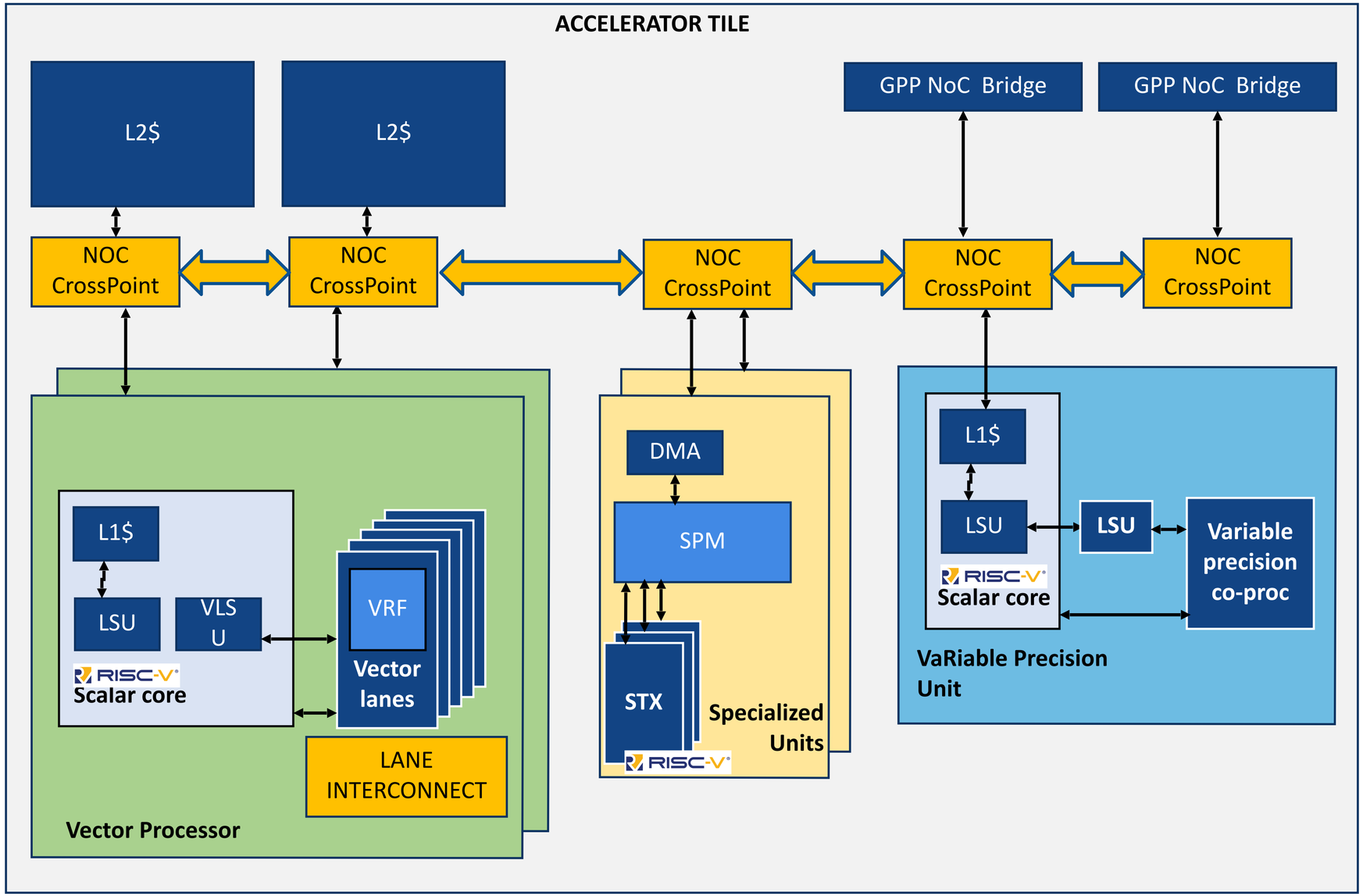
- 6 nm, chip-let technology
- **ARM-SVE** tiles
- L1, L2, L3 cache subsystem + HBM + DDR



RISC-V Accelerator Demonstrator Test Chip

- 22 nm FDSOI
- Only one RISC-V accelerator tile
- On-chip L1, L2 + off-chip HBM + DDR PHY
- Targets 16 DP GFLOPS per core (vector processor only)

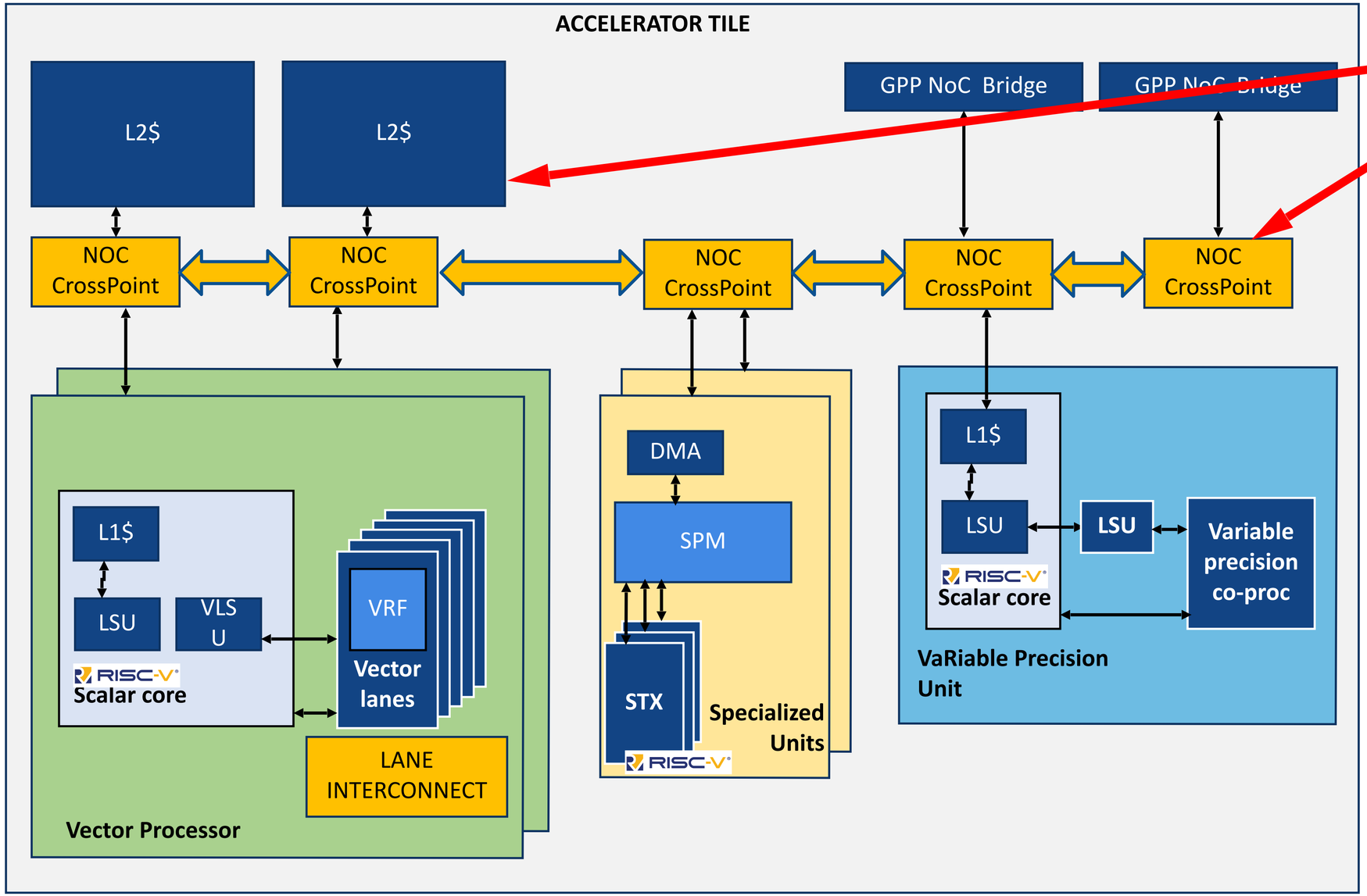
EPAC ARCHITECTURE VIEW



CONTRIBUTING PARTNERS:

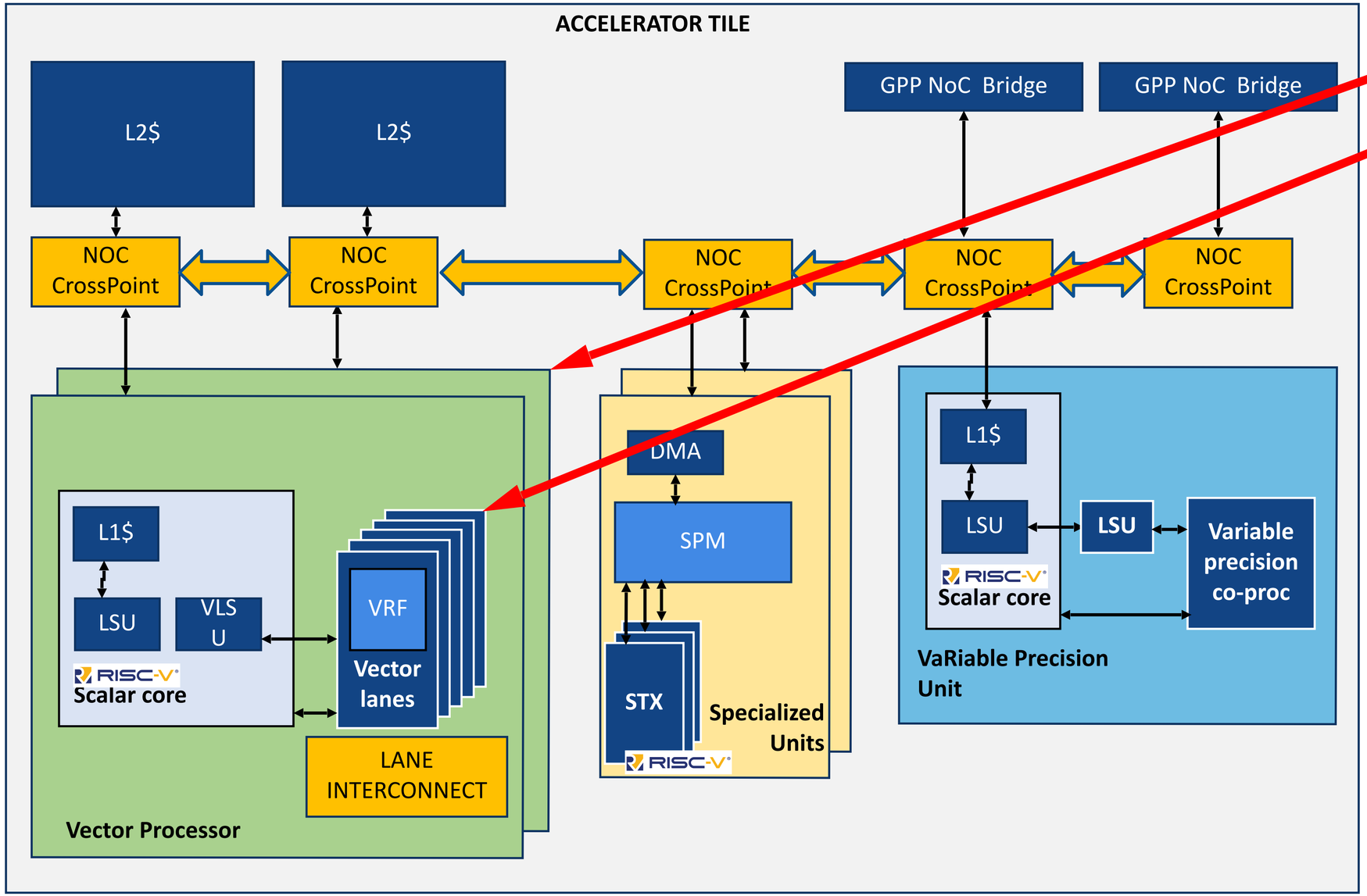
- BSC
- CEA
- Chalmers
- E4
- ETH Zurich
- Extoll
- FORTH
- Fraunhofer
- Semidynamics

EPAC ARCHITECTURE VIEW



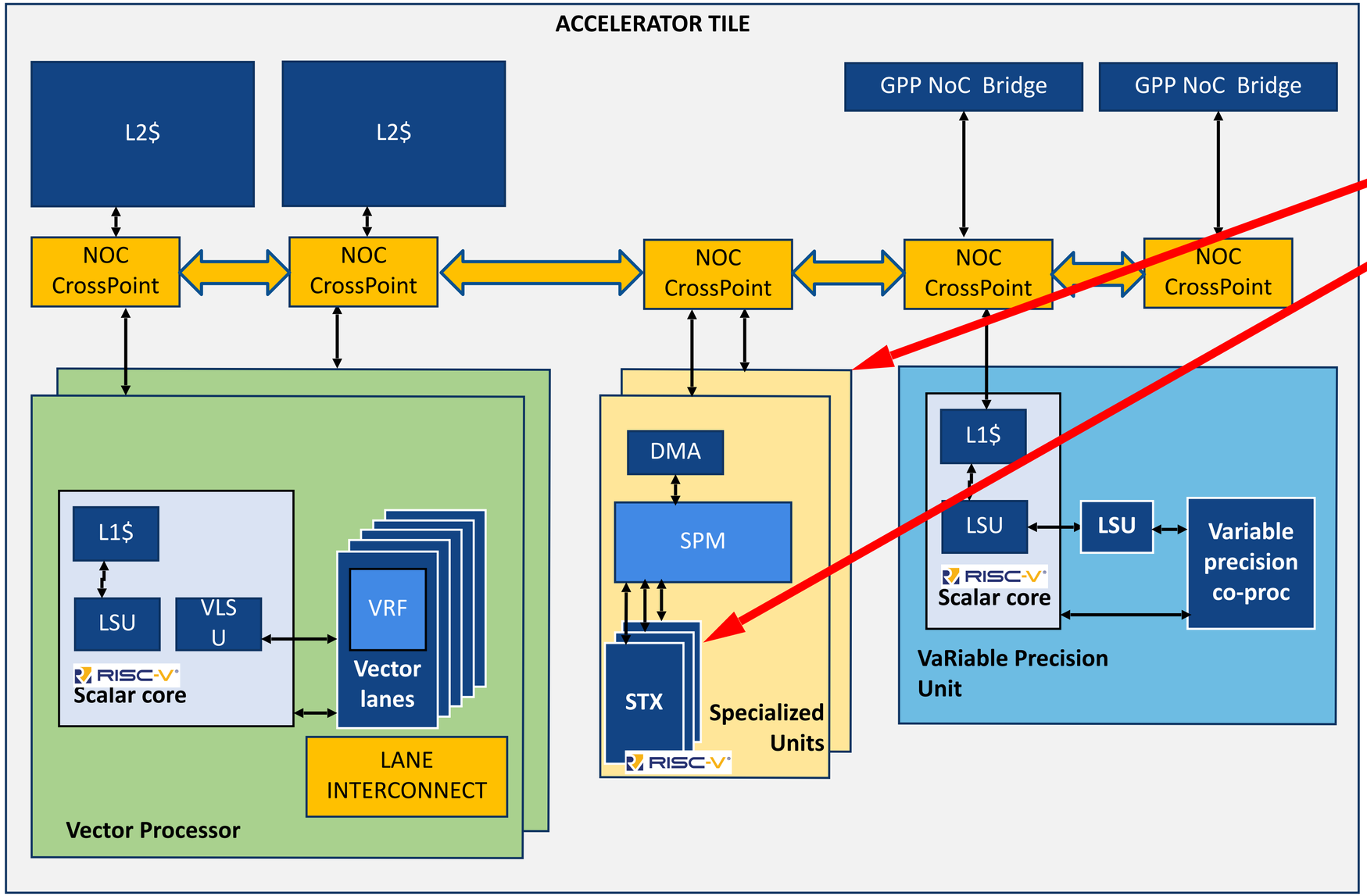
- Shared L2 cache banks
- Cache coherent NoC

EPAC ARCHITECTURE VIEW



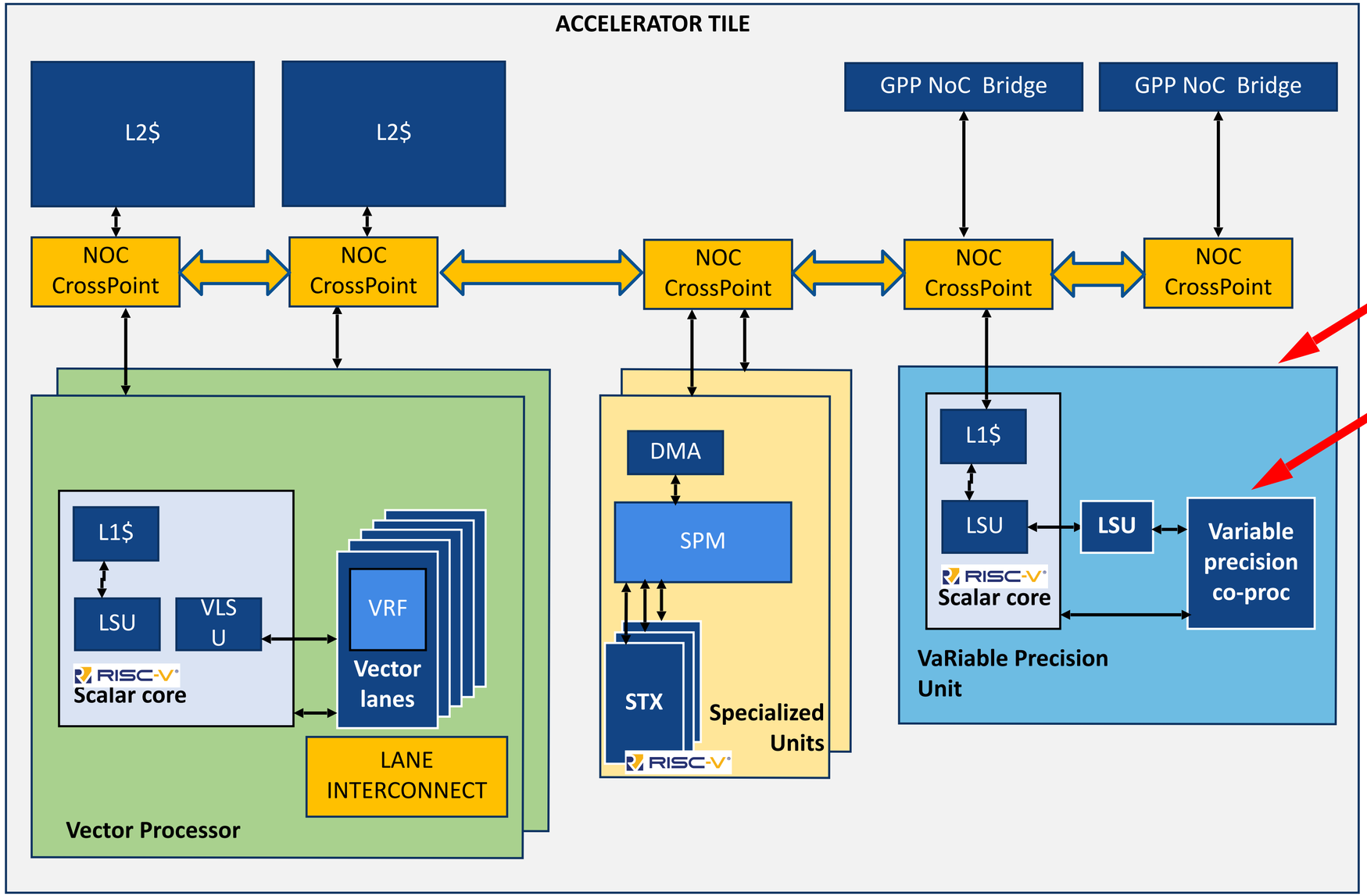
- Up to 8 vector processors
- Vector Lanes act as tightly coupled (ISA mapped) acceleration units to the scalar core in the vector processor
- Heavily pipelined
- RISC-V vector extension compliant

EPAC ARCHITECTURE VIEW



- Up to 8 Specialized Units
- The STX Units act as loosely coupled, memory mapped acceleration units to the scalar cores
- Fast single-cycle MACs in parallel

EPAC ARCHITECTURE VIEW

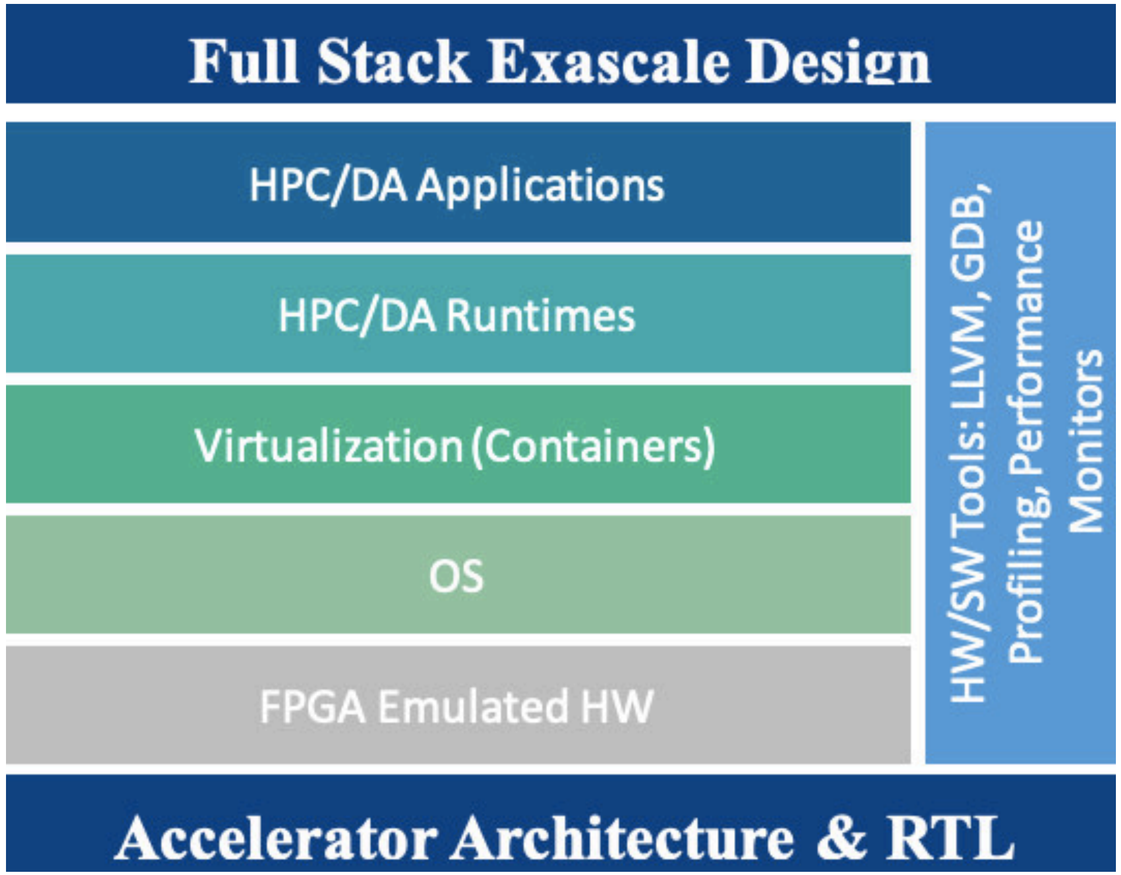


- At least one Variable Precision unit
- The variable precision co-processor act as execution unit extension to the scalar core

MEEP

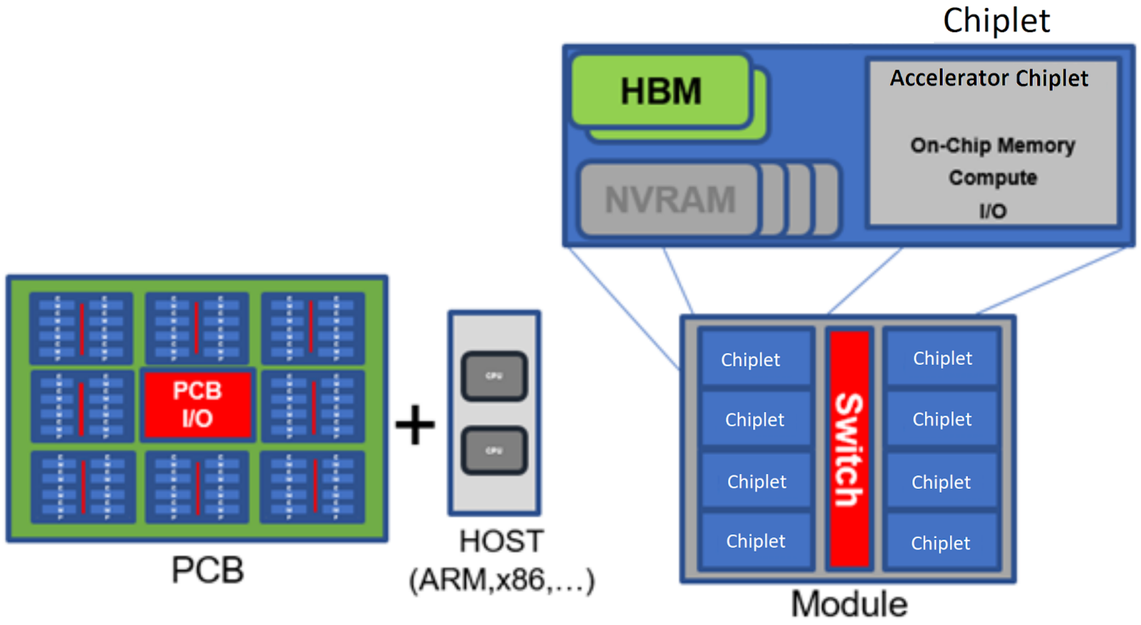
Formerly the European Exascale Accelerator Project

- FPGA infrastructure for rapid hardware architecture evaluation
- Vehicle for interactive development of software stack at reasonable speed
- Digital laboratory for hardware-software co-design, testing and evaluating future exascale accelerators and systems



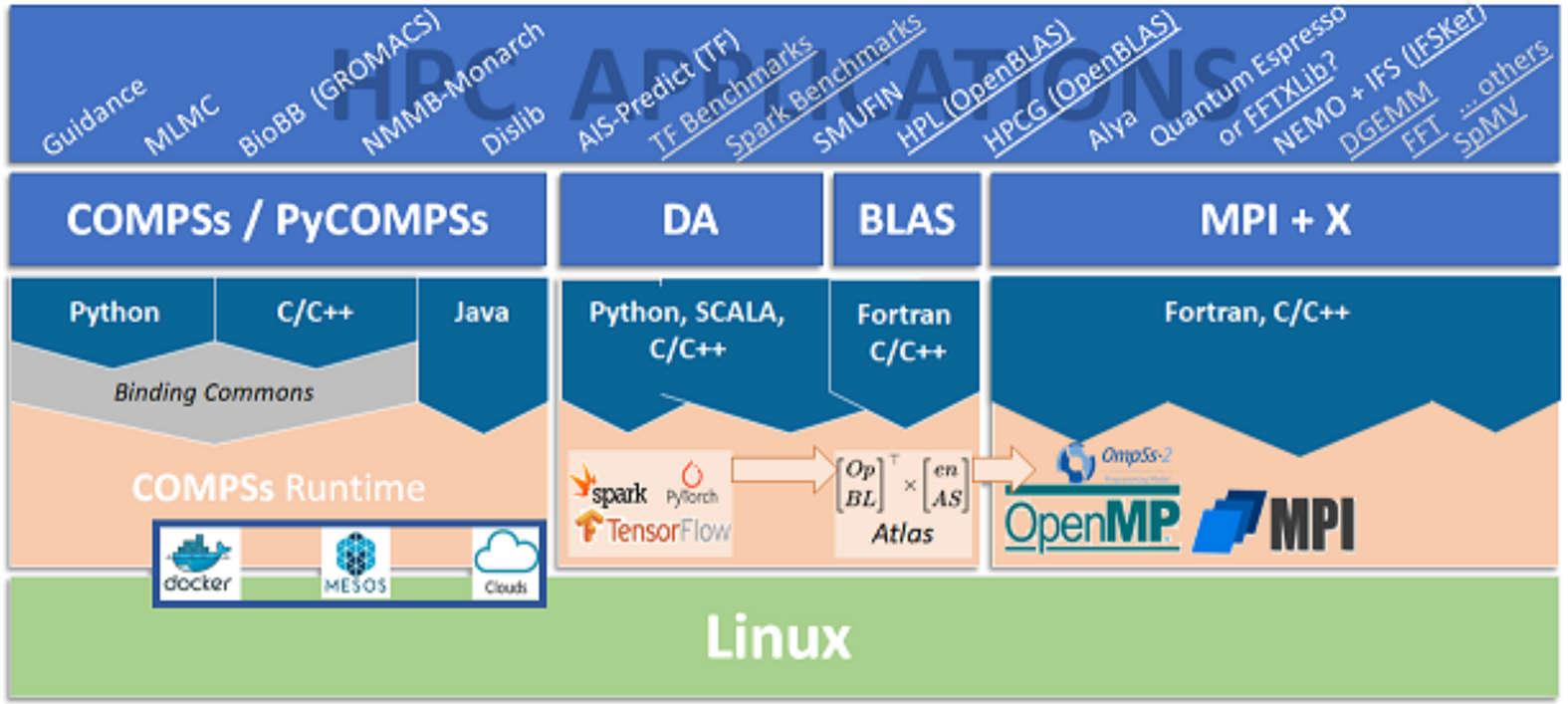
FPGA Platform

- FPGA with HBM models accelerator chip
  - Reduced number of cores/vector lanes
  - Lower clock speed
- Module/PCB structure models real system
  - Fewer cores/chiplets/modules
  - Time-shared communication channels
- Reasonable functional approximation of real system running at 1-10% real time



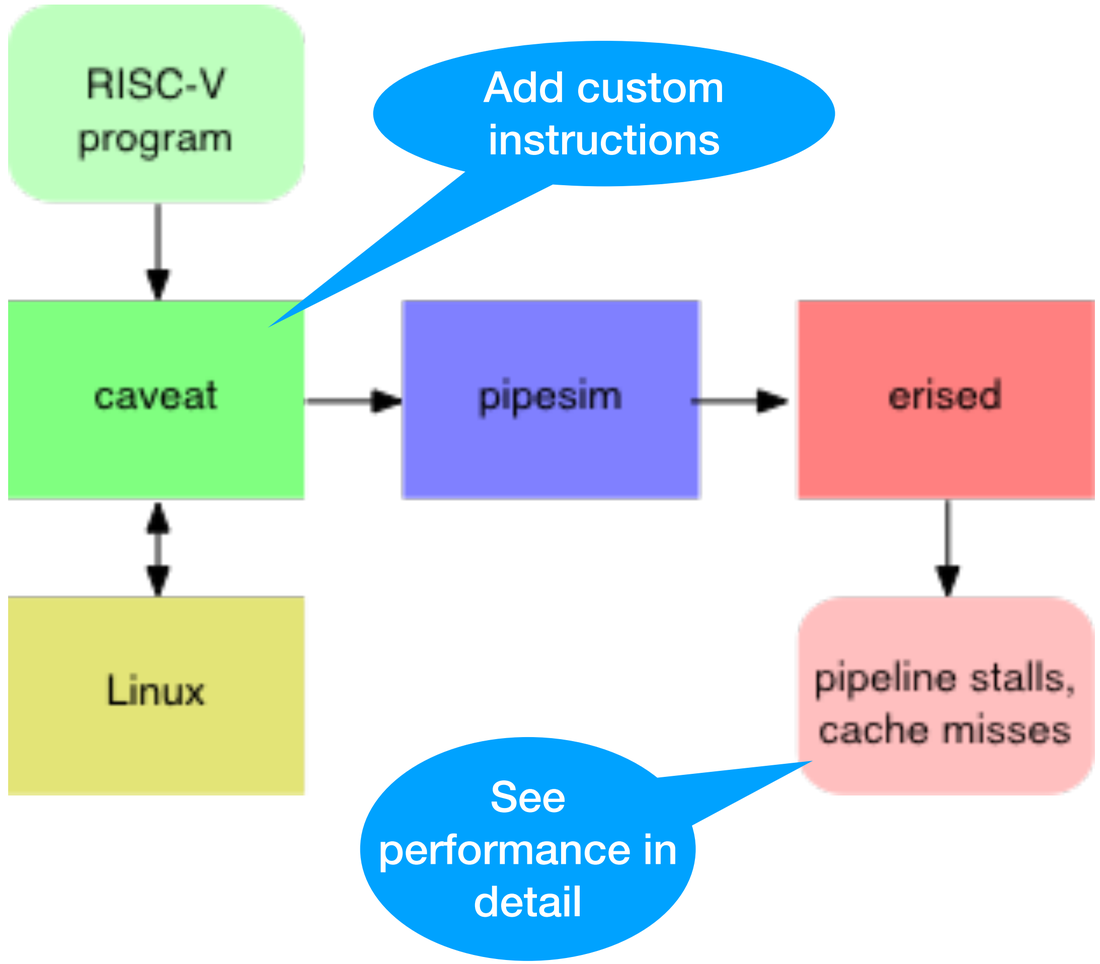
Software Stacks

- Real ecosystem based on MareNostrum supercomputer @ BSC
- FPGA platform for software development
- Co-design compiler/ runtime and hardware architecture
- Full system performance evaluation using real HPC applications

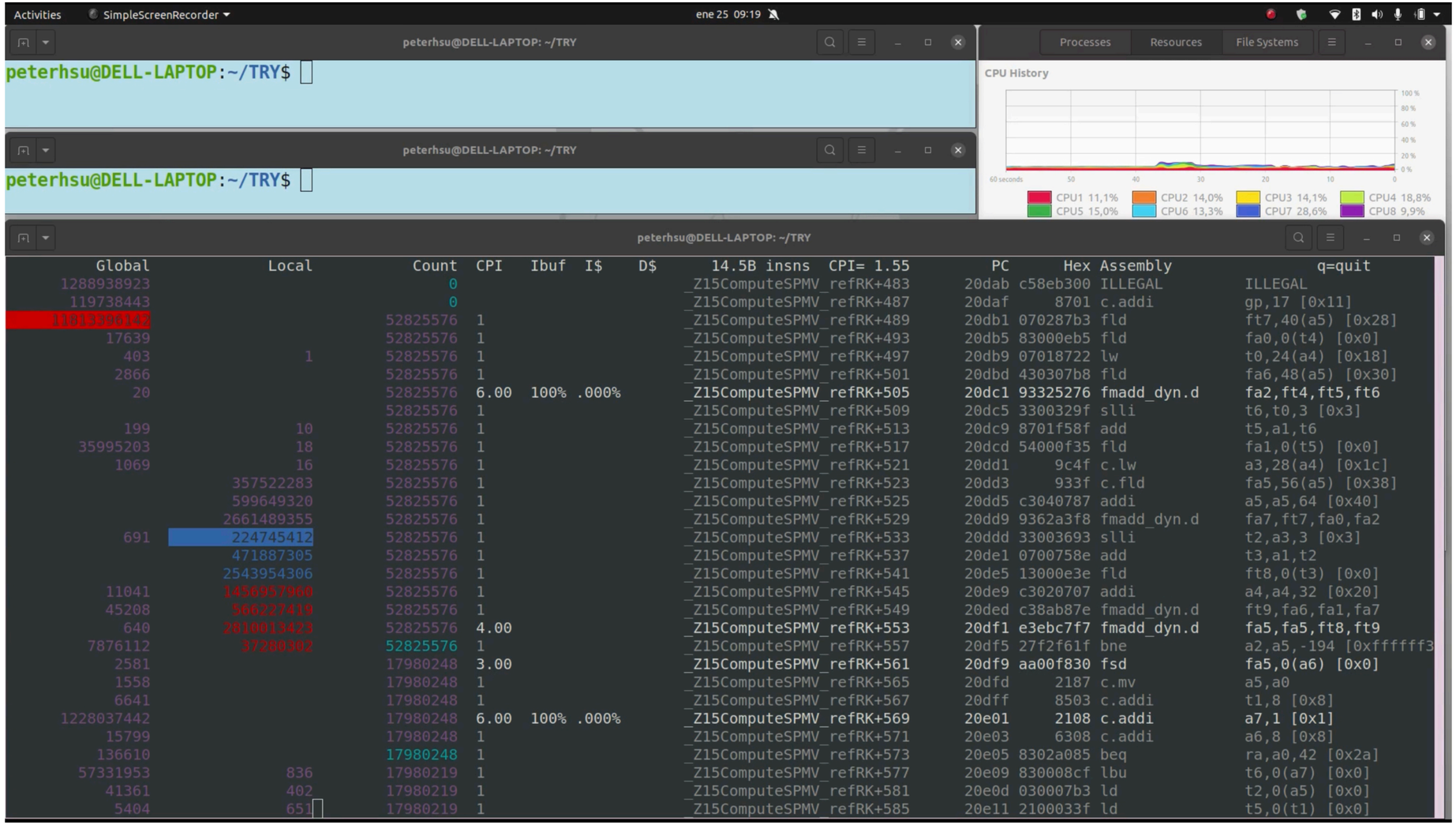


Cavatools

- Software simulation toolkit for performance analysis of real applications
  - Virtual RISC-V Linux machine
  - Execution-driven pipeline simulator
  - Real-time noninvasive viewer for instruction-level stalls, cache misses
- Fast enough to evaluate new architecture running large production programs
  - 100+ MIPS on 4-core x86 laptop
- Open source



Demo Video


Activities
SimpleScreenRecorder
ene 25 09:19
peterhsu@DELL-LAPTOP: ~/TRY
peterhsu@DELL-LAPTOP:~/TRY$
peterhsu@DELL-LAPTOP: ~/TRY
peterhsu@DELL-LAPTOP:~/TRY$
Processes
Resources
File Systems
CPU History
CPU1 11,1%
CPU2 14,0%
CPU3 14,1%
CPU4 18,8%
CPU5 15,0%
CPU6 13,3%
CPU7 28,6%
CPU8 9,9%
peterhsu@DELL-LAPTOP: ~/TRY
Global Local Count CPI Ibuf I$ D$ 14.5B insns CPI= 1.55 PC Hex Assembly q=quit
1288938923 0 _Z15ComputeSPMV_refRK+483 20dab c58eb300 ILLEGAL ILLEGAL
119738443 0 _Z15ComputeSPMV_refRK+487 20daf 8701 c.addi gp,17 [0x11]
1101398143 52825576 1 _Z15ComputeSPMV_refRK+489 20db1 070287b3 fld ft7,40(a5) [0x28]
17639 52825576 1 _Z15ComputeSPMV_refRK+493 20db5 83000eb5 fld fa0,0(t4) [0x0]
403 1 52825576 1 _Z15ComputeSPMV_refRK+497 20db9 07018722 lw t0,24(a4) [0x18]
2866 52825576 1 _Z15ComputeSPMV_refRK+501 20dbd 430307b8 fld fa6,48(a5) [0x30]
20 52825576 6.00 100% .000% _Z15ComputeSPMV_refRK+505 20dc1 93325276 fmadd_dyn.d fa2,ft4,ft5,ft6
52825576 1 _Z15ComputeSPMV_refRK+509 20dc5 3300329f slli t6,t0,3 [0x3]
199 10 52825576 1 _Z15ComputeSPMV_refRK+513 20dc9 8701f58f add t5,a1,t6
35995203 18 52825576 1 _Z15ComputeSPMV_refRK+517 20dcd 54000f35 fld fa1,0(t5) [0x0]
1069 16 52825576 1 _Z15ComputeSPMV_refRK+521 20dd1 9c4f c.lw a3,28(a4) [0x1c]
357522283 52825576 1 _Z15ComputeSPMV_refRK+523 20dd3 933f c.fld fa5,56(a5) [0x38]
599649320 52825576 1 _Z15ComputeSPMV_refRK+525 20dd5 c3040787 addi a5,a5,64 [0x40]
2661489355 52825576 1 _Z15ComputeSPMV_refRK+529 20dd9 9362a3f8 fmadd_dyn.d fa7,ft7,fa0,fa2
691 224745412 52825576 1 _Z15ComputeSPMV_refRK+533 20ddd 33003693 slli t2,a3,3 [0x3]
471887305 52825576 1 _Z15ComputeSPMV_refRK+537 20de1 0700758e add t3,a1,t2
2543954306 52825576 1 _Z15ComputeSPMV_refRK+541 20de5 13000e3e fld ft8,0(t3) [0x0]
11041 1456957960 52825576 1 _Z15ComputeSPMV_refRK+545 20de9 c3020707 addi a4,a4,32 [0x20]
45208 566227419 52825576 1 _Z15ComputeSPMV_refRK+549 20ded c38ab87e fmadd_dyn.d ft9,fa6,fa1,fa7
640 2810013423 52825576 4.00 _Z15ComputeSPMV_refRK+553 20df1 e3ebc7f7 fmadd_dyn.d fa5,fa5,ft8,ft9
7876112 37280302 52825576 1 _Z15ComputeSPMV_refRK+557 20df5 27f2f61f bne a2,a5,-194 [0xffffff3
2581 17980248 3.00 _Z15ComputeSPMV_refRK+561 20df9 aa00f830 fsd fa5,0(a6) [0x0]
1558 17980248 1 _Z15ComputeSPMV_refRK+565 20dfd 2187 c.mv a5,a0
6641 17980248 1 _Z15ComputeSPMV_refRK+567 20dff 8503 c.addi t1,8 [0x8]
1228037442 17980248 6.00 100% .000% _Z15ComputeSPMV_refRK+569 20e01 2108 c.addi a7,1 [0x1]
15799 17980248 1 _Z15ComputeSPMV_refRK+571 20e03 6308 c.addi a6,8 [0x8]
136610 17980248 1 _Z15ComputeSPMV_refRK+573 20e05 8302a085 beq ra,a0,42 [0x2a]
57331953 836 17980219 1 _Z15ComputeSPMV_refRK+577 20e09 830008cf lbu t6,0(a7) [0x0]
41361 402 17980219 1 _Z15ComputeSPMV_refRK+581 20e0d 030007b3 ld t2,0(a5) [0x0]
5404 651 17980219 1 _Z15ComputeSPMV_refRK+585 20e11 2100033f ld t5,0(t1) [0x0]

Conclusion

- RISC-V accelerator and supercomputing projects at BSC
  - EPI — classical vector processor design with “V” instructions
  - MEEP — FPGA emulation platform for RISC-V HPC systems
  - Cavatools — software simulator for co-design evaluation of custom instruction extensions on real applications
- More RISC-V projects not presented
  - Visit www.bsc.es

Peter Hsu is a senior researcher at Barcelona Supercomputing Center (BSC) and has a consulting business Peter Hsu & Associates S.L.U. in Barcelona, Spain. He was formerly director of the European Exascale Accelerator Project at BSC. Peter has worked in the United States at Oracle Research Labs, Toshiba America, Silicon Graphics, Sun Microsystems and IBM Research. He co-founded ArtX, design firm for Nintendo GameCube graphics chip, since acquired by ATI/AMD. He was architect of the MIPS R8000 TFP microprocessor in the Silicon Graphics Power Challenge supercomputers. Dr. Hsu received his degree from the University of Illinois, Urbana-Champaign. He was visiting scholar at EPFL University in Switzerland, and the University of Wisconsin at Madison.