

# EUROPEAN PROCESSOR INITIATIVE TUTORIAL

HIPEAC 2021

VIRTUAL EVENT

18 JANUARY 2021



European  
Processor  
Initiative



# FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES



THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION'S HORIZON 2020 RESEARCH AND INNOVATION PROGRAMME UNDER GRANT AGREEMENT NO 826647



# EPI OVERVIEW AND INTRODUCTION TO TUTORIAL TOPICS

DENIS DUTOIT (CEA)



# EPI OVERVIEW

# 56<sup>TH</sup> EDITION OF THE TOP500 LIST (NOVEMBER 2020)

	NOVEMBER 2020	SYSTEM	SPECS	SITE	COUNTRY	CORES	RMAX PFLOP/S	POWER MW
1	Fugaku	Fujitsu A64FX (48C, 2.2GHz), Tofu Interconnect D		RIKEN R-CCS	Japan	7,630,848	442.0	29.9
2	Summit	IBM POWER9 (22C, 3.07GHz), NVIDIA Volta GV100 (80C), Dual-Rail Mellanox EDR Infiniband		DOE/SC/ORN	USA	2,414,592	148.6	10.1
3	Sierra	IBM POWER9 (22C, 3.1GHz), NVIDIA Tesla V100 (80C), Dual-Rail Mellanox EDR Infiniband		DOE/NNSA/LLNL	USA	1,572,480	94.6	7.44
4	Sunway TaihuLight	Shenwei SW26010 (260C, 1.45 GHz) Custom Interconnect		NSCC in Wuxi	China	10,649,600	93.0	15.4
5	Selene	NVIDIA DGX A100, AMD EPYC 7742 (64C, 2.25GHz), NVIDIA A100, Mellanox HDR Infiniband		NVIDIA Corporation	USA	555,520	63.4	2.65

- Top#1 performance today:
  - 0.4 10<sup>18</sup> Flop/s Peak
  - It is 2half 1/5 of Exascale level of performance

## ■ Users:

#1: Japan











#2-3: US



#4: China



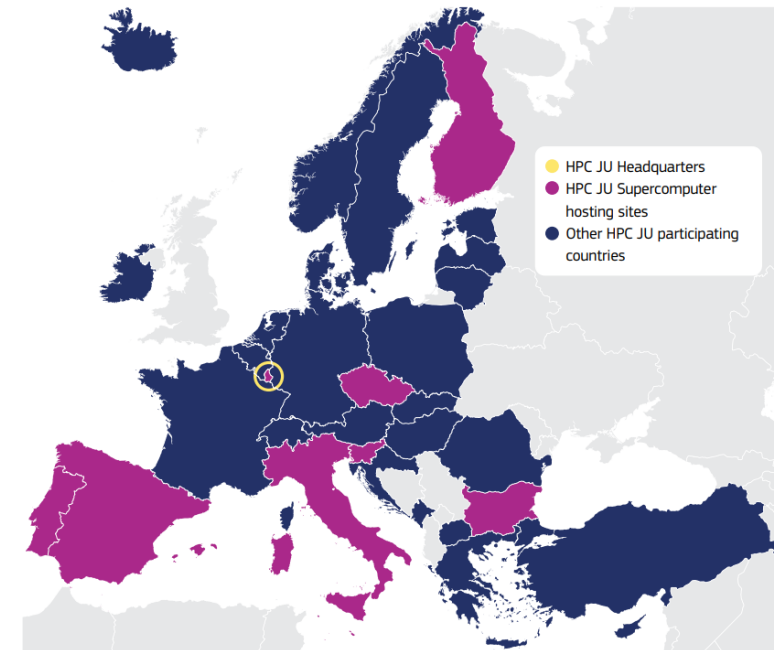
Chip	Design	Manuf.
Fujitsu A64FX		
IBM POWER9		
NVIDIA Volta GV100		
Sunway SW26010		

Japan is back, and Europe ?

How to bring back Europe into processor race ?

# EU EXASCALE HPC STRATEGY

- March 2017, Rome: EC launched the *EuroHPC declaration*
- November 2018, EuroHPC Joint Undertaking, a 1 billion Euro joint initiative between the EU and European countries to develop a World Class Supercomputing Ecosystem in Europe
- Oct 2020: 32 participating countries



## EUROPE'S AMBITION: EUROHPC

- Developing a new European supercomputing ecosystem: HPC systems, network, software, applications, access through the cloud
- Making HPC resources available to public and private users, including SMEs.
- Stimulating a technology supply industry



# DRIVERS OF THE EPI PROPOSAL

## Societal challenges

- Climate change
- Cybersecurity
- Increasing energy needs
- Intensifying global competition
- Aging population
- Sovereignty (data, economical, embargo)

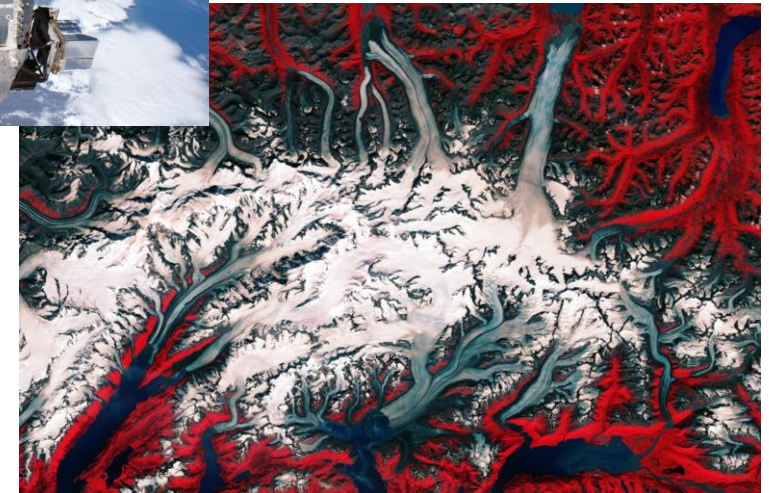


Image: <https://www.combiomed.eu/services/software-hub/>



# DRIVERS OF THE EPI PROPOSAL

- Connected mobility & *Autonomous Driving computing needs beyond 2023*
- Develop customized processors able to meet the performance needed for autonomous vehicles that would offer:
  - implementation of vehicle perception tasks in real-time in a fail-operational manner
  - increased computing performance, fail-operational, functional safety, cyber-security and real-time behaviour (RT)
  - compute resources with the same characteristics as their “big brothers” in exascale class supercomputers
- Sovereignty (data, economical, embargo)
- EU car manufacturing supremacy



# 27 PARTNERS FROM 10 EU COUNTRIES



# EPI OBJECTIVES

- Overall: Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments
  - Short-term objective
    - supply the EU-designed microprocessor to empower the EU Exascale machines
  - Long-term objective
    - Europe needs a sovereign (=not at risk of limitation or embargo by non-EU countries) access to high-performance, low-power microprocessors, from IP to products
  - EPI has been set to fulfil this objective
  - EPI has to cover all Technical Readiness levels (TRL)
    - TRL 1-3 are for long-term objectives (EU IP)
- \*and\*
- TRL 4-9 are for short to mid-term objectives (decade) with products designed in EU



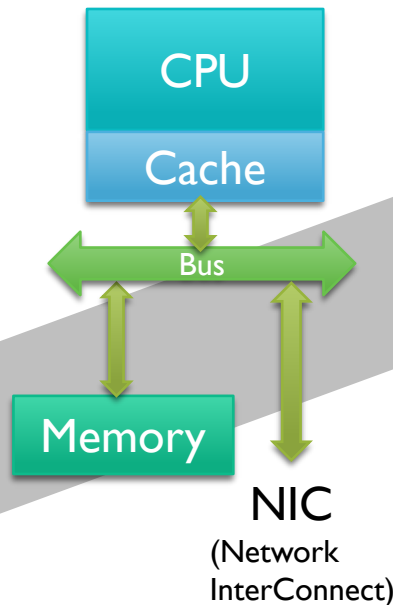


# EPI COMMON PLATFORM

SLIDES PREPARED BY SIPEARL, PRESENTED BY DENIS DUTOIT (CEA)

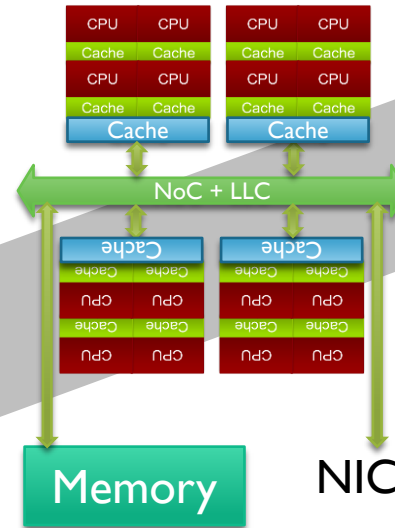
# COMPUTE NODE ARCHITECTURE EVOLUTION

## Mono-Core

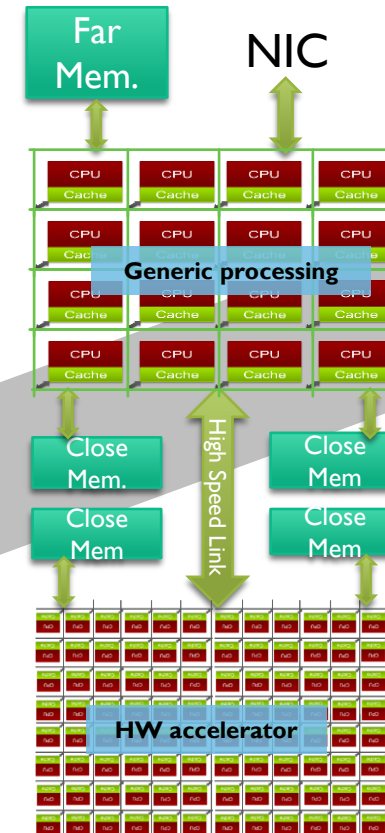


2005  
Frequency wall

## Multi-Core



2015  
Power wall

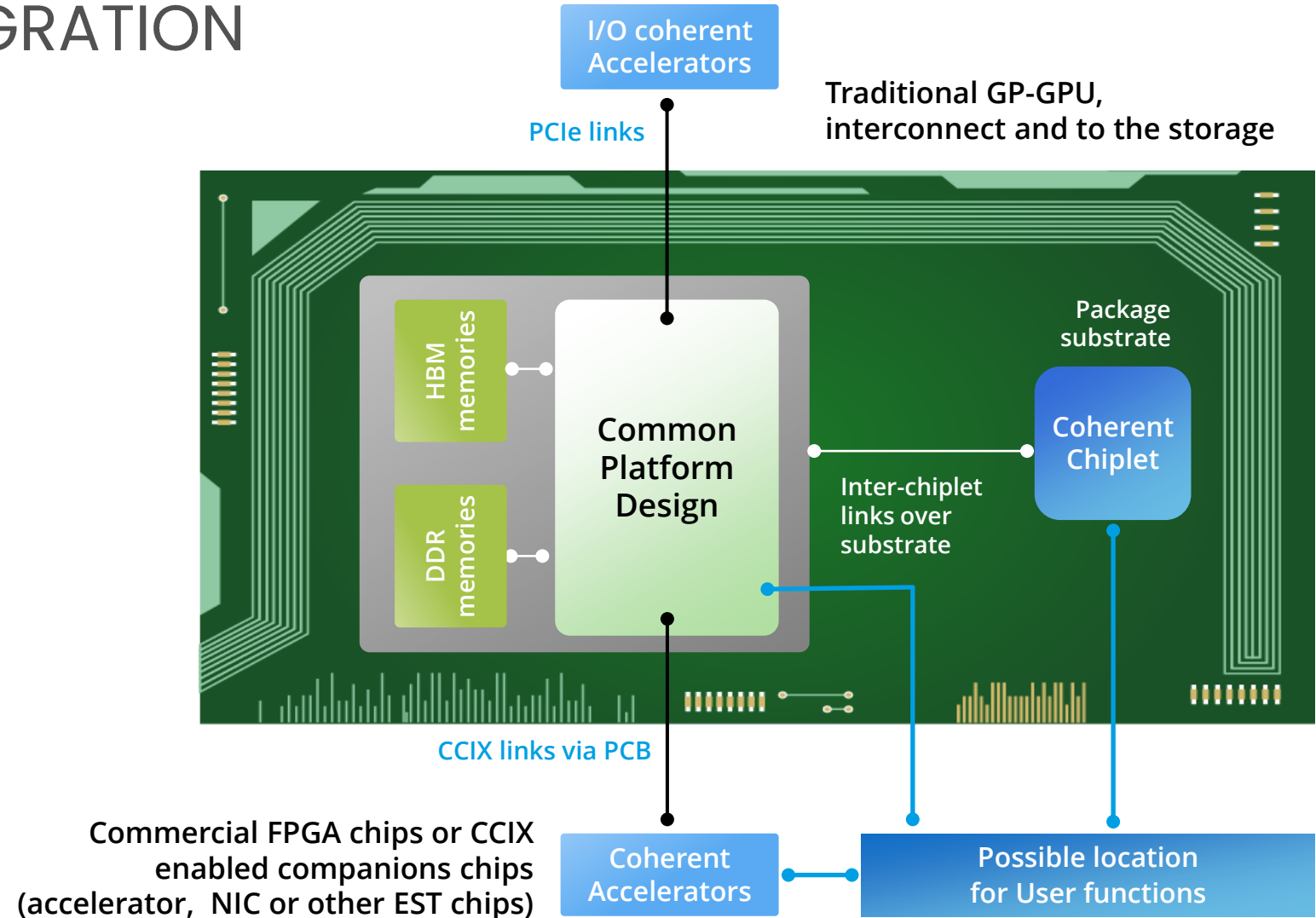


2025  
Moore's law slow-down  
Cost wall

- ## Heterogeneous Many-cores
- General-Purpose Processing
  - Accelerators

# HETEROGENEOUS INTEGRATION

- Allows integration of customized functions in chip, in package, on board, or over PCIe or network link
- EPI Accelerators work in I/O coherent mode and share the same memory viewSingle or dual chiplet package for power efficient sizing
- Designing for high Byte/FLOP ratio
- HBM2e, DDR5 and PCIe gen5
- Coherent NoC with system level cache to keep data local
- D2D interface open to EPI (and beyond)



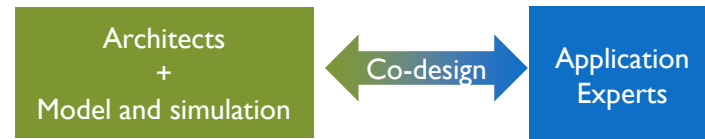


# COMMON PLATFORM TO HARMONIZE THE HETEROGENEOUS COMPUTING ENVIRONMENT

## Computing Units

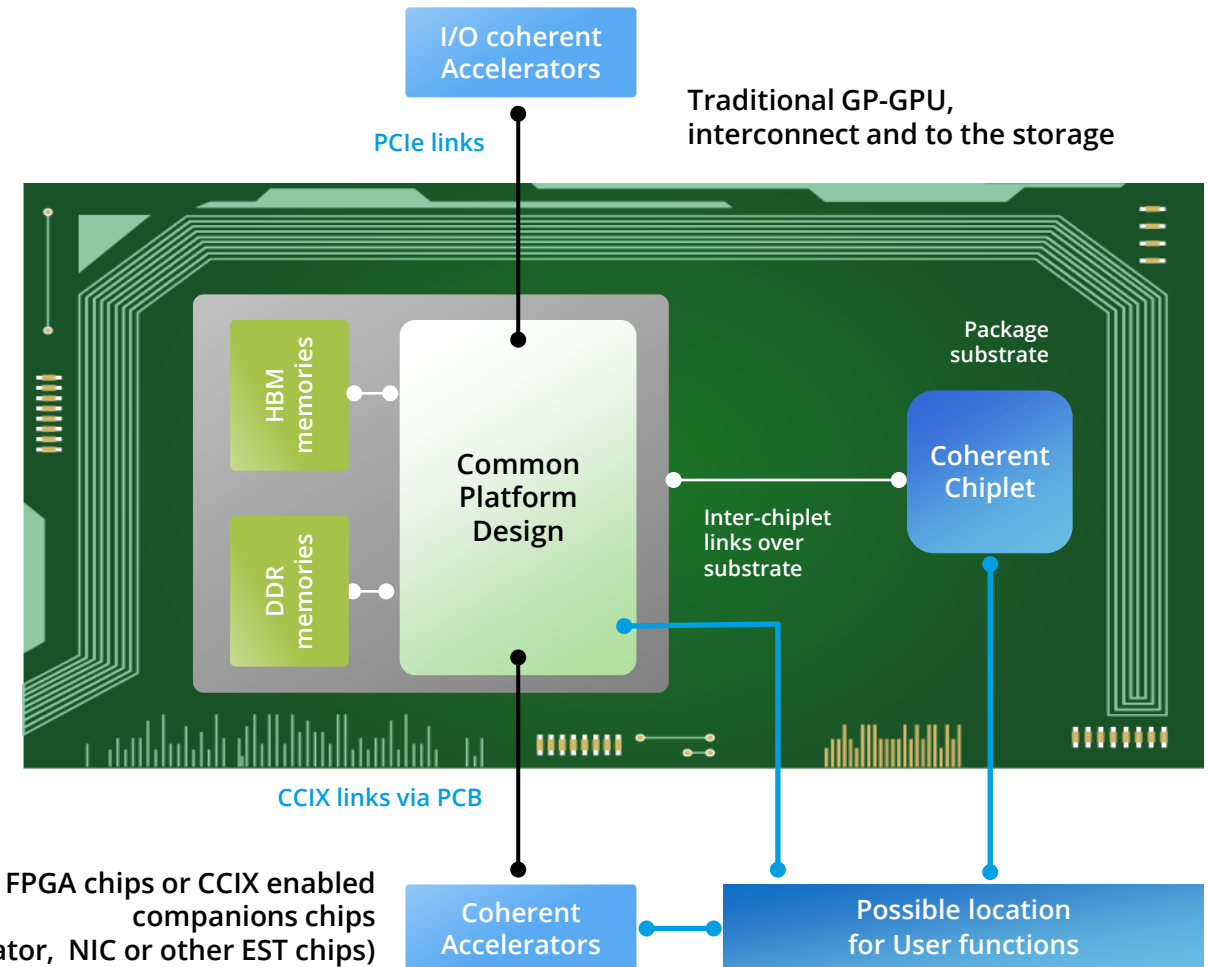
- Arm – Scalable Vector Extension
- MPPA - Multi-Purpose Processing Array
- EPAC – RISC-V based Accelerators
- eFPGA - embedded FPGA

### METHODOLOGY



### SOFTWARE

Automotive eHPC software support	Programming tools & Libraries
Low-level Software, Security, Power Management	
Linux Operating System	
EPI Processor and Reference Hardware	

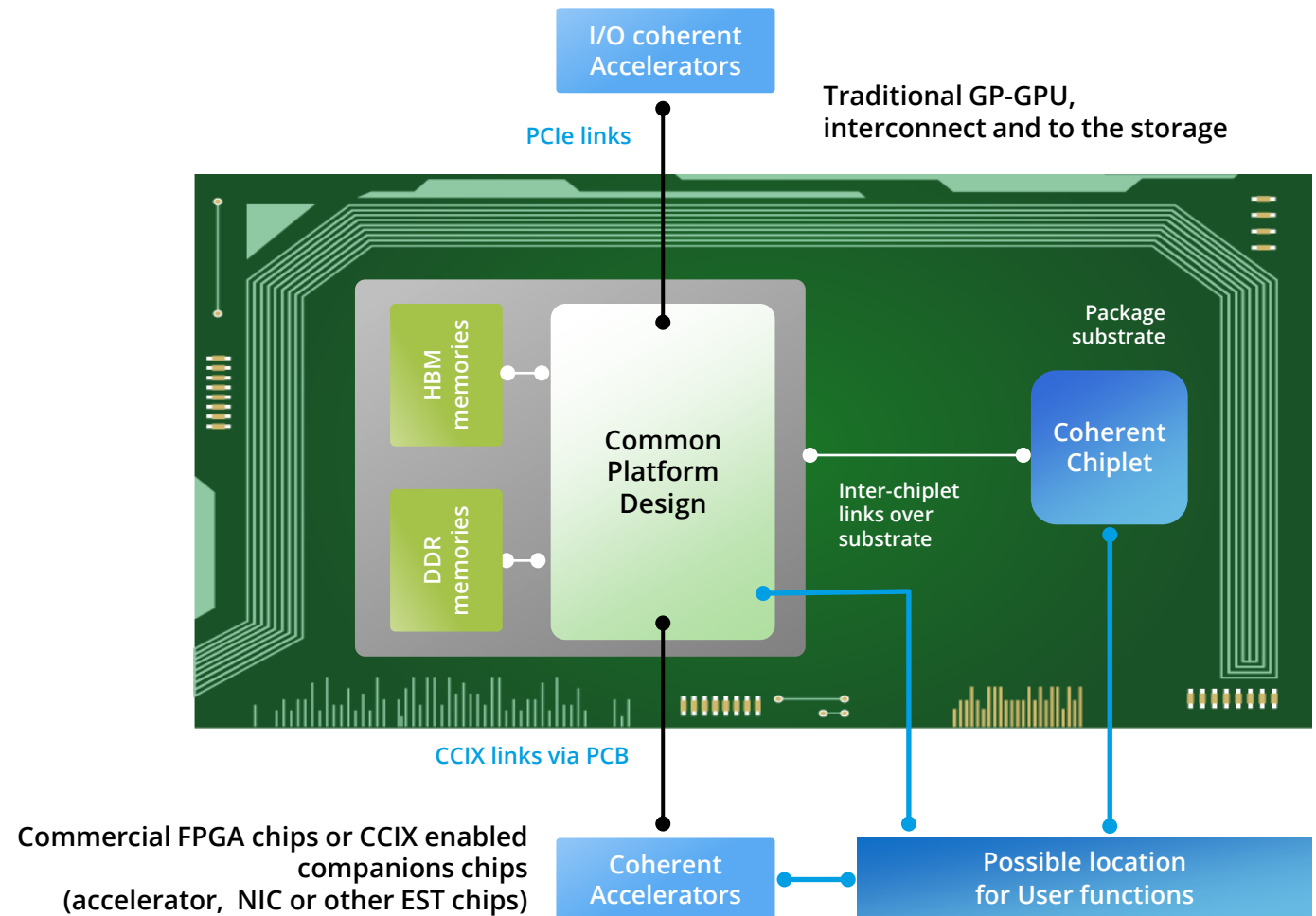


# ON-CHIP HETEROGENEOUS INTEGRATION

- 2D-mesh Network-on-Chip (NoC) to connect computing units: Arm, EPAC, MPPA, eFPGA.
- Common software environment between heterogeneous computing tiles to harmonize their integration with the external environment such as memories (DDR, HBM) and loosely coupled accelerators (through PCIe).

## SOFTWARE

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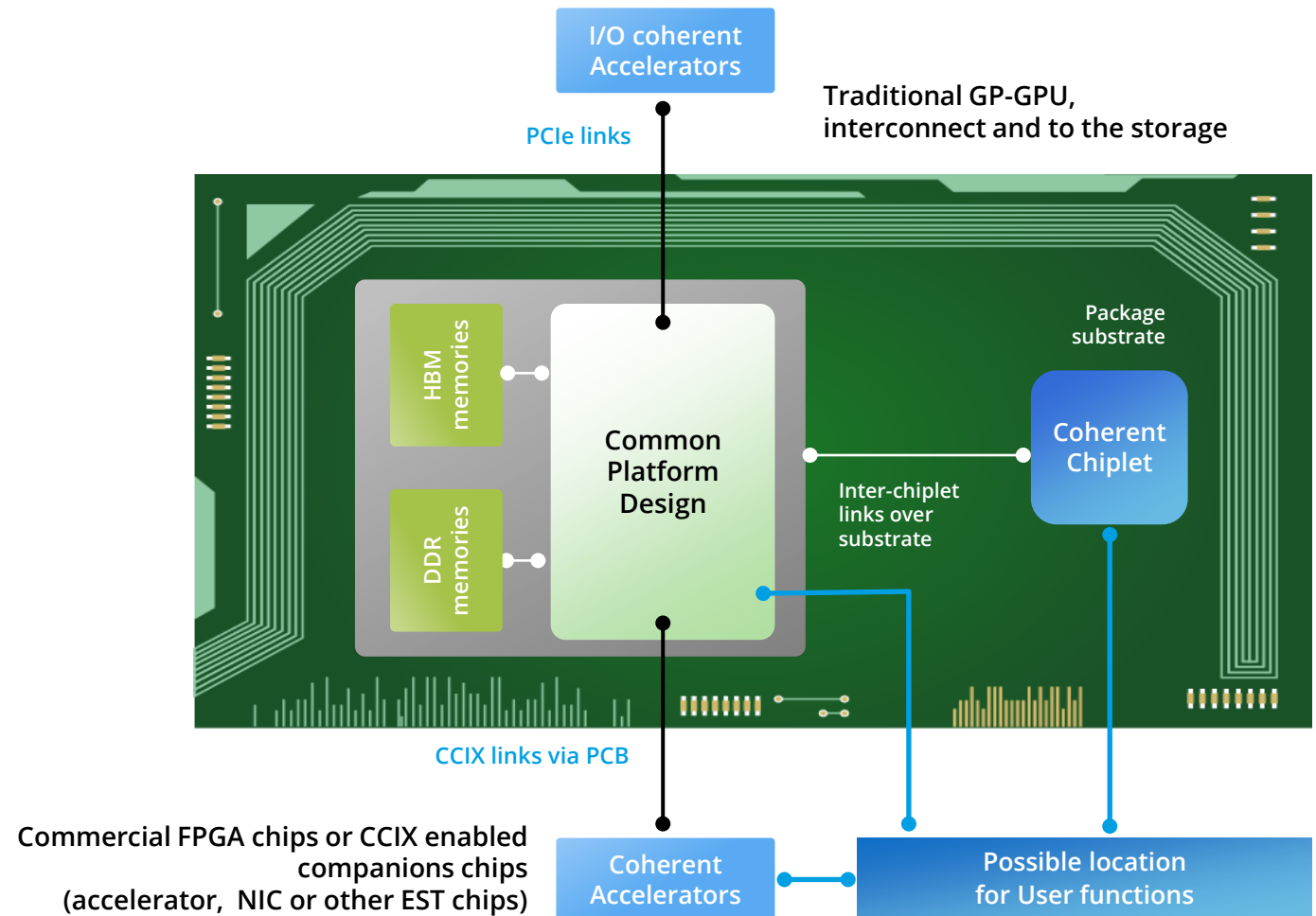
# OFF-CHIP HETEROGENEOUS INTEGRATION

- Chiplet
- Socket
- Network



## SOFTWARE

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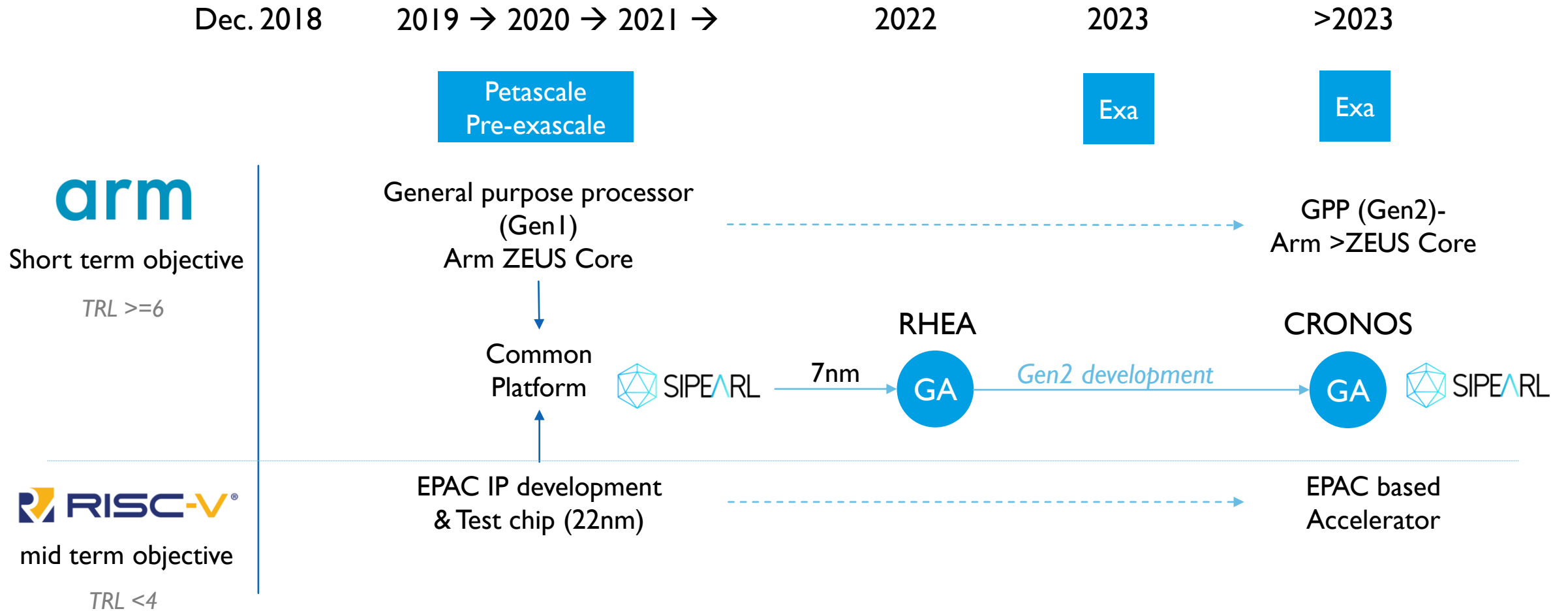




# EPI ROADMAP

SLIDE PREPARED BY SIPEARL, PRESENTED BY DENIS DUTOIT (CEA)

# OVERALL ROADMAP





# CONCLUSION





# INTRODUCTION TO TUTORIAL TOPICS

# AGENDA

FROM	TO	TOPIC
15:00		<b>EPI overview and introduction to tutorial topics</b> <i>Denis Dutoit, CEA</i>
15:30		<b>Hardware Security Module in the EPI General Purpose Processor</b> <i>Sergio Saponara, UNIP</i>
16:00	16:10	<b>Break</b>
16:10		<b>Update of the PCIe boards as development testbed for EPI</b> <i>Fabrizio Magugliani, E4</i>
16:40		<b>SESAM/VPSim: fast and highly-configurable simulation framework for the EPI processor</b> <i>Lilia Zaourar, Tanguy Sassolas CEA</i>
17:20	17:30	<b>Break</b>
17:35		<b>Emulating the power controller of HPC power management systems</b> <i>Andrea Bartolini, Giovanni Bambini, UNIBO</i>
18:10		<b>More Q&amp;A and discussion</b>



# THANK YOU