

EPI, DRIVING THE EUROPEAN HPC ECOSYSTEM TOWARDS THE EXASCALE

HIPEAC 2021

VIRTUAL EVENT

19 JANUARY 2021



European
Processor
Initiative



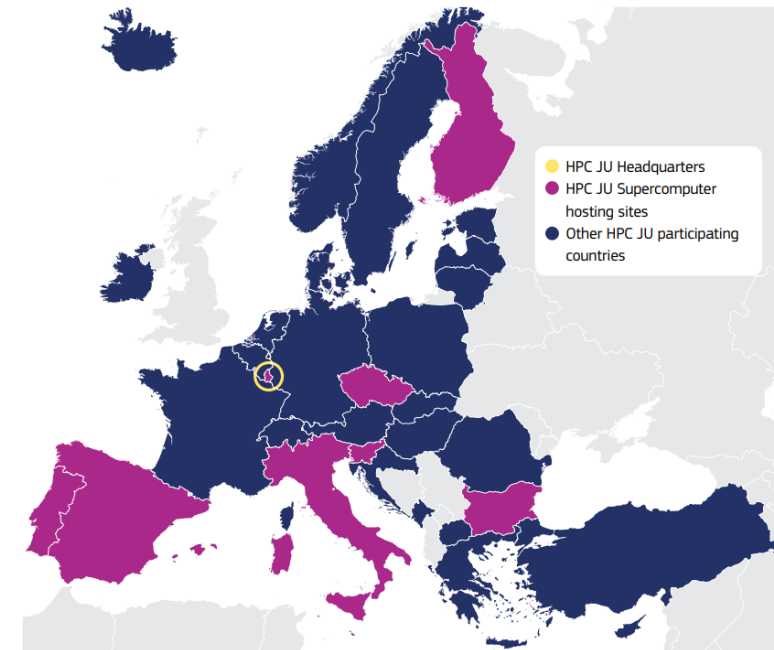
FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES



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EU EXASCALE HPC STRATEGY

- March 2017, Rome: EC launched the *EuroHPC declaration*
- November 2018, EuroHPC Joint Undertaking, a 1 billion Euro joint initiative between the EU and European countries to develop a World Class Supercomputing Ecosystem in Europe
- Oct 2020: 32 participating countries



EUROPE'S AMBITION: EUROHPC

- Developing a new European supercomputing **ecosystem**: HPC systems, network, software, applications, access through the cloud
- Making HPC resources **available to public and private users**, including SMEs.
- Stimulating a **technology supply industry**



EPI OBJECTIVES

- Overall: Develop a complete EU-designed high-end microprocessor, addressing Supercomputing and edge-HPC segments
- Short-term objective
 - Develop and manufacture the EU-designed microprocessor to empower the EU Exascale machines
- Long-term objective
 - Sovereign access to high-performance, low-power microprocessors, from IP to products

27 PARTNERS FROM 10 EU COUNTRIES





EPI COMMON PLATFORM

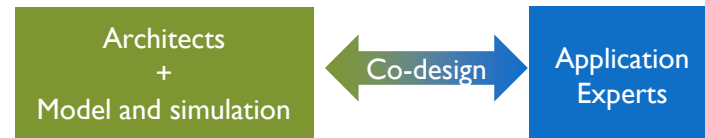
SLIDES PREPARED BY SIPEARL, PRESENTED BY DENIS DUTOIT (CEA)

COMMON PLATFORM TO HARMONIZE THE HETEROGENEOUS COMPUTING ENVIRONMENT

Computing Units

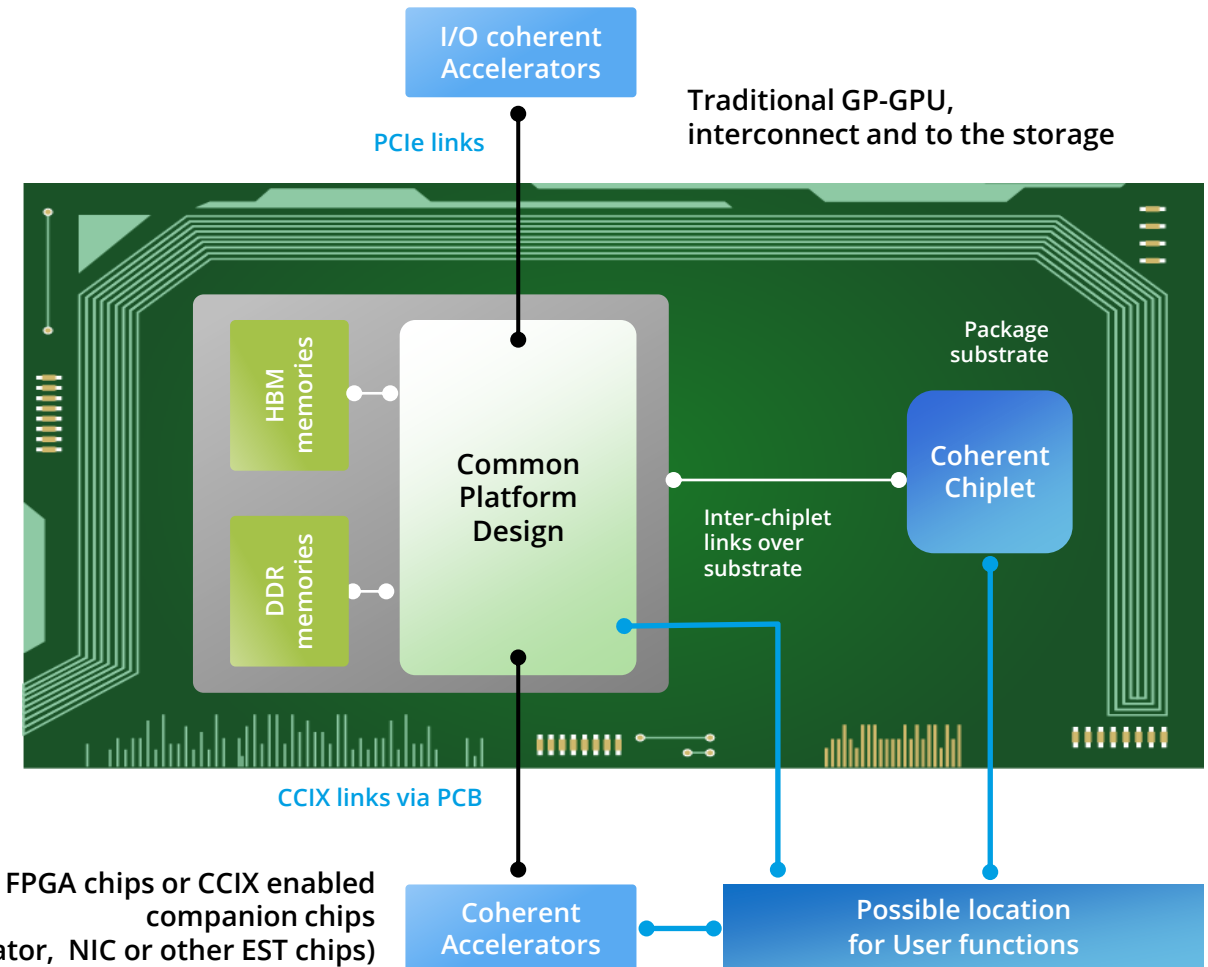
- Arm – Scalable Vector Extension
- MPPA - Multi-Purpose Processing Array
- EPAC – RISC-V based Accelerators
- eFPGA - embedded FPGA

METHODOLOGY



SOFTWARE

Automotive eHPC software support	Programming tools & Libraries
Low-level Software, Security, Power Management	
Linux Operating System	
EPI Processor and Reference Hardware	

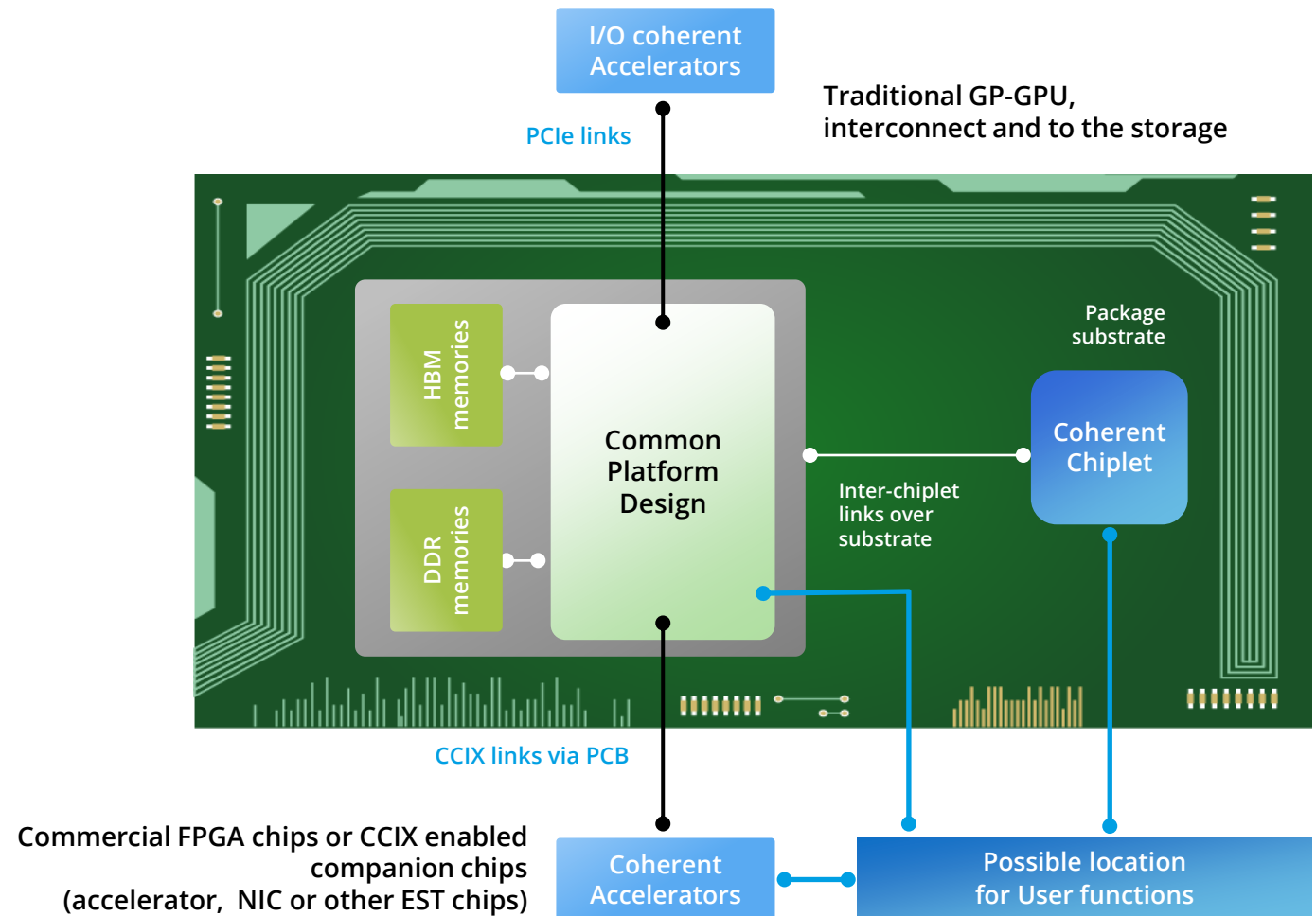


ON-CHIP HETEROGENEOUS INTEGRATION

- 2D-mesh Network-on-Chip (NoC) to connect computing units: Arm, EPAC, MPPA, eFPGA.
- Common software environment between heterogeneous computing tiles to harmonize their integration with the external environment such as memories (DDR, HBM) and loosely coupled accelerators (through PCIe).

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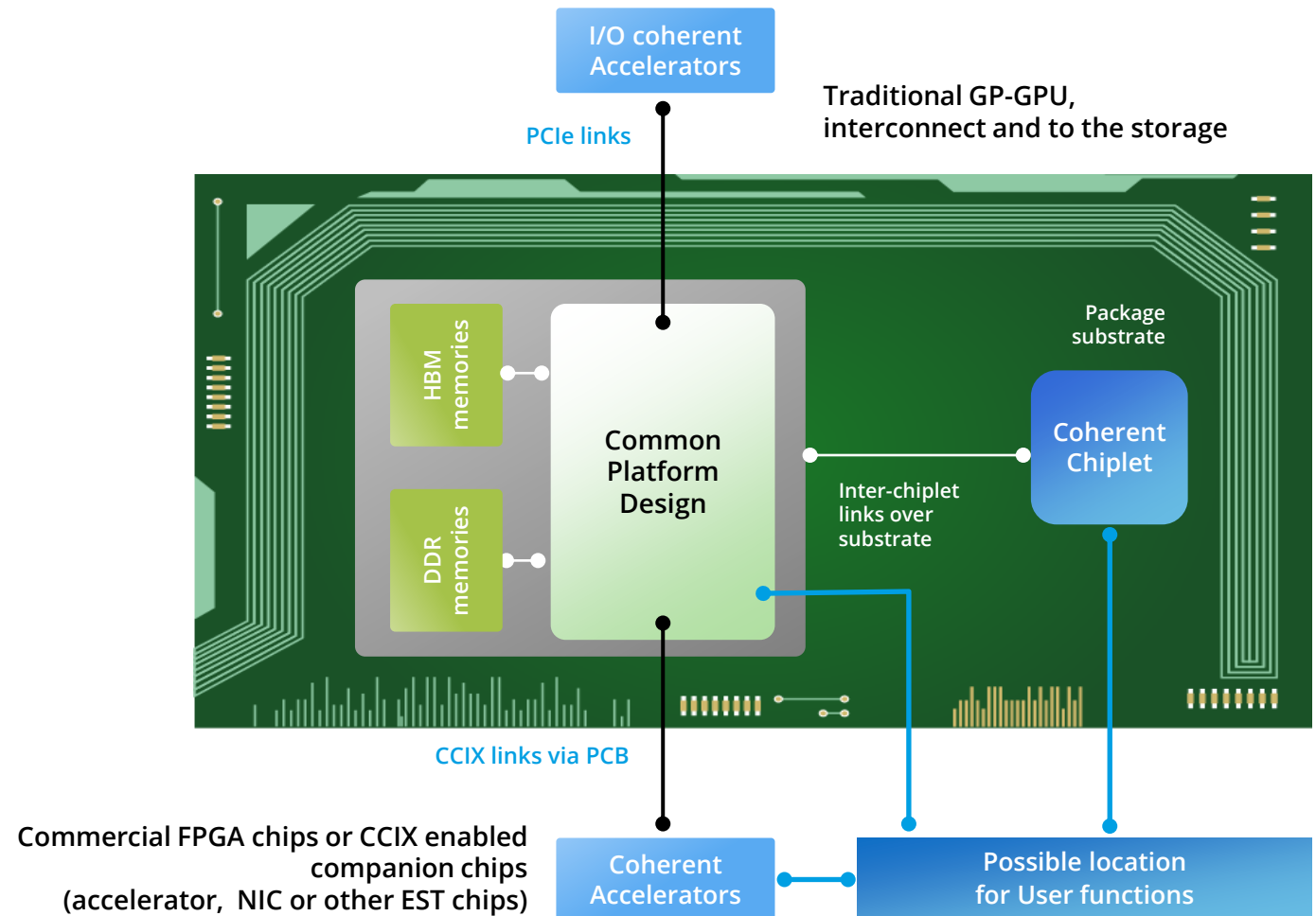
OFF-CHIP HETEROGENEOUS INTEGRATION

- Chiplet
- Socket
- Network



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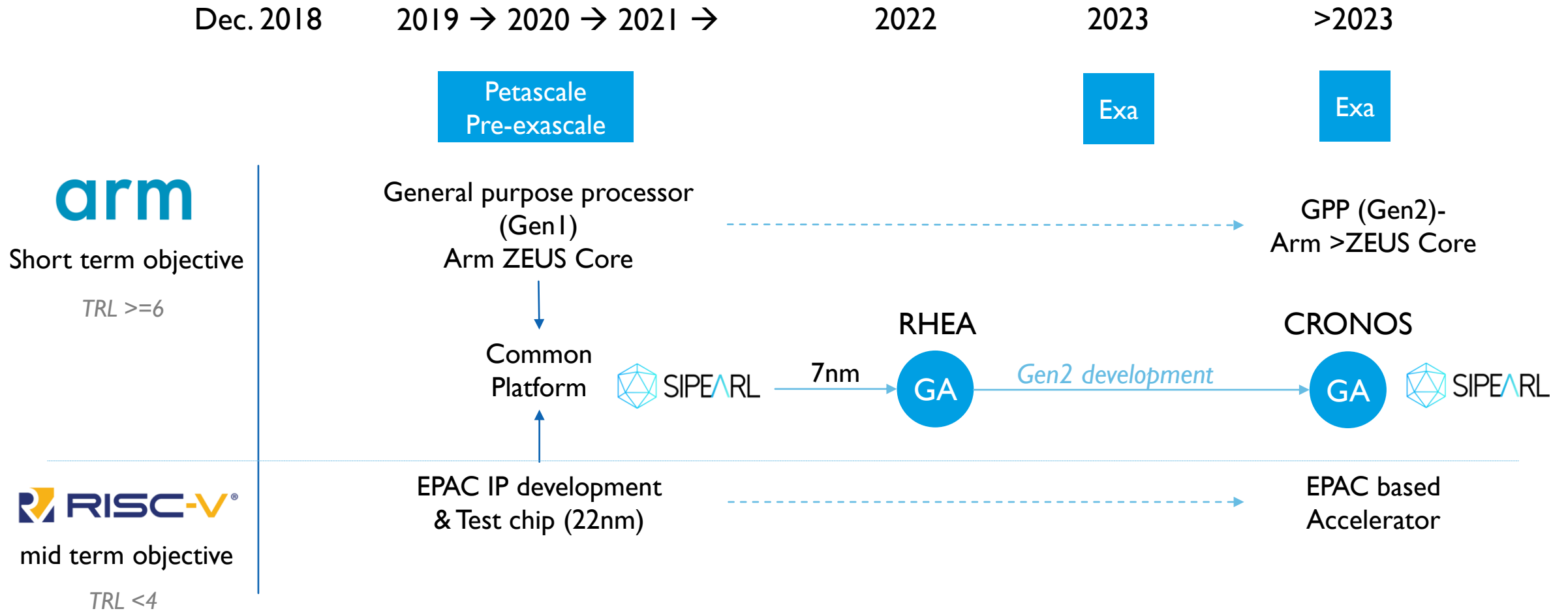




EPI ROADMAP

SLIDE PREPARED BY SIPEARL OF BEHALF OF EPI, PRESENTED BY FABRIZIO MAGUGLIANI (E4 COMPUTER ENGINEERING)

OVERALL ROADMAP





CONCLUSION

FOR FURTHER INFORMATION

<https://www.european-processor-initiative.eu/>



THANK YOU