

THE EPI TECHNOLOGY: EPI PCIE DAUGHTER CARD AS SOFTWARE DEVELOPMENT VEHICLE

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RATIONALE FOR THE PCIe DAUGHTER CARD APPROACH

For the development, testing and ‘stress’ of the design.

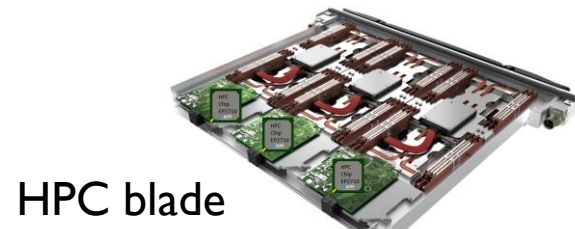
For validating the hardware units, develop the software, and run applications

A PCIe daughter card hosting the EPAC Test Chip and the GPP is

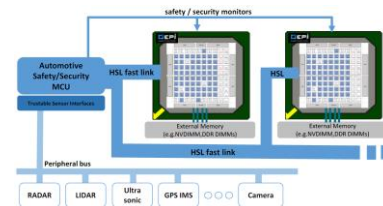
- (relatively...) Easy to design
- Easy to install on any platforms having a PCIe slot (who doesn't???)
- Easy to change configuration/set-up/update system software & drivers
- (relatively...) Affordable (targeting a large potential market)
- Providing key feedback to the design team
- Providing an ideal development platform to developers, ISVs,

WHERE THE PCIE DAUGHTER CARDS FIT IN THE OVERALL EPI PICTURE?

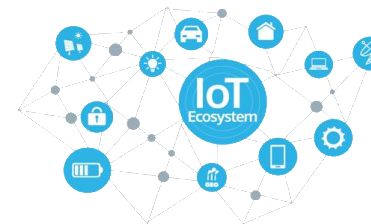
- HPC 'Reference Blade' as the target board for HPC applications
- PCIe daughter card as the development vehicle, available earlier than the Reference Blade and providing input for the design of the Reference Blade
- Enabler for early-access PoC in target markets



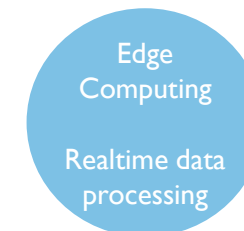
- PCIe daughter card
- GPP
 - EPAC Test Chip



Automotive PoC

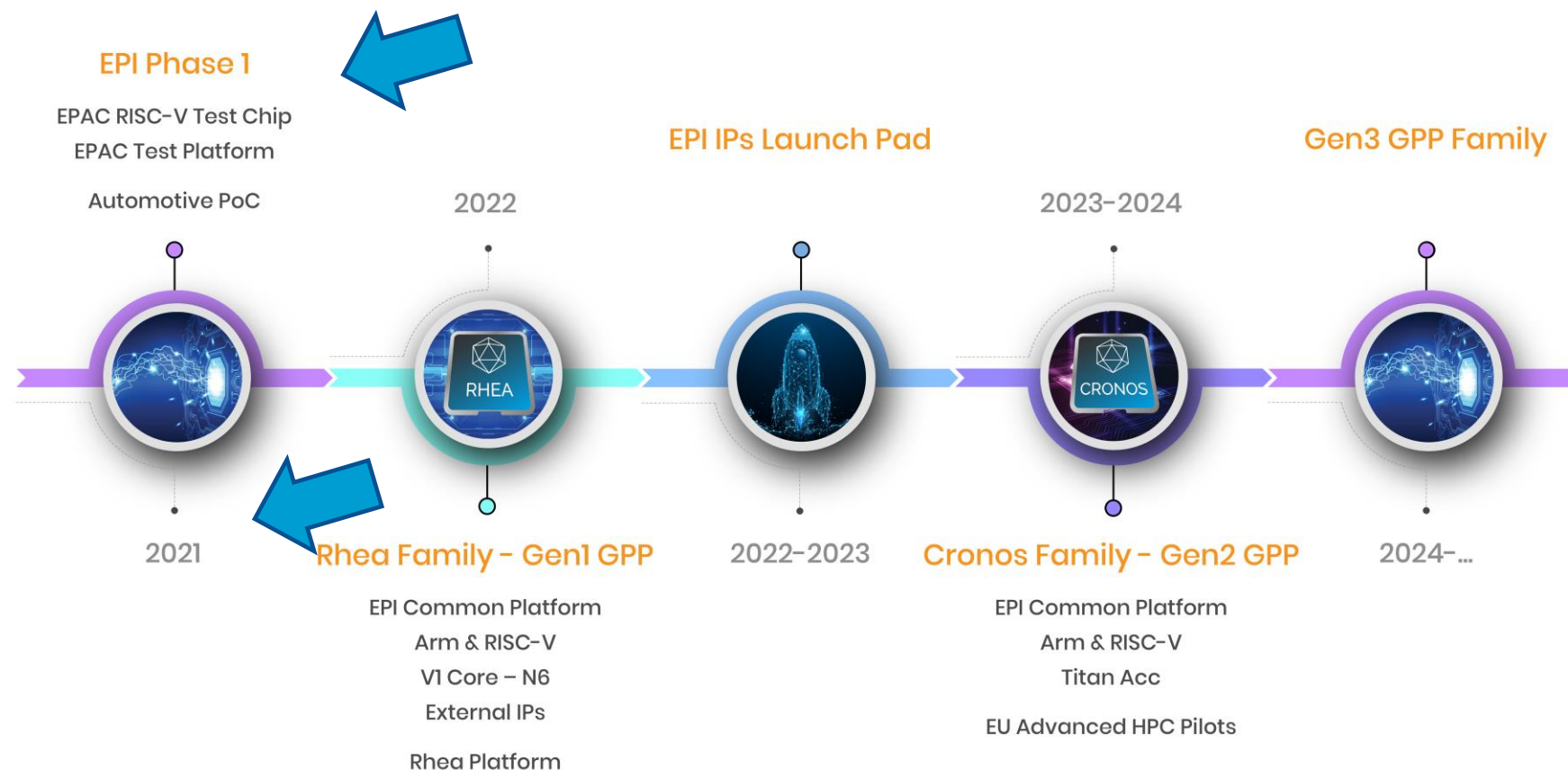


IoT PoC



Edge Computing PoC

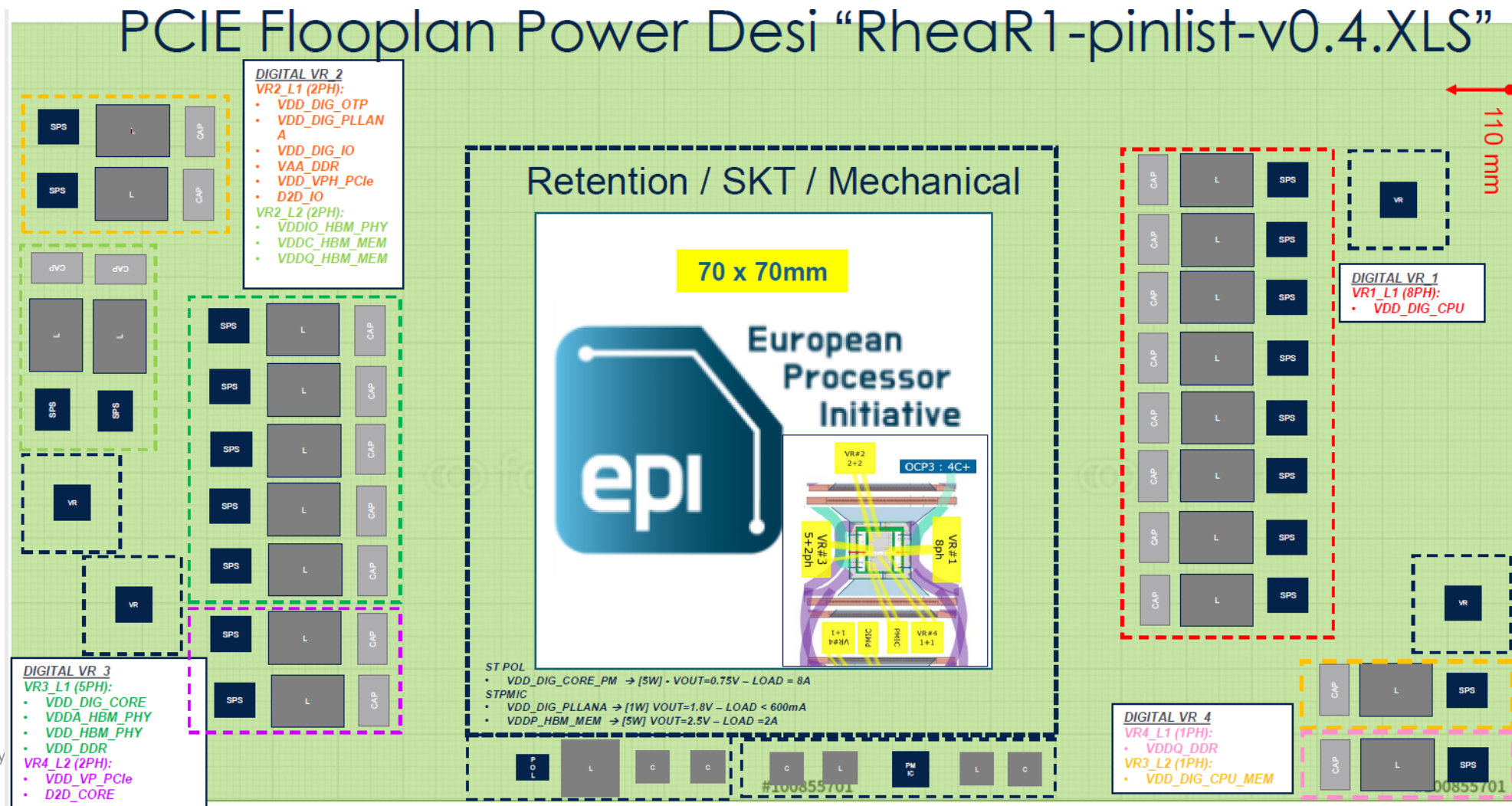
WHEN WILL THE PCIE DAUGHTER CARDS BE AVAILABLE?



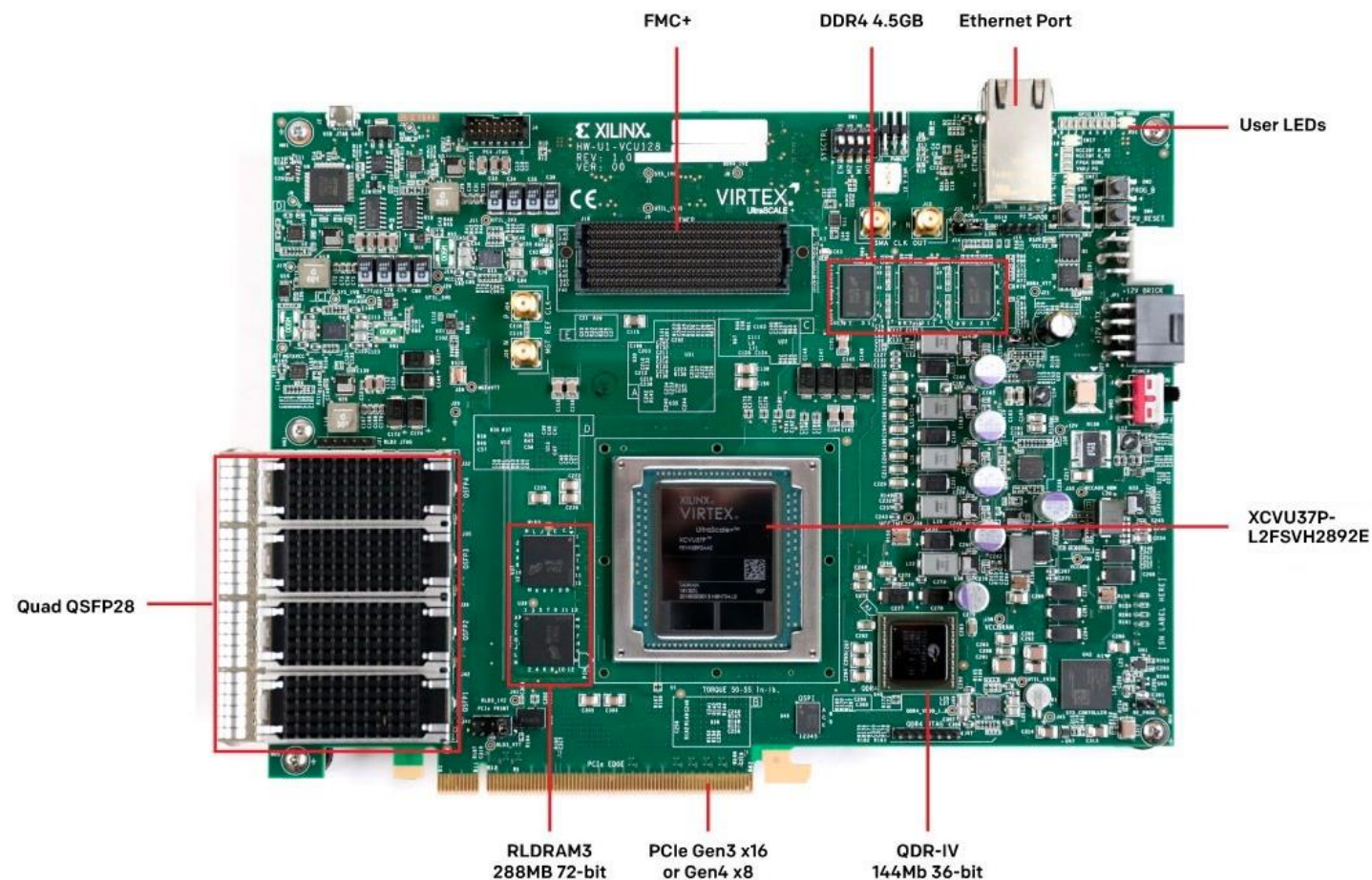
EPI ROADMAP

CURRENT STATUS OF THE PCIE/GPP DAUGHTER CARD

PCIE Flooplan Power Desi "RheaR1-pinlist-v0.4.XLS"



CURRENT STATUS OF THE PCIE/TEST CHIP DAUGHTER CARD



CONCLUSION

- The PCIe daughter board is instrumental for the development, testing and ‘stress testing’ the design of the EPI
- When the board has reached a production quality, it will represent the ideal hardware and software development platform
- Stay tuned....

 www.european-processor-initiative.eu

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