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EXCELENCIA SEVERO OCHOA

LOCA:
Embracing Open Source Hardware to create an Open Source Ecosystem

John D. Davis, Ph.D.

October 22, 2020

An Open HPC Ecosystem?

- Technology Landscape
- HPC History
- LOCA
- Open Source Hardware Projects

Today´s technology trends

Massive penetration of Open Source Software

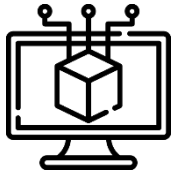
- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)

Moore´s Law + Power = **Specialization**

- More cost effective
- More performant
- Less Power

SOFTWARE/
HARDWARE
CO-DESIGN

Today´s technology trends



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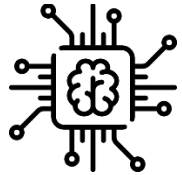


New Open Source Hardware Momentum from IoT and the Edge to HPC

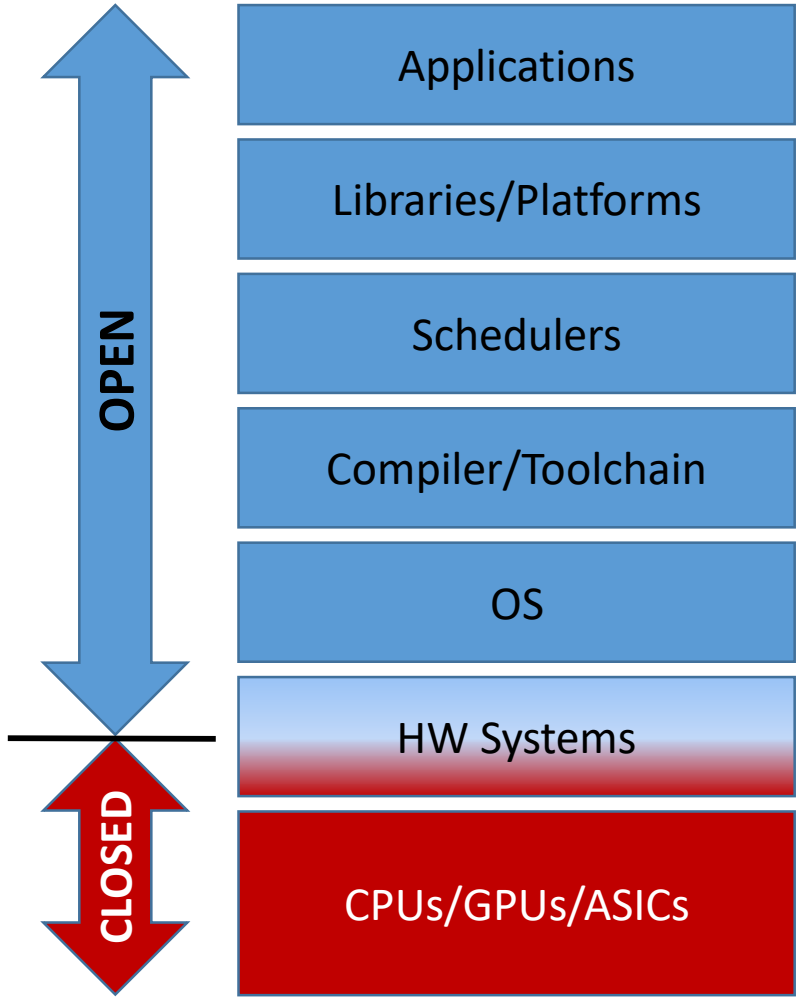
- RISC-V
- OpenPOWER

Linux History

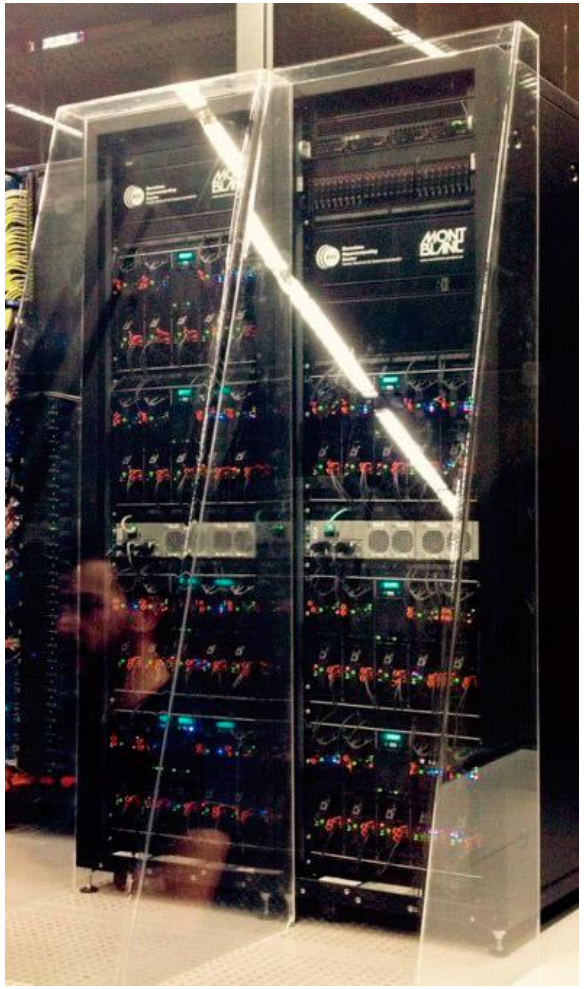
- 1991: Started development, release
- 1992: X Windows released
- 1998: Adopted by many major companies
- 2004: BSC Supercomputer OS
- 2009: Basis for many new business systems and the cloud
- 2013: Android in 75% of the world smart phones
- 2015: De facto OS for IoT, mobile, cloud, and supercomputers

HPC Today

- **Europe has led the way in defining a common open HPC software ecosystem**
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU?**
- Inhibits opportunities in holistic co-design
  - Facing barrier to innovation
  - Being able to have a conversation or not



Mont-Blanc HPC Stack for ARM



Industrial applications

Pharmacelera, MUREX, DASSAULT AVIATION, AVL, Termo Fluids, Cenaero, ROLLS ROYCE

Applications

GENCI, CINECA, UNI GRAZ, HLRS, University of BRISTOL

System software

ARM, ETH zürich, Inria, Barcelona Supercomputing Center, JÜLICH FORSCHUNGSZENTRUM, Bull atos technologies

Hardware

ARM, Barcelona Supercomputing Center, Bull atos technologies, cea, UC UNIVERSIDAD DE CANTABRIA

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The Exascale Race – The Japanese example

Co-design from Apps to Architecture

R-CCS

- **Architectural Parameters to be determined**
  - #SIMD, SIMD length, #core, #NUMA node, O3 resources, specialized hardware
  - cache (size and bandwidth), memory technologies
  - Chip die-size, power consumption
  - Interconnect
- **We have selected a set of target applications**
- **Performance estimation tool**
  - Performance projection using Fujitsu FX100 execution profile to a set of arch. parameters.
- **Co-design Methodology (at early design phase)**
  1. Setting set of system parameters
  2. Tuning target applications under the system parameters
  3. Evaluating execution time using prediction tools
  4. Identifying hardware bottlenecks and changing the set of system parameters

Target applications representatives of almost all our applications in terms of computational methods and communication patterns in order to design architectural features.

Target Application	
Program	**Brief description**
① GENESIS	MD for proteins
② Genomon	Genome processing (Genome alignment)
③ GAMERA	Earthquake simulator (FEM in unstructured & structured grid)
④ NICAM+LETK	Weather prediction system using Big data (structured grid stencil & ensemble Kalman filter)
⑤ NTChem	molecular electronic (structure calculation)
⑥ FFB	Large Eddy Simulation (unstructured grid)
⑦ RSDFT	an ab-initio program (density functional theory)
⑧ Adventure	Computational Mechanics System for Large Scale Analysis and Design (unstructured grid)
⑨ CCS-QCD	Lattice QCD simulation (structured grid Monte Carlo)

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RIKEN

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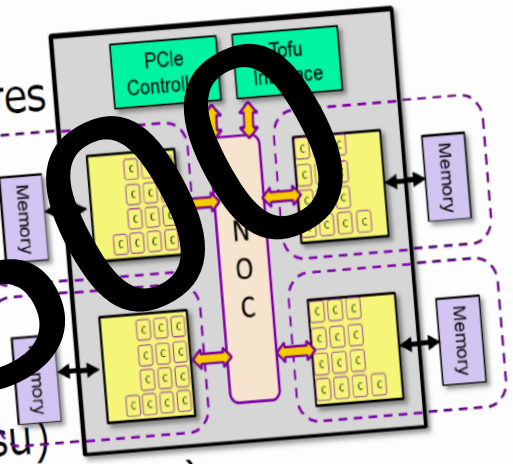
The Exascale Race – The Japanese example

"Post-K" Arm64fx Processor is…

- an Many-Core ARM CPU…
  - 48 compute cores + 2 or 4 assistant (OS) cores
  - Brand new core design by Fujitsu
  - Near Xeon-Class Integer performance co
  - ARM V8.2 --- 64bit ARM ecosyste
- …but also a GPU-like processor
  - SVE 512 bit vector extensions (ARM & Fujitsu)
    - Inte (1, 2, 4, 8 bytes) + float (16, 32, 64 bytes)
  - Cache + ccess localization (sector cache) – similar to scratchpad
  - HBM2 OPL – Massive Mem BW (1TByte/s, Bytes/DPF ~0.4 same as K)
  - Streaming memory access, strided access, scatter/gather etc.
  - Intra-chip barrier synch. and other memory enhancing features
  - 40GByte/s Tofu-.D interconnect + PCIe 3
- GPU-like High performance in HPC, AI/Big Data, Auto Driving…



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#1 TOP500

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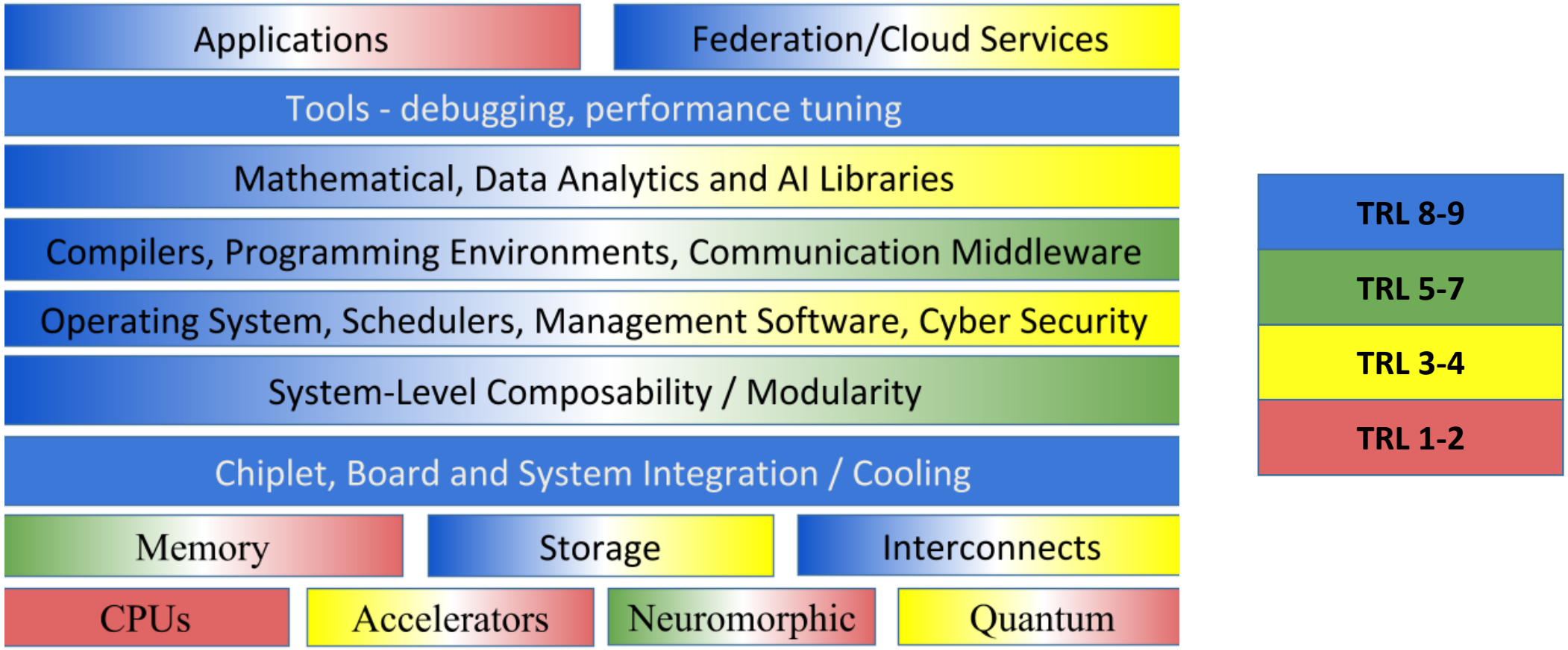
The European Open System Stack



Why Europe needs its own processor

- Processors now control almost every aspect of our lives
- **Security** (back doors, etc.)
- Possible **future restrictions on exports to EU** due to increasing protectionism
- **A competitive EU supply chain** for HPC technologies will create jobs and growth in Europe

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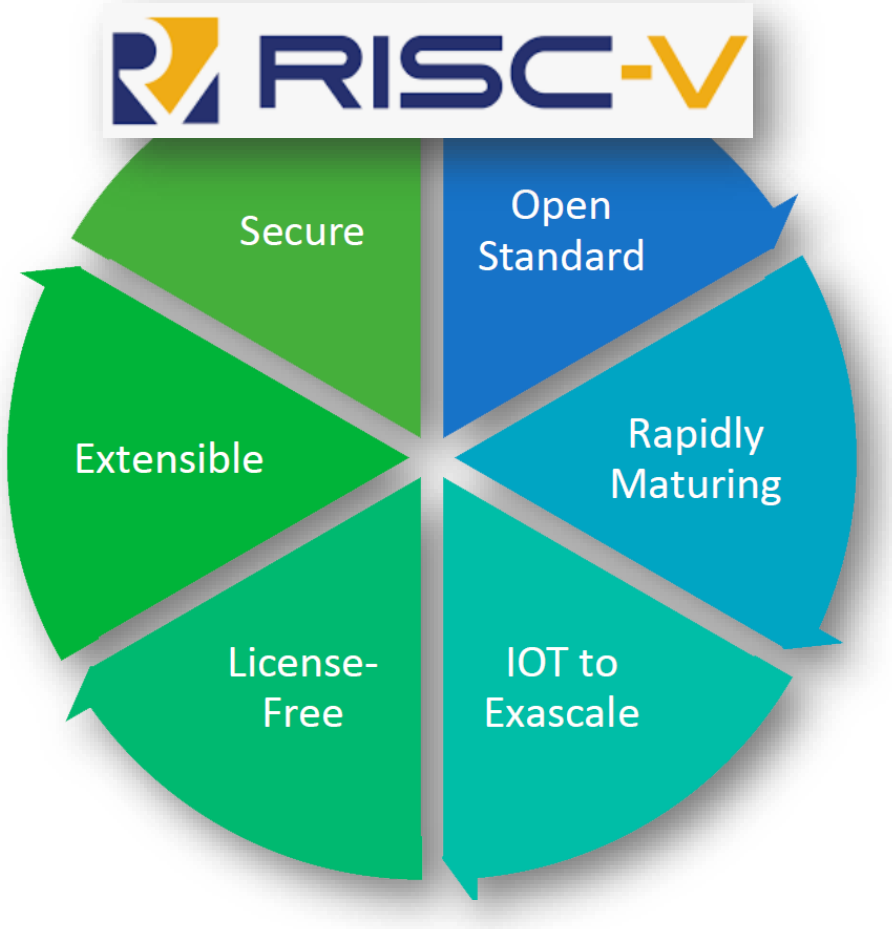
RISC-V is democratizing chip-design

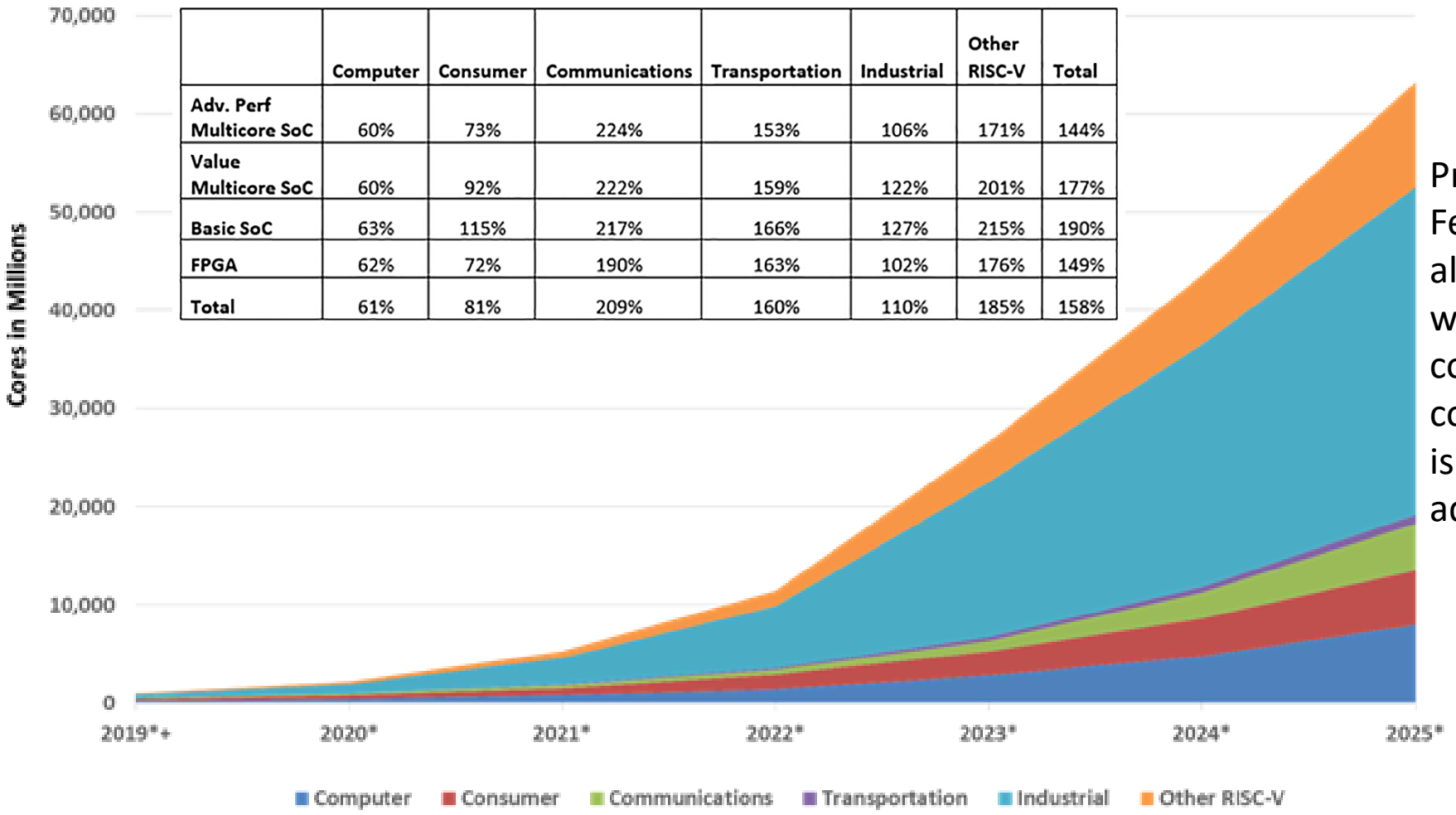


- More and more global IT actors are adopting RISC-V architectures to be vendor independent
  - Google
  - Amazon
  - Western Digital
  - Alibaba
- And of course the entire IoT ecosystem for lower performance, lower energy applications.
- Major opportunity for ICT industry also in Spain

RISC-V Worldwide Growth Projection

CAGR for RISC-V CPU cores between 2018 and 2025

	Computer	Consumer	Communications	Transportation	Industrial	Other RISC-V	Total
Adv. Perf Multicore SoC	60%	73%	224%	153%	106%	171%	144%
Value Multicore SoC	60%	92%	222%	159%	122%	201%	177%
Basic SoC	63%	115%	217%	166%	127%	215%	190%
FPGA	62%	72%	190%	163%	102%	176%	149%
Total	61%	81%	209%	160%	110%	185%	158%



President of Semico Research, Jim Feldhan, commented: “Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of 62.4 billion RISC-V cores by 2025, signaling that RISC-V is on the fast track to mainstream adoption.”

Source: Semico Research Corp.

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RISC-V History

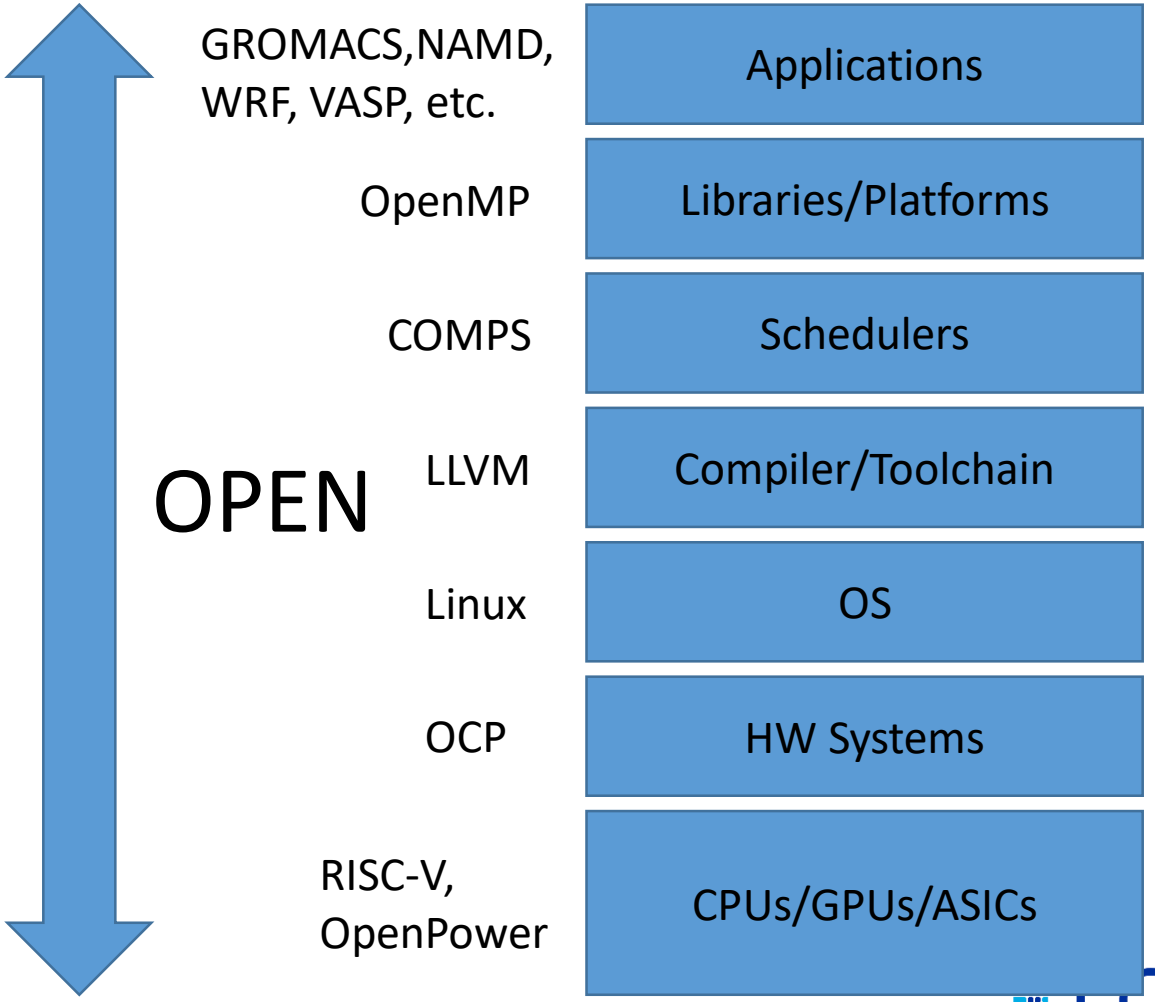
- 2010: Started development and initial proposal
- 2015: RISC-V Foundation formed
- 2019: Adopted by many major companies
  - Starting in the embedded market with already over 1 Billion CPUs

- 2020
  - RISC-V Foundation moves to Switzerland

The time is now to embrace and support RISC-V from IoT to HPC

HPC Tomorrow

- Europe can lead the way to a completely **open SW/HW stack for the world**
- RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
- Europe can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- **RISC-V can unify, focus, and build a new microelectronics industry in Europe.**



Open Source Beyond 2020

"**Open Source has become mainstream across all software industry** during the past 10 years. To a large extent, **open software re-use has proven economically efficient**. The level of maturity of Open Source Hardware (OSH) remains far lower than that of Open Source Software (OSS). However, **business ecosystems for OSH are developing fast so that OSH could constitute a cornerstone of the future Internet of Things (IoT) and the future of computing**."

- DG Connect & DG IT Workshop, Brussels, Nov. 14-15, 2019

Source: https://ec.europa.eu/digital-single-market/en/news/workshop-about-future-open-source-software-and-open-source-hardware

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European Laboratory for Open
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BSC full stack

SW

HW

Software/Hardware Co-Design

HPC Applications

Specialization using HW/SW Co-Design

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HPC Hardware

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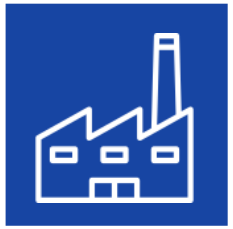
LOCA Goals

- Mechanism to extend open source ecosystem to include H/W
  - Add H/W expertise to BSC and European partners, leveraging S/W expertise
  - Provide proven/usable Open Source H/W
  - Intersection of academia and industry
  - Open European IP repository → rapid implementation
  - Catalyst to reinvigorate European ICT industry
  - **Global** collaboration and training center
  - Incubator for European IP

Open

- Participation from Academia across Europe
  - Student training
  - Affiliate Labs at other institutions
  - Research collaboration
  - Repository for research work



- Participation from European and global industry
  - Engagement with European Research and Development
  - Access to European talent
  - European visibility and branding
  - Innovation incubator

European Collaboration & Education

Casteller
(human tower)

- Traditional chip design is done in a Master/Apprentice environment
- LOCA recreates this environment by bringing in Masters from industry to collaborate with a variety of people, pushing beyond RTL
- Professors, students, and industry veterans all together
- Ideal sandbox for creative and innovative work
- Research and Design to chip fabrication

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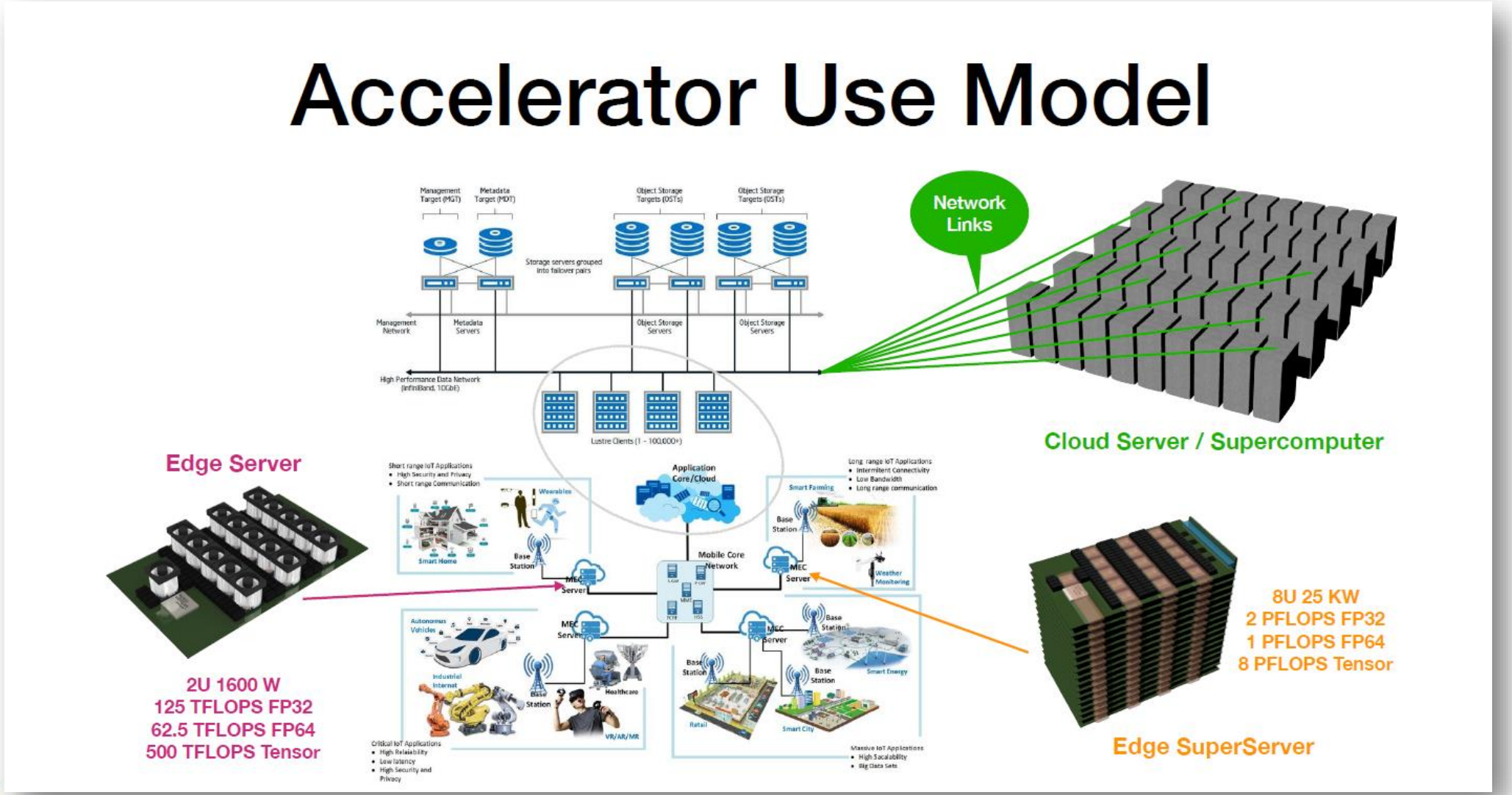
From IoT, Edge Computing, Clouds to Supercomputers



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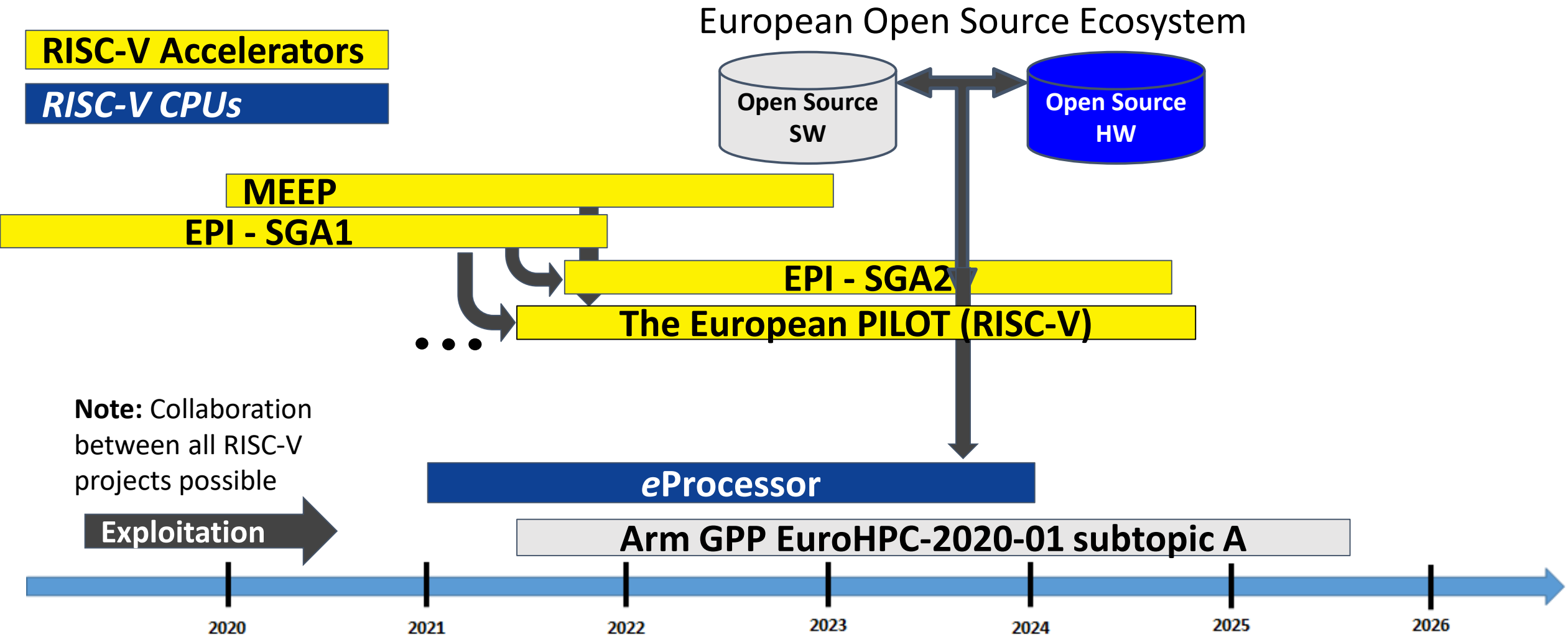
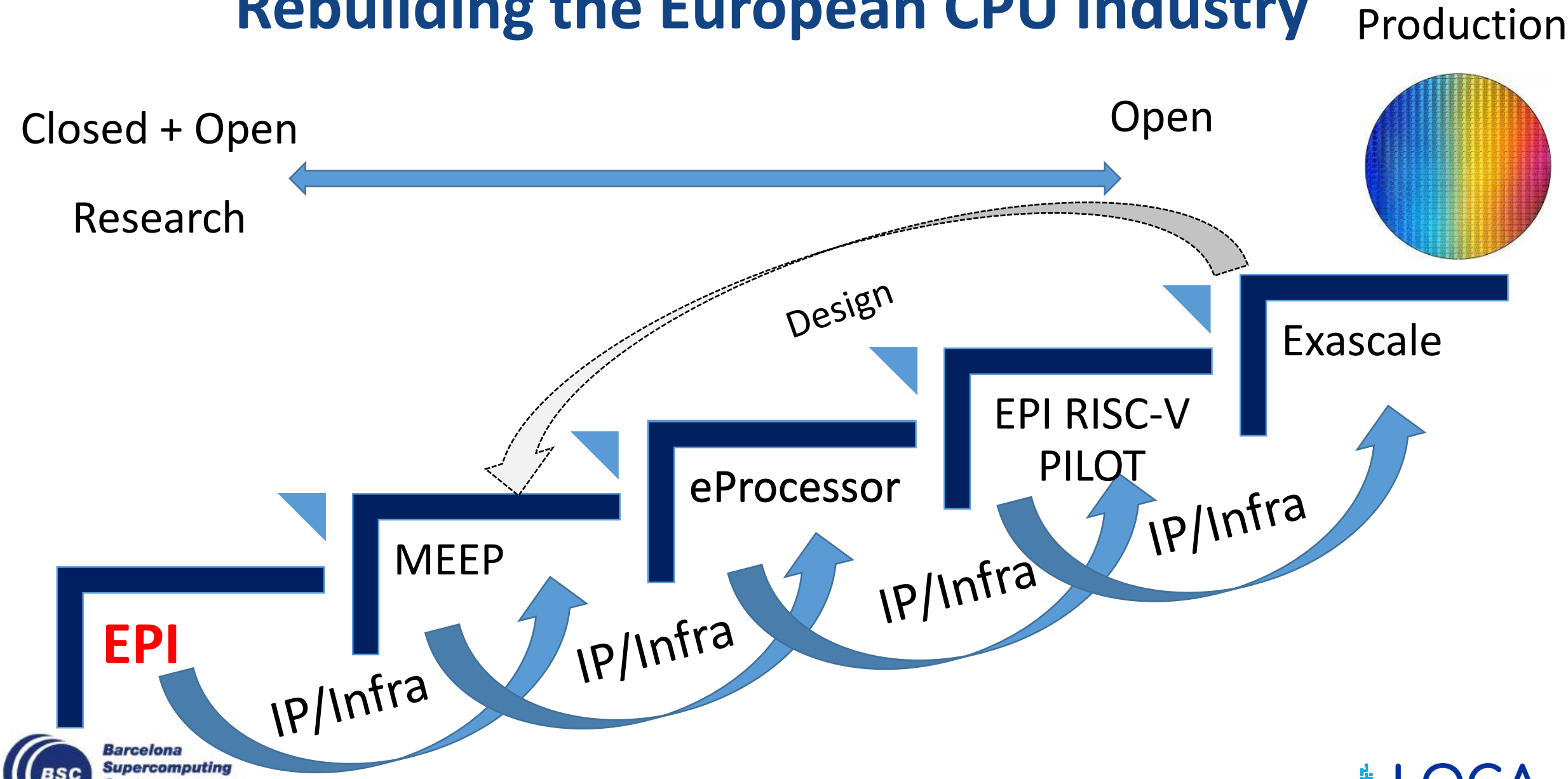
Current BSC RISC-V European Accelerator & CPU Landscape



Rebuilding the European CPU Industry



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The European Processor Initiative

- In the same way BSC led the development of ARM processors for HPC in the various MontBlanc projects, now it leads the RISC-V HPC accelerator development in EPI
- EPI is a 100% funded EuroHPC project (120 M€) to develop European processor technology by 2022
- BSC was the original initiator of EPI and most active proponent in the scientific and technical community
- EPI is led by Atos/Bull with 28 partners from leading HPC industrial and academic centers

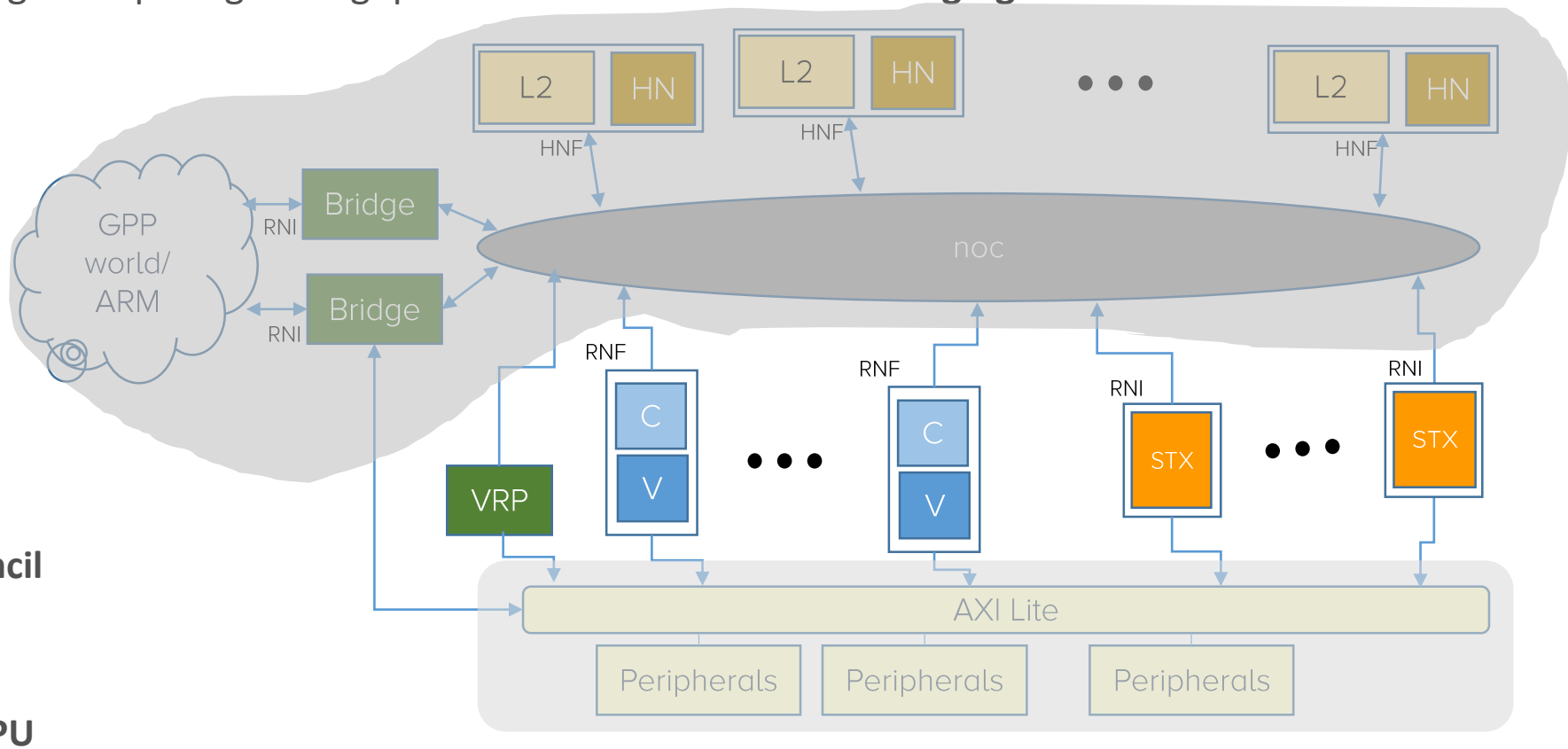
EPI Partners

EPAC architecture

- **Objective: Develop** & demonstrate **fully European** processor IPs based on the **RISC-V ISA.** Build on existing EU IP, leverage EU background and vision
- Provide a very **low power** and high computing throughput **accelerator for HPC & Emerging -> Automotive**

Main Contributors:

- **RISC-V in the Tile:**
  - **8 Vector cores, 8 STX, 1 VRP**
- **Vector Core :**
  - **Spain + Italy + Croatia**
  - **C: RISC-V Scalar core**
  - **V: RISC-V Vector core: 8 lanes**
- **STX**
  - **Switzerland + Germany**
  - **RISC-V NTX (AI/ML/DL) + Stencil**
- **VRP**
  - **France**
  - **RISCV + Extended precision FPU**



UNIBO | IST | CEA | Chalmers | FORTH | Semidynamics | BSC | ETH + FhG | EXTOLL | ETH

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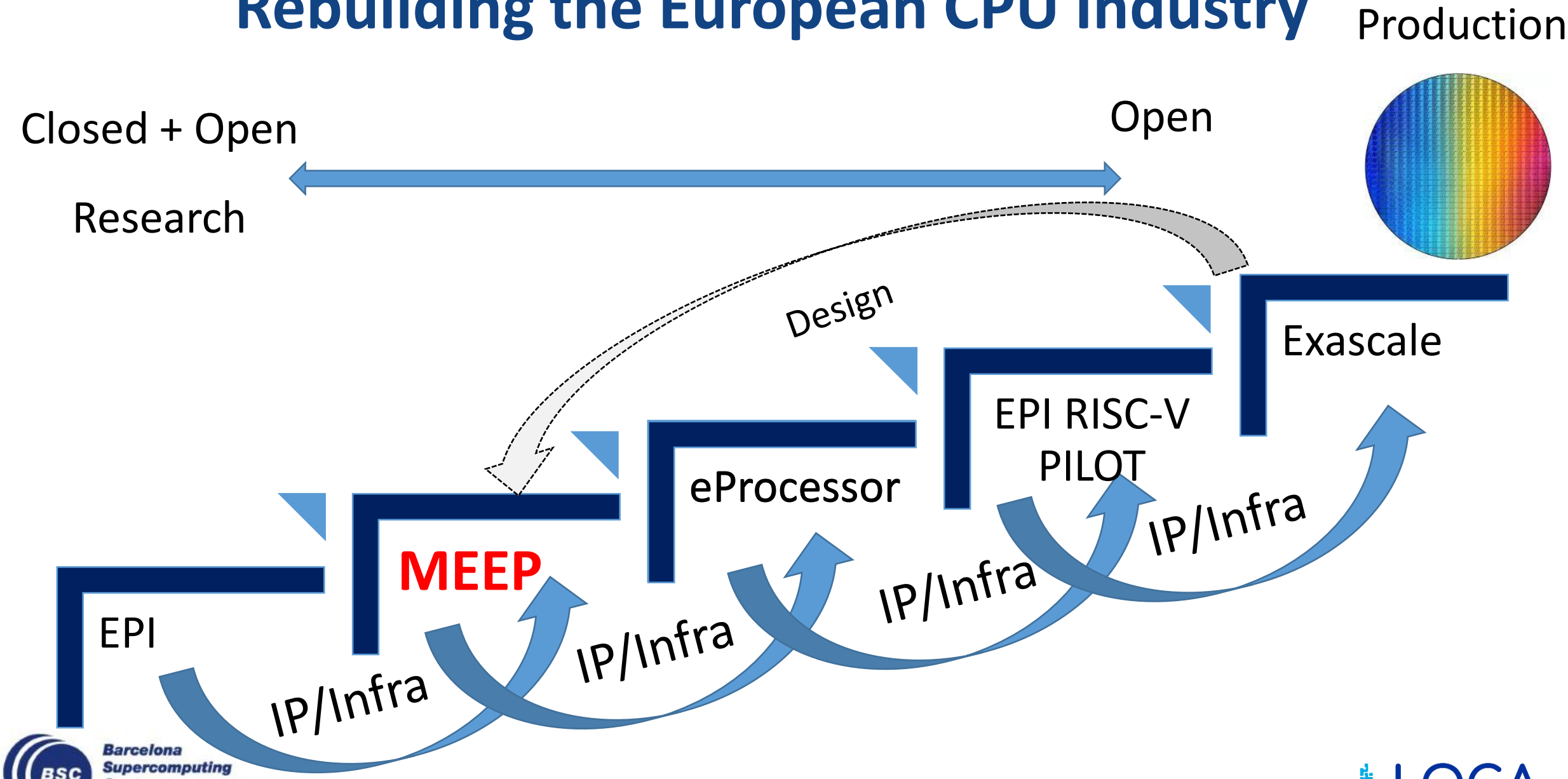

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MareNostrum 5
A European pre-exascale supercomputer

- **200 Petaflops** peak performance (200 x 10^{15})
- **Experimental platform (MEEP)** to create supercomputing technologies “made in Europe”

Hosting Consortium:

Spain **Portugal** **Turkey** **Croatia** **Ireland**

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The MEEP project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and Spain, Croatia, Turkey.

EuroHPC Joint Undertaking

MEEP: MareNostrum Experiment Exascale Platform

MEEP is a flexible FPGA-based emulation platform that will explore hardware/software co-designs for Exascale Supercomputers and other hardware targets, based on European-developed IP. The project provides two functions:

An evaluation platform of pre-silicon IP and ideas, at speed and scale.

A software development and experimentation platform to enable software readiness for new hardware.

MEEP

MareNostrum Experimental Exascale Platform

The MEEP project has received funding from the European High-Performance Computing Joint Undertaking Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Croatia, Turkey.

MEEP will enable software development, accelerating software maturity, compared to the limitations of software simulation. IP can be tested and validated before moving to silicon, saving time and money.

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Faculty of Electrical Engineering and Computing

TÜBİTAK BİLGEM

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Accelerated Compute and Memory Engine (ACME) Architecture

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Mapping ACME Architecture to an FPGA

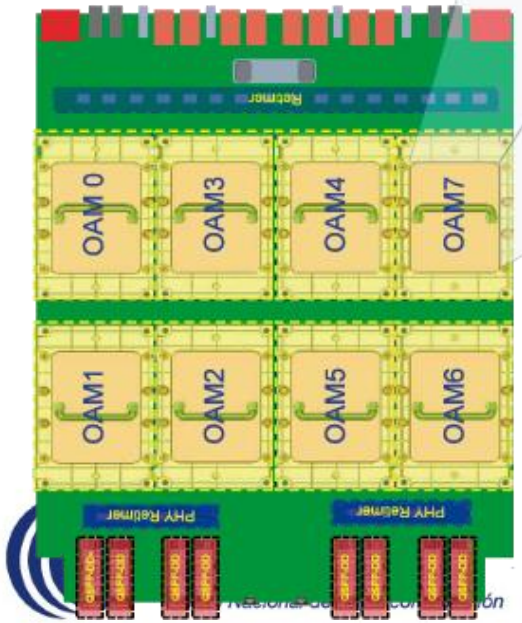
IoT to HPC, AI/ML/DL

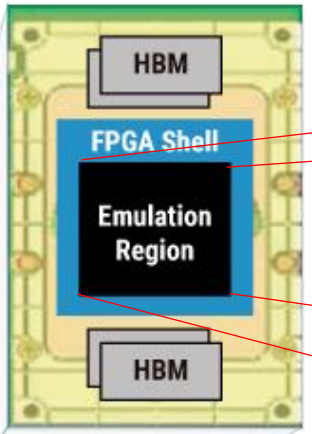
Performance Optimisation and Productivity

OmpSs-2 Programming Model

OpenMP

LINUX





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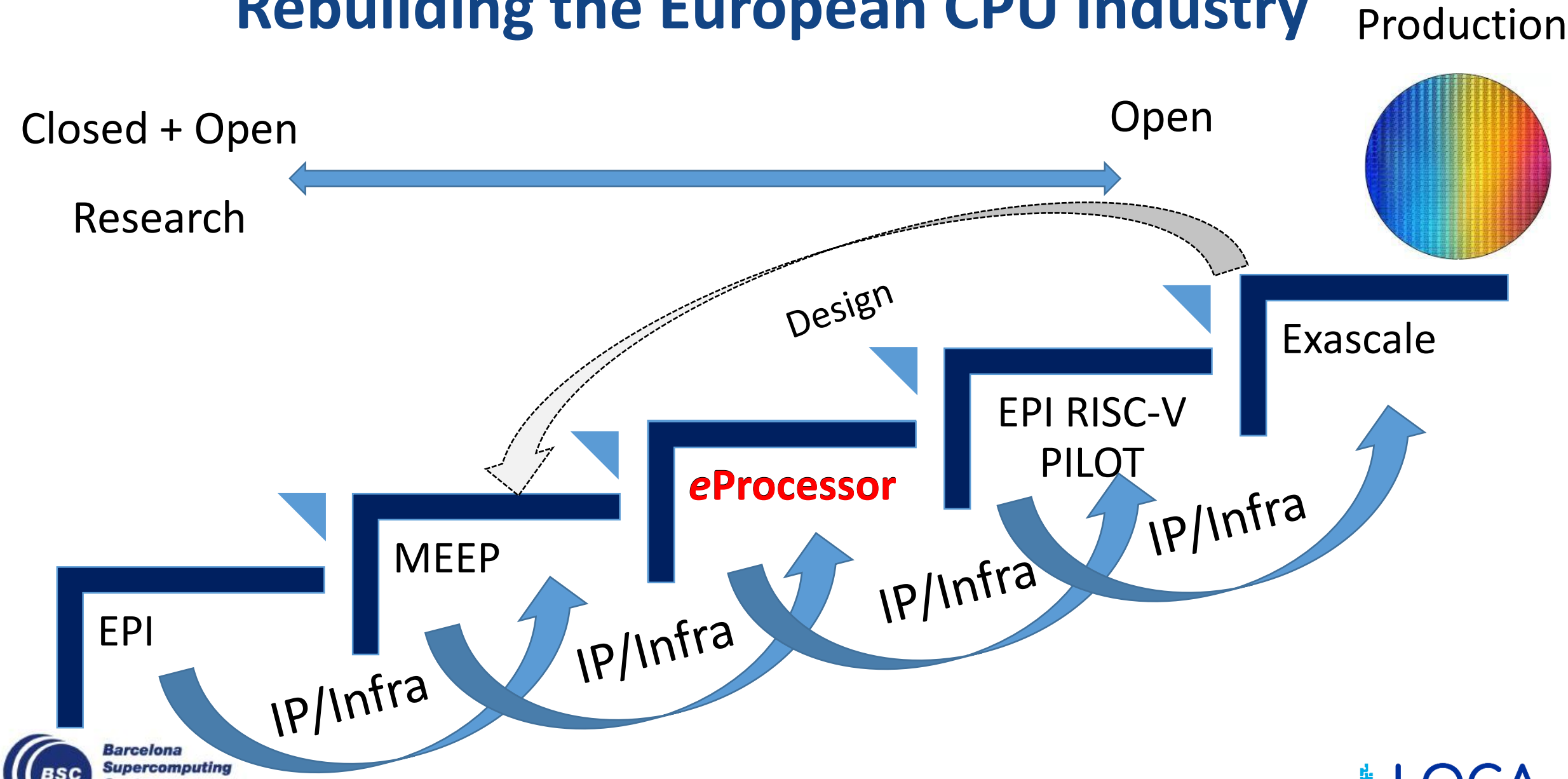

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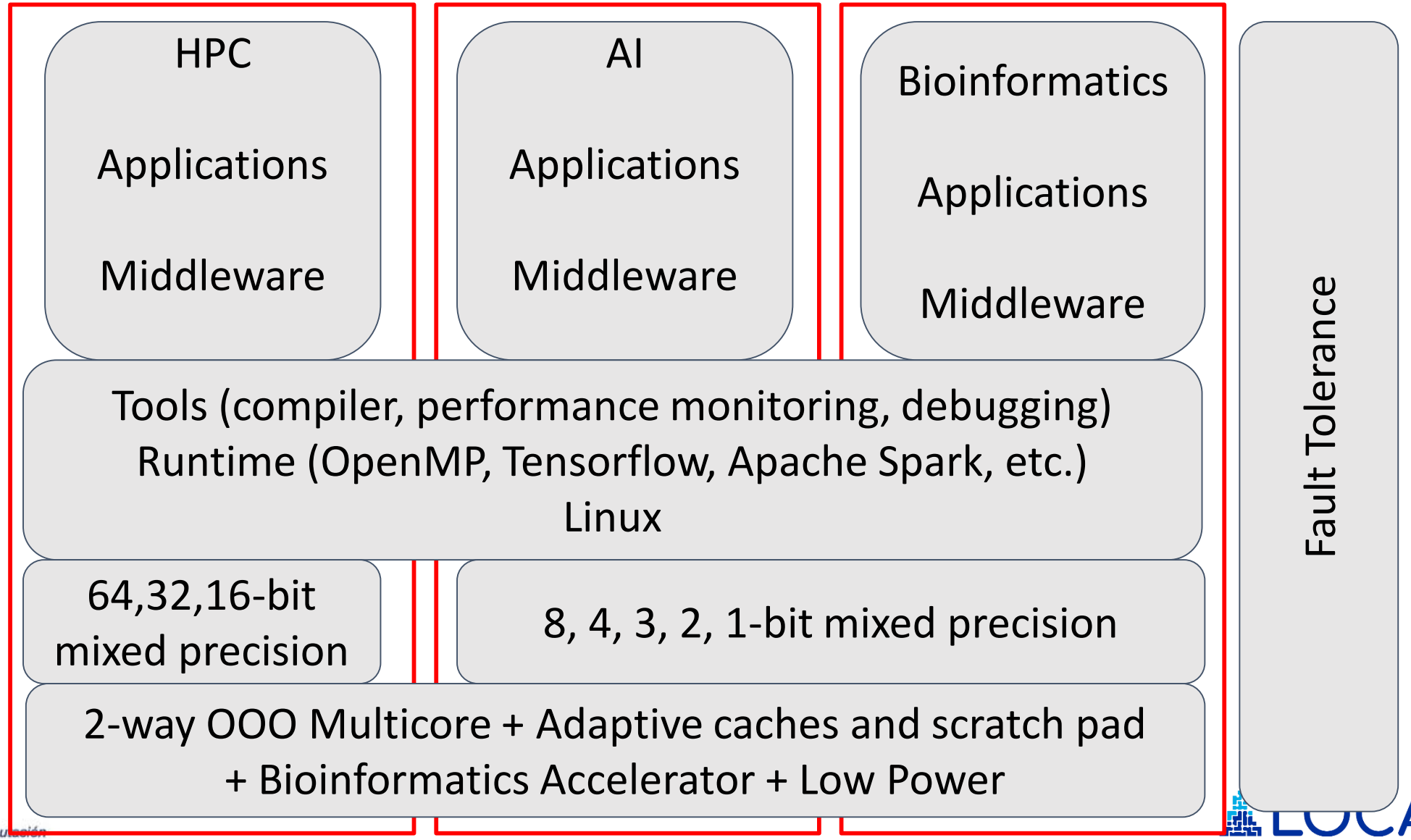
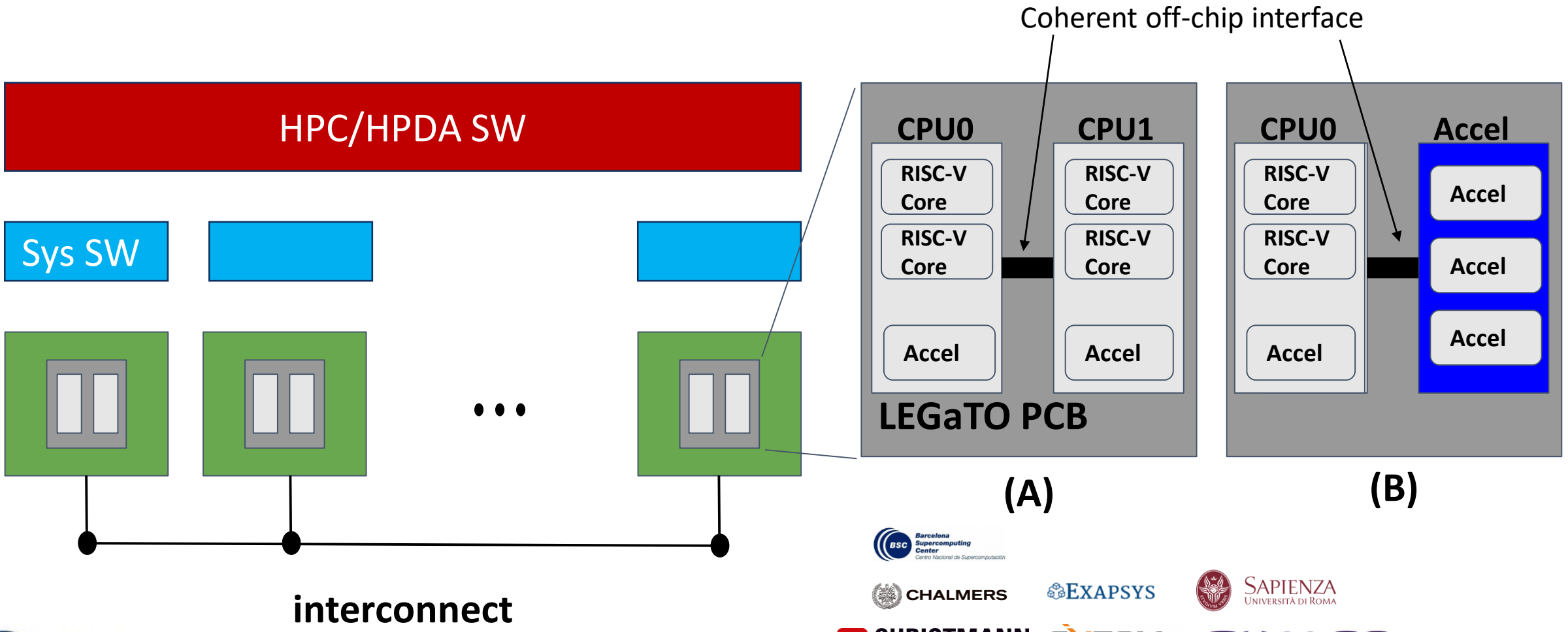
*e*Processor Stack



eProcessor System diagram



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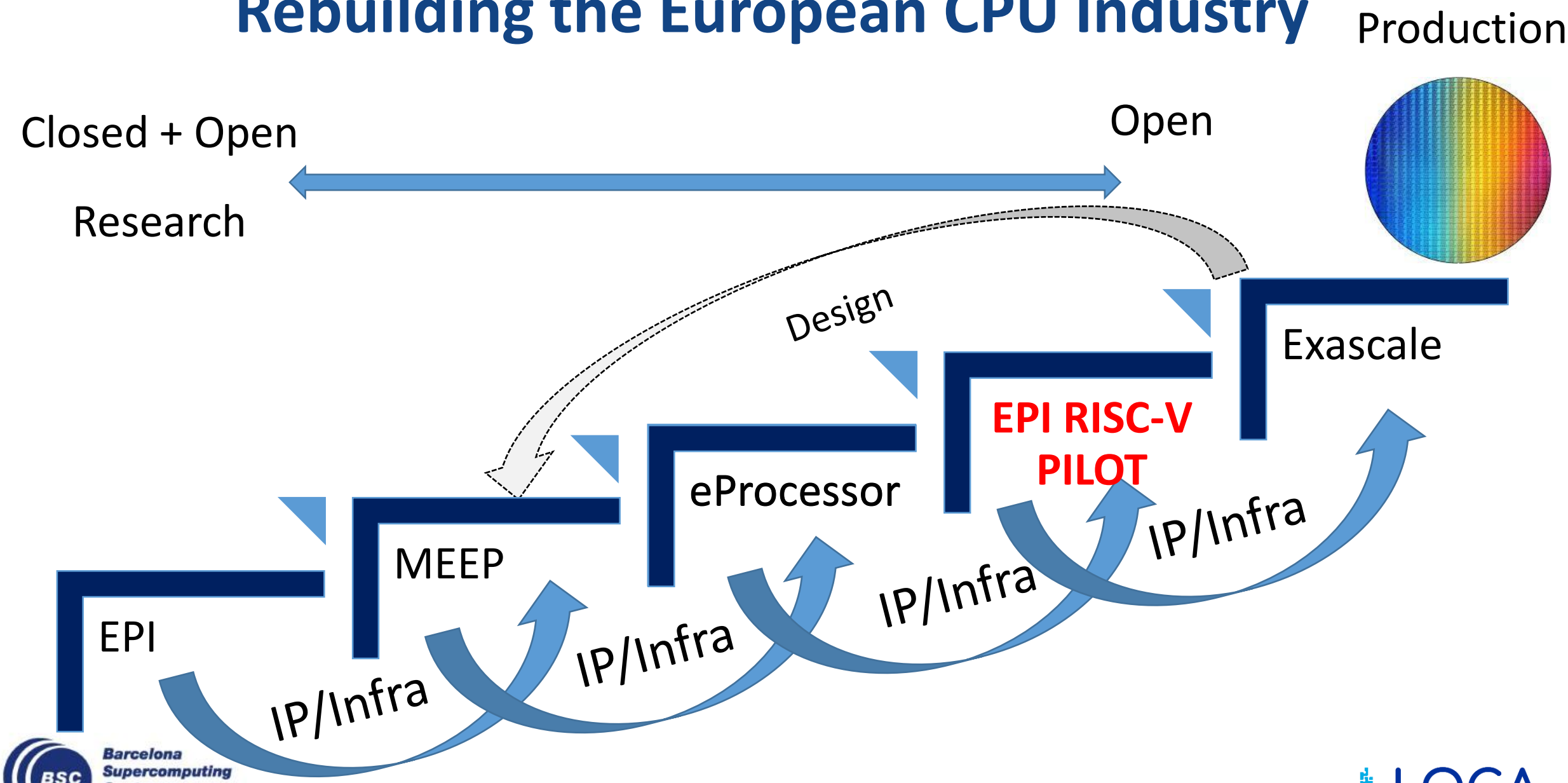

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The European PILOT

Stream 2: PILOT SW Stack

	HPC Vector	ML/AI/Stencil
Applications:	GROMACS, EC-EARTH, MD + AI	Video, BERT
SW Libraries:	FFT, BLIS, Video, oneDNN, Neural Net, MLS-DNN	
AI Framework:	Tarantella, Tensorflow, Dace	
Runtime & Schedulers:	MPI, OpenMP, DLB, TAMPI	
System SW:	BeeGFS, SLURM, DROM, Boot, Drivers, Linux, BBQUE	
Toolchain:	Inference Engine, LLVM	

VEC Accel

MLS Accel

Accelerator Chips

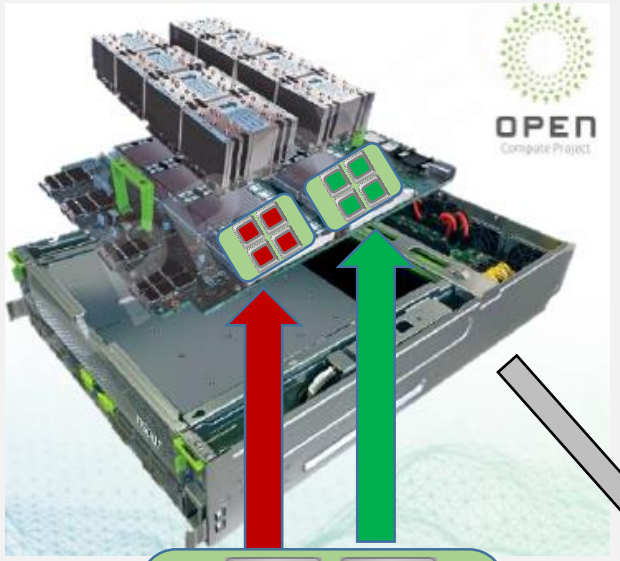
VEC

MLS

Stream 3: European RISC-V Accelerators

Stream 4: European PILOT

Accelerator Chassis



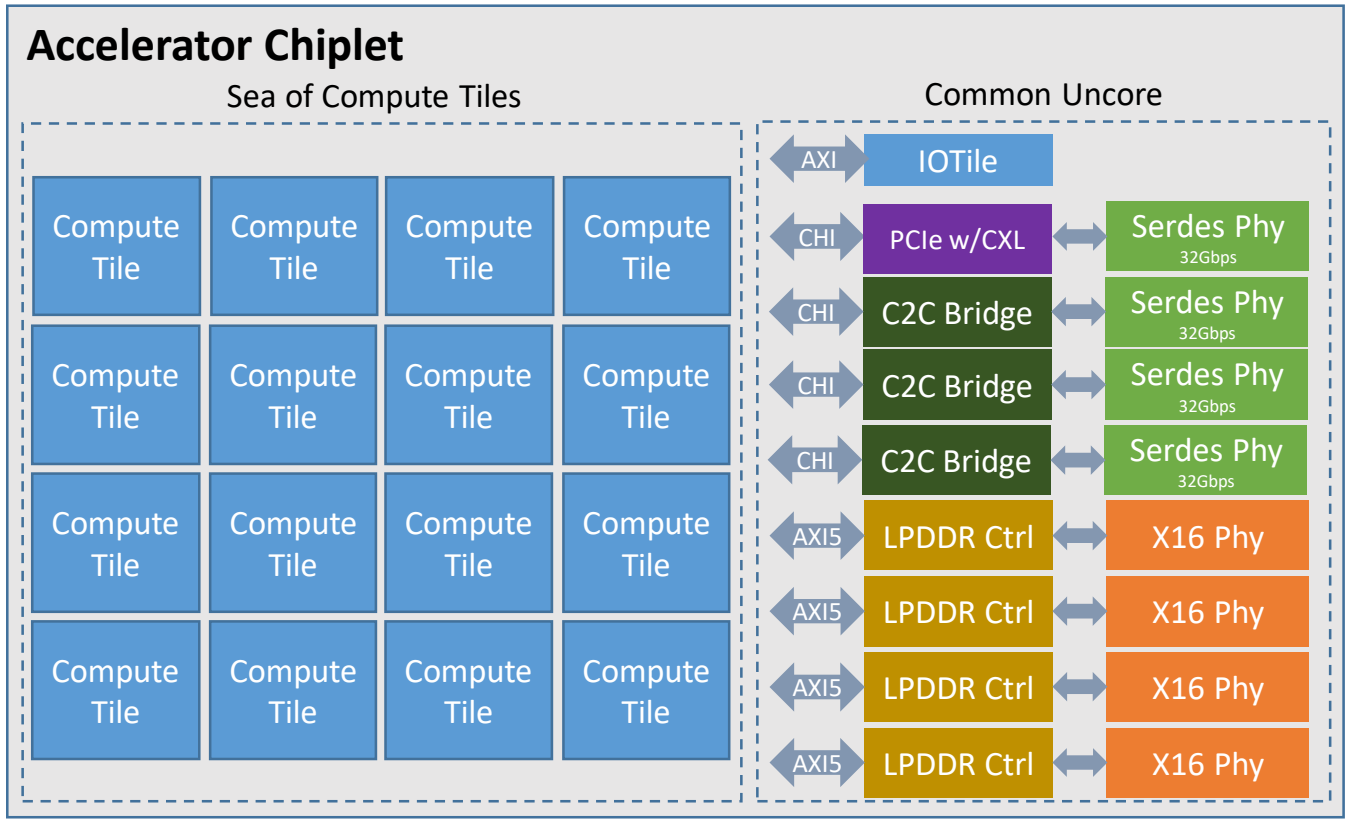
Arm (Rhea, etc.)
and/or x86 **host**

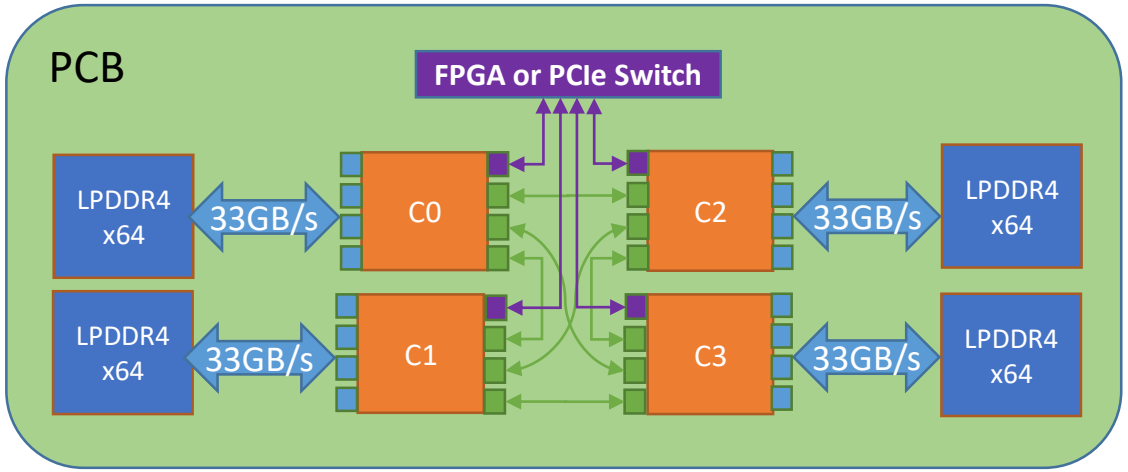
+

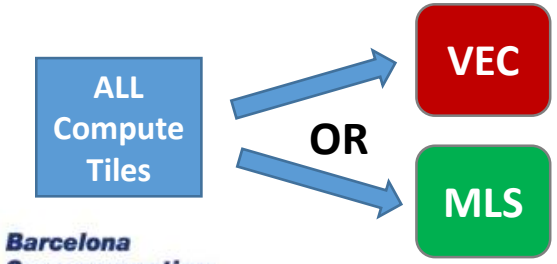
Accelerator PCB Cards

Immersive Cooling

The European PILOT Accelerator Architecture







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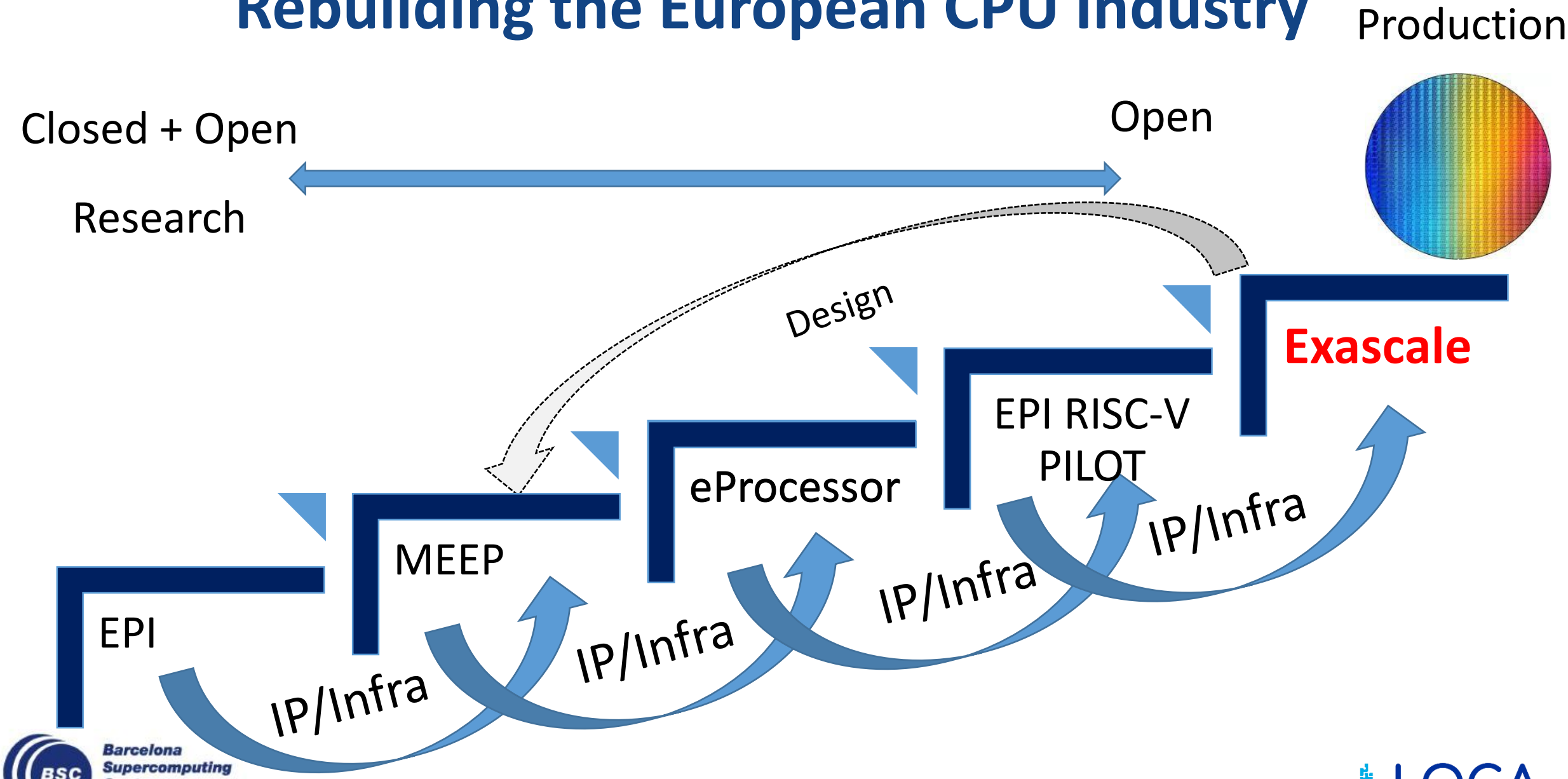

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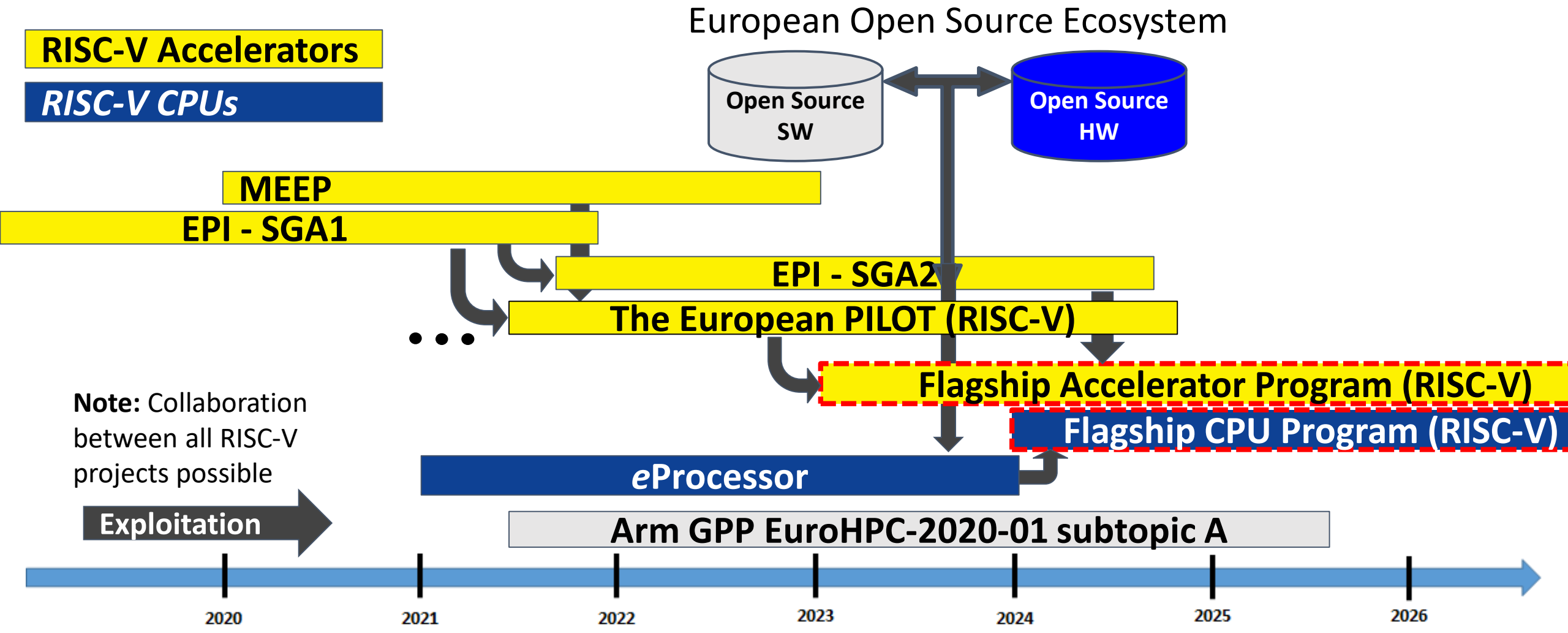
The Future: Flagship RISC-V Exascale Accelerator



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A Successful EC Roadmap for the Future

- Embrace Open Source Hardware
  - Build infrastructure to support open source
  - Create an environment that links research to the ICT industry
  - Supported by DG Connect and other funding instruments
- Teach, train, and collaborate
- Leverage the Global Technology ecosystem
- Requires **SIGNIFICANT** funding for programs to build made in Europe IP
  - Many **focused** projects: Horizon Europe, Digital Europe, …
  - Many **focused** teams: Collaborative IP and TRL development
  - Total and integrated vision for the future
  - Large Accelerator and CPU investment **(> 1B€)**

The Future is Wide Open!

- There is an urgent need, from mobile phones to supercomputers: more compute at lower power
- The RISC-V ecosystem is in the nascent period where it can become the de facto open hardware platform of the future
  - An opportunity for Europe to lead the charge to creating a full stack solution for everything, from supercomputers down to IoT devices

- Our main goal: Create European chips that meet the needs of future European and global markets across HPC, cloud, automotive, mobile to IoT

- **This is the framework for the Exascale Supercomputing Initiative at BSC**

Focus, Freedom, and Forward

- BSC is embracing a Open Source Hardware to complement OSS
  - RISC-V has the momentum to succeed as the Open Source ISA, much like Linux
- BSC is building the infrastructure to support the future of computing
  - Combining applications, system software, hardware design and hardware
- BSC can organize and coordinate full stack efforts
  - More resources = faster time to success
  - More partners (Academia/Industry)
  - Research/Resource multiplier
- Europe and the world can unite around the BSC Vision to move forward faster, together

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

BSC is Made in Europe

LOCA is Bigger than Barcelona!

Casteller
(human tower)

LOCA
European Laboratory for Open Computer Architecture

European Open Hardware, Architecture Initiative

We must stand on the shoulders of giants to build great things.
We are assembling many giants and hope you can join us.

Thank you

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