European Processor Initiative: Second year of activities

The project is finishing its second year ready to unveil updated roadmap

The European Processor Initiative, a project with 27 partners from 10 European countries, with the goal of helping the EU achieve independence in HPC technologies, is finishing its second year of activities.

Despite 2020 bringing upon our young efforts the circumstances that were previously unimaginable, causing the subsequent cancellation of the first-ever planned European Processor Initiative Forum, the partners in the Initiative managed to stay the course and maintain all activities in all designated streams.

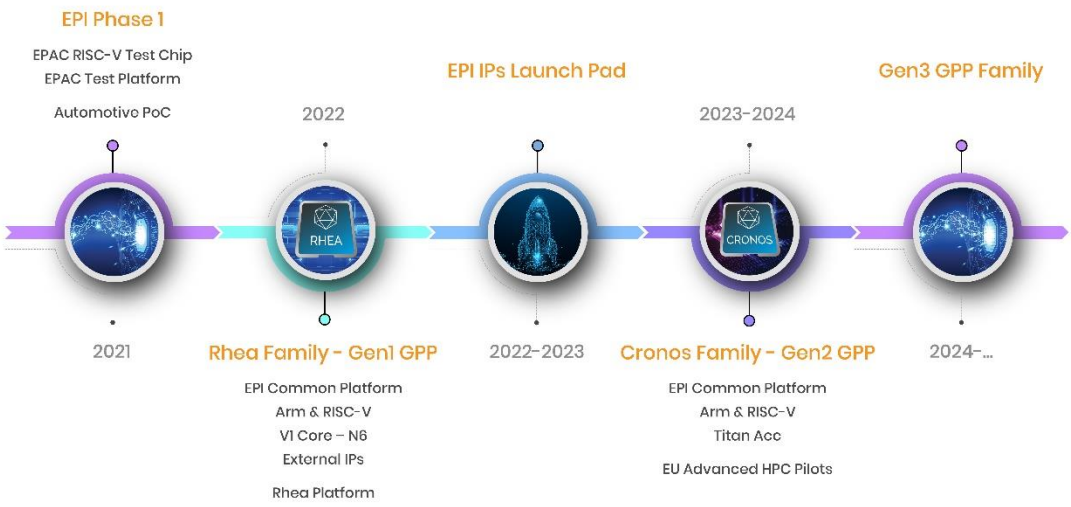
The year began with our latest partner, SiPearl, launching to start their activities dedicated to developing commercialized implementations of our technology. Very soon after announcing their presence on the global stage, SiPearl signed a licensing agreement with Arm and opened a branch in Germany.

At the same time, European Processor Initiative partners have finalized the first version of our RISC-V accelerator architecture, named EPAC, and we look forward to the delivery of the first European Processor Initiative silicon featuring EPAC Test Chip in the exciting year that follows. The EPAC Test Chip silicon will be complemented with PCIe EPAC Test Platform enabling the test and enhancements of the architecture for future revisions.

At the software level, we already have a compiler supporting RISC-V vector intrinsics and automatic parallelization of C/C++ codes. We are evaluating the generated code on emulation platforms that provide detailed insight for the holistic co-design of applications, compiler, and architecture. We also have other software development vehicles (SDV) where we are adapting the Operating System for the Heterogeneous ARM+RISC-V architecture of the European Processor Initiative project.

Our automotive activities in the previous year have been focused on the design of state-of-the-art automotive high-performance computing proof-of-concept with the ambition to demonstrate how European Processor Initiative IP will enable future ADAS functionality, paving the way to exploit the GPP, the RISC-V platform, the Kalray MPPA, and the Menta eFPGA IP.

Based on this project progress, the Consortium is ready to announce the updated project roadmap shown below:



European Processor Initiative will, together with colleagues from other European exascale projects, attend the virtual Supercomputing20, where we will showcase our latest developments and update to the roadmap. We invite you to attend our virtual booth and join in the lively discussions about the future of HPC!