



# THE EUROPEAN APPROACH FOR EXASCALE AGES

THE ROAD TOWARD SOVEREIGNTY

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Chairman of the Board

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# THE EUROPEAN COMMISSION & HPC



## European Commission President Jean-Claude Juncker

*« Our ambition is for Europe to become one of the top 3 world leaders in high-performance computing by 2020 »*

Paris, 27 October 2015



## Vice President Andrus Ansip

*« I encourage even more EU countries to engage in this ambitious endeavour »*

Digital Day Rome, 23 March 2017

Ministers from seven MS (France, Germany, Italy, Luxembourg, Netherlands, Portugal and Spain) sign a declaration to support the next generation of computing and data infrastructures

# THE NEW COMMISSION HAS SET NEW AMBITIONS



## Letter of mission\* (extracts)

- task for the next five years is to put in place the right framework to allow Europe to make the most of the digital transition, while ensuring that our enduring values are respected as new technologies develop.
- Enhance Europe’s Technological Sovereignty
  - blockchain, high-performance computing, algorithms, and data-sharing and data-usage tools.
  - 5G-Networks
  - Artificial Intelligence & Digital Services Act
  - Single Market for cybersecurity
  - Joint Cyber Unit
  - Digital Education Action plan

\* [https://ec.europa.eu/commission/sites/beta-political/files/president-elect\\_von\\_der\\_leyens\\_mission\\_letter\\_to\\_thierry\\_breton.pdf](https://ec.europa.eu/commission/sites/beta-political/files/president-elect_von_der_leyens_mission_letter_to_thierry_breton.pdf)

# EPI OBJECTIVES

- Overall: Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments
  - Short-term objective
    - supply the EU-designed microprocessor to empower the EU Exascale machines
  - Long-term objective
    - Europe needs a sovereign (=not at risk of limitation or embargo by non-EU countries) access to high-performance, low-power microprocessors, from IP to products
  - EPI has been set to fulfil this objective
  - EPI has to cover all Technical Readiness levels (TRL)
    - TRL 1-3 are for long-term objectives (EU IP)
- \*and\*
- TRL 4-9 are for short to mid-term objectives with products designed in EU





# FROM OBJECTIVES TO ROADMAP

Dec. 2018

2019 → 2020 → 2021 →

2022

2023

>2023

**arm**  
Short term  
objective

mid term  
objective



General purpose processor  
(Gen I)  
ARM ZEUS Core


Common Platform 

EPAC IP development  
& Test chip (22nm)

7nm

GA

EuroHPC  
ExaScale  
machines

GPP (Gen2)-  
ARM >ZEUS Core  SIPEARL

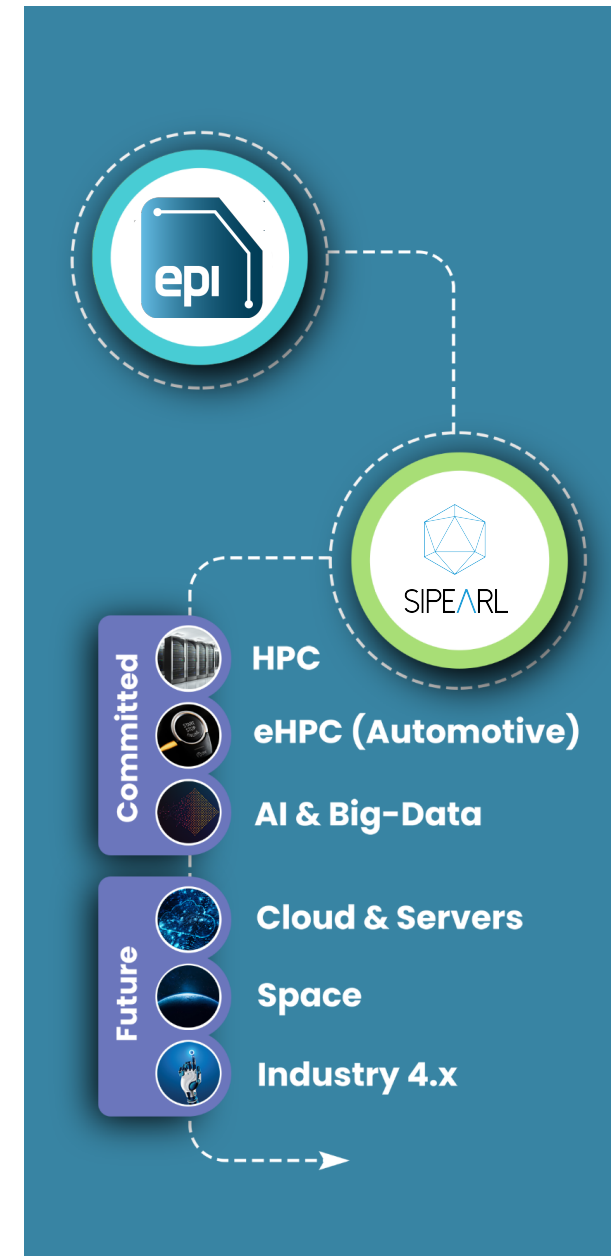
EPAC based  
Accelerator

# 27 PARTNERS FROM 10 EU COUNTRIES



# FROM IPR TO PRODUCTS FROM EPI TO SIPEARL

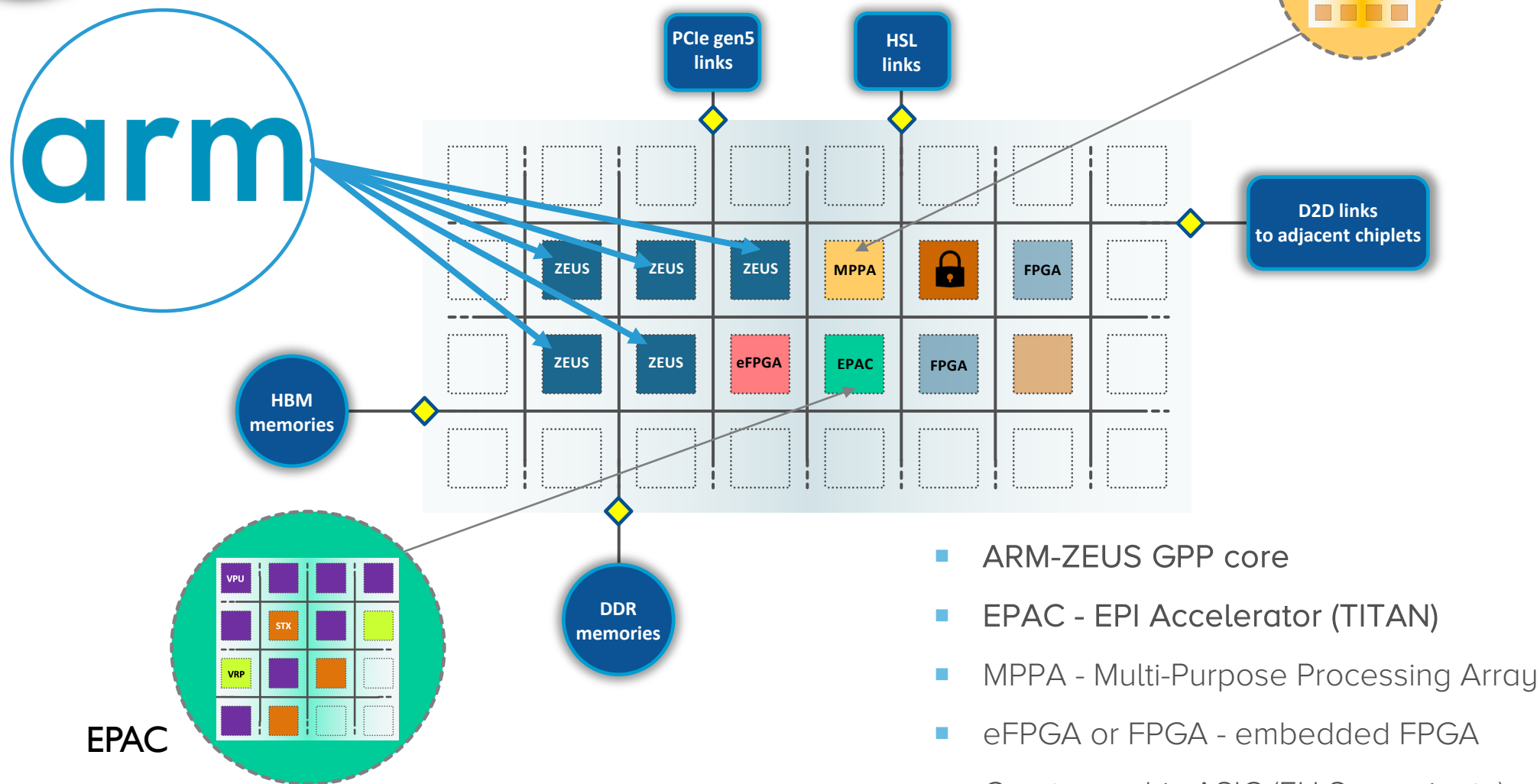
- SIPEARL is
  - Incorporated in EU (France)
  - the industrial and business ‘hand’ of EPI
  - the Fabless company
- licence of IPs from the partners
- develop own IPs around it
- licence the missing components from the market
- Raise in equity the missing budget (~100M€)
- generate revenue from both the HPC, IA, server and eHPC markets
- integrate, market, support & sell the chip
- work on the next generations



# TECHNOLOGY



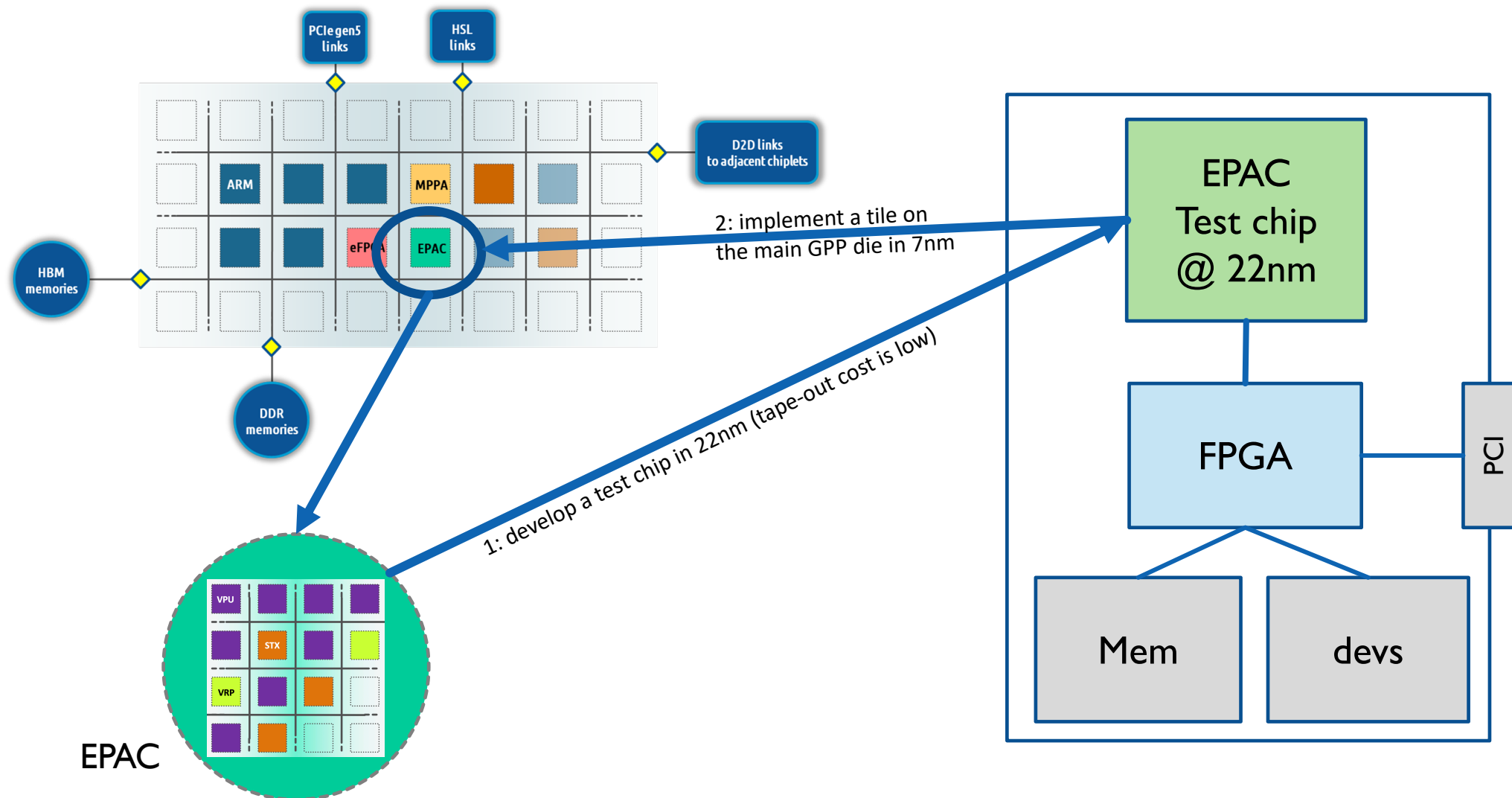
# GPP ARCHITECTURE CONCEPT



- ARM-ZEUS GPP core
- EPAC - EPI Accelerator (TITAN)
- MPPA - Multi-Purpose Processing Array
- eFPGA or FPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)

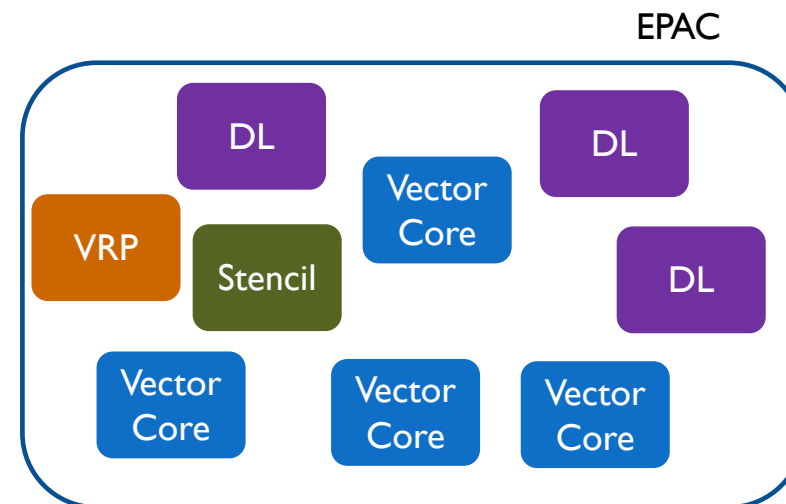


# EPAC OUTCOMES



# EPAC IN A NUTSHELL

- **Develop** and demonstrate **fully European** processor IPs based on the RISC-V ISA
  - Build on existing EU IP, leverage EU background and vision
- Provide a very **low power** and high computing throughput **accelerator**
  - HPC
  - Emerging → Automotive
- Key Ips
  - Vector Core: HPC cores for FP64
  - NTX: neuro stream accelerator for Deep Learning
  - Stencil: Specialized accelerator for Stencil computation
  - VRP: Extended variable precision arithmetic (>64 bits)



# RISC-V LONG VECTORS – HARDWARE & SOFTWARE

- Vector Length Agnostic : Dynamically adapt algorithmic structure to architecture
- Hierarchical balance between granularity levels (architecture and programming)
  - MPI – OpenMP (Nesting) - Long Vectors
  - “Limited” number of control flows
- Long vectors
  - Latency → throughput: decouple Front end – back end
  - Potential to optimize memory throughput: Convey access pattern semantics to the architecture, Locality hints ...
- ISA is important
  - Leverage system software technologies (Operating system, Compiler)

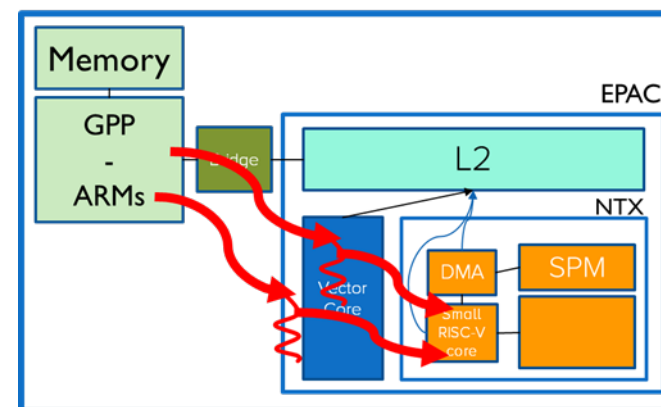
- MPI + OpenMP
  - Offloading
  - Tasks
  - SIMD
  - Specific language extensions

```
void axpy_omp_nest_3 (double a, double *dx, double *dy, int n) {
    int i, chunk;

    #pragma omp taskloop
    for (i=0; i<n; i+=TS) {
        chunk= n>i+TS? TS : n-i;
        #pragma omp target map(to:dx[i:i+chunk], tofrom:dy[i:i+chunk])
        axpy_omp      (a, &dx[i], &dy[i], chunk);
    }
}
```

```
void axpy_SIMD      (double a, double *dx, double *dy, int n) {
    int i;

    #pragma omp simd
    for (i=0; i<n; i++) {
        dy[i] += a*dx[i];
    }
}
```



# PERSPECTIVES AND CHALLENGES



# BY 2022-23, EPI DELIVERS!

- A General Purpose Processor for HPC machines can be developed in EU by a EU Company (SiPearl)
- The fundamental IPs for a 100% European HPC Accelerator, based on RISC-V®, can be developed in EU
- The expertise for developing high-end and complex processing units in Europe, after decades of dis-investment
- We'll be ready to move to the next step: engage on the development on a general purpose processor.





## (CHALLENGES FOR) THE NEXT YEARS – 1/2

- This MUST be a progressive multi-years approach, over 5 years or more. We have to move up on the TRL scale.
- Some IP are extremely difficult to develop. Competencies are rare and very expensive.
- Ecosystem in the datacenter and high-end space does not exist yet but can be created and be enlarged over the next 5 years.

# (CHALLENGES FOR) THE NEXT YEARS – 1/2



The road to a RISC-V GPP be progressive, multi-years approach, over 5 years or more. We have to move up on the TRL scale.



Some IP are extremely difficult to develop. Competencies are rare and expensive.



SW Ecosystem in the datacenter and high-end space does not exist yet. It has to be created and be enlarged over the next years.

# (CHALLENGES FOR) THE NEXT YEARS – 2/2

- Main challenges are related to industrialization and associated costs
  - >\$50M are required to develop a PRODUCT manufactured with advanced processes (5nm or better)
  - Only large corporation could offer this investment level (or investment funds)
  - First question *'do I make money out of my investment?'*
  - Such private investors are rare in Europe because investment is huge and return on investment is long with a very high risk
- Competition is well established (X86, ARM) and comes with proven solutions with a rich ecosystem
- Nobody knows where the processor market will be in 5 years
  - Other (open) instruction sets could rise
  - Between now and 2025 several RISC-V based solution could be put on the market and fail, scaring future investors
- The RISC-V IP ecosystem could become fragmented with many proprietary forks (like it happened with Linux)

# THANK YOU FOR YOUR ATTENTION



# European Processor Initiative



[www.european-processor-initiative.eu](http://www.european-processor-initiative.eu)

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