
European Processor Initiative


# THE EUROPEAN APPROACH FOR EXASCALE AGES

## THE ROAD TOWARD SOVEREIGNTY

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Chairman of the Board

THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION'S HORIZON 2020 RESEARCH AND INNOVATION PROGRAM UNDER GRANT AGREEMENT NO 826647

# THE EUROPEAN COMMISSION & HPC

**European Commission President**
**Jean-Claude Juncker**

*« Our ambition is for Europe to become one of the top 3 world leaders in high-performance computing by 2020 »*

Paris, 27 October 2015


**Vice President**
**Andrus Ansip**

*« I encourage even more EU countries to engage in this ambitious endeavour »*

Digital Day Rome, 23 March 2017

Ministers from seven MS (France, Germany, Italy, Luxembourg, Netherlands, Portugal and Spain) sign a declaration to support the next generation of computing and data infrastructures

EuroHPC Joint Undertaking

# THE PRESIDENT OF THE EUROPEAN UNION HAS SET NEW AMBITIONS

SEPTEMBER, 16TH, 2020

**Ursula Von Der Lyen**
**State of the Union**
***Brussels – September, 16th, 2020***

- NextGenerationEU is also a unique opportunity to develop a more coherent European approach to connectivity and digital infrastructure deployment.
- None of this is an end in itself - it is about Europe's digital sovereignty, on a small and large scale.
- In this spirit, I am pleased to announce an **investment of 8 billion euros in the next generation of supercomputers** - cutting-edge technology made in Europe.
- And **we want the European industry to develop our own next-generation microprocessor** that will allow us to use the increasing data volumes energy-efficient and securely.
- This is what **Europe's Digital Decade** is all about!

https://ec.europa.eu/commission/presscorner/detail/en/SPEECH_20_1655

# EPI OBJECTIVES

- Overall: Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments
- Short-term objective
  - supply the EU-designed microprocessor to empower the EU Exascale machines
- Long-term objective
  - Europe needs a sovereign (=not at risk of limitation or embargo by non-EU countries) access to high-performance, low-power microprocessors, from IP to products
- EPI has been set to fulfil this objective
- EPI has to cover all Technical Readiness levels (TRL)
  - TRL 1-3 are for long-term objectives (EU IP)

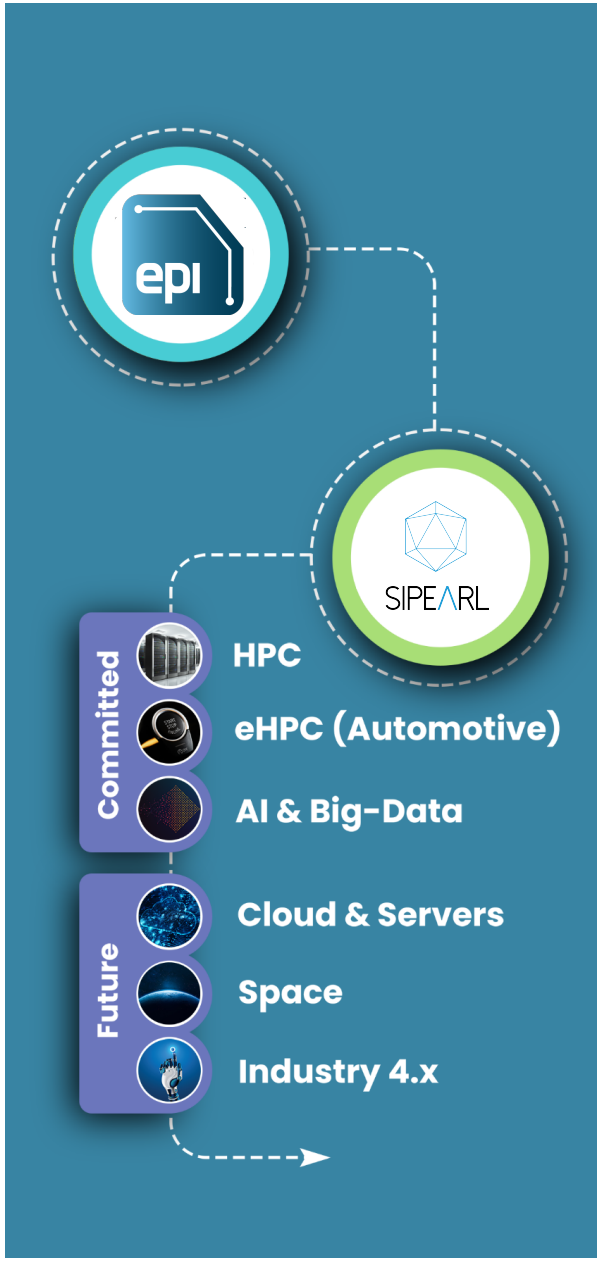
*and*

  - TRL 4-9 are for short to mid-term objectives (decade) with products designed in EU

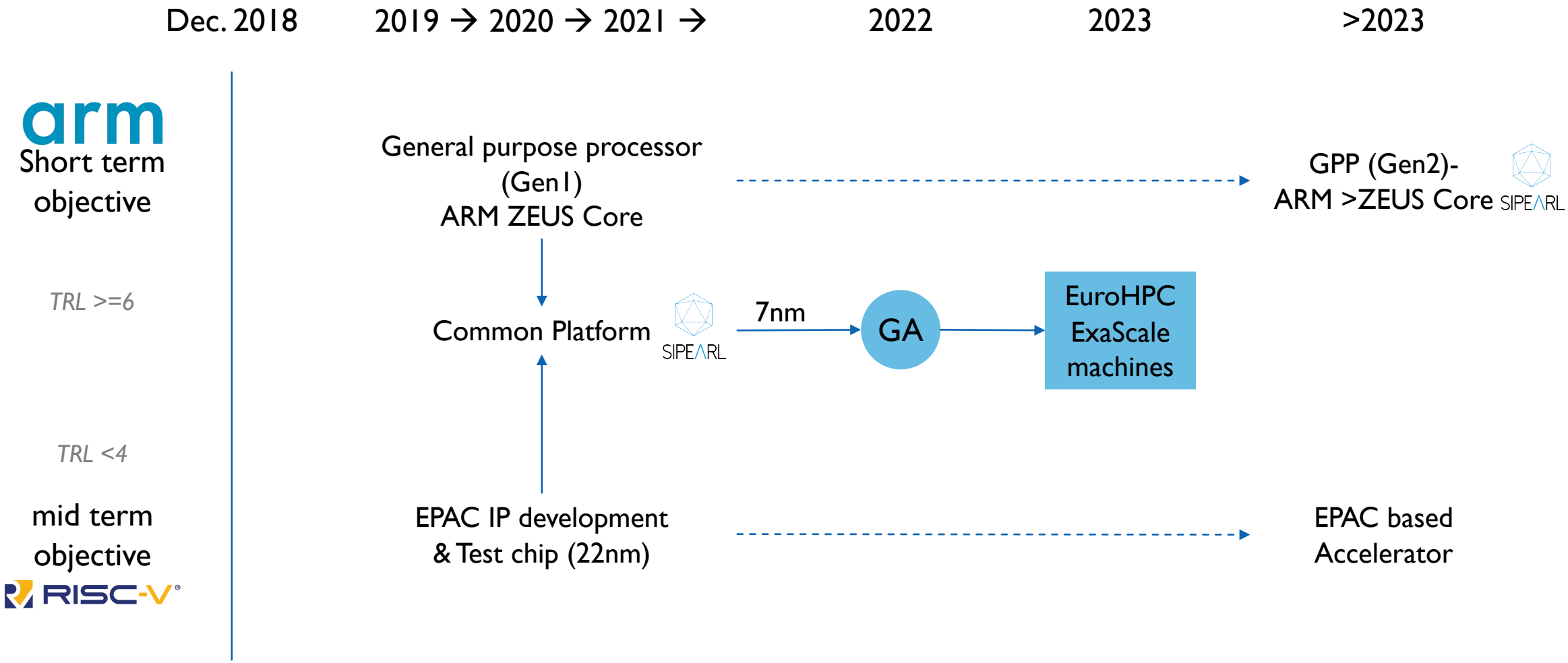
# 27 PARTNERS FROM 10 EU COUNTRIES

# FROM **IPR** TO **PRODUCTS**
# FROM **EPI** TO **SIPEARL**

- SIPEARL is
  - Incorporated in EU (France)
  - the industrial and business ‘hand’ of EPI
  - the Fabless company
- licence of IPs from the partners
- develop own IPs around it
- licence the missing components from the market
- Raise in equity the missing budget (~100M€)
- generate revenue from both the HPC, IA, server  and eHPC markets
- integrate, market, support & sell the chip
- work on the next generations



# FROM OBJECTIVES TO ROADMAP, FROM ROADMAP TO PRODUCTS



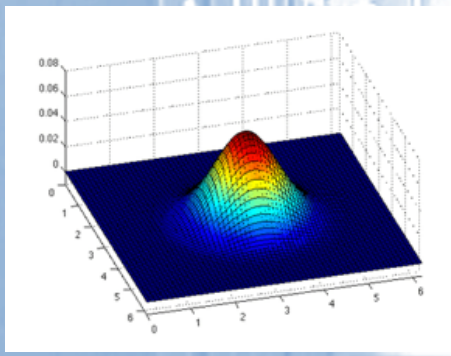
# TECHNOLOGY
# PART I – EXASCALE SUPERCOMPUTERS

# HPC BEFORE ARTIFICIAL INTELLIGENCE

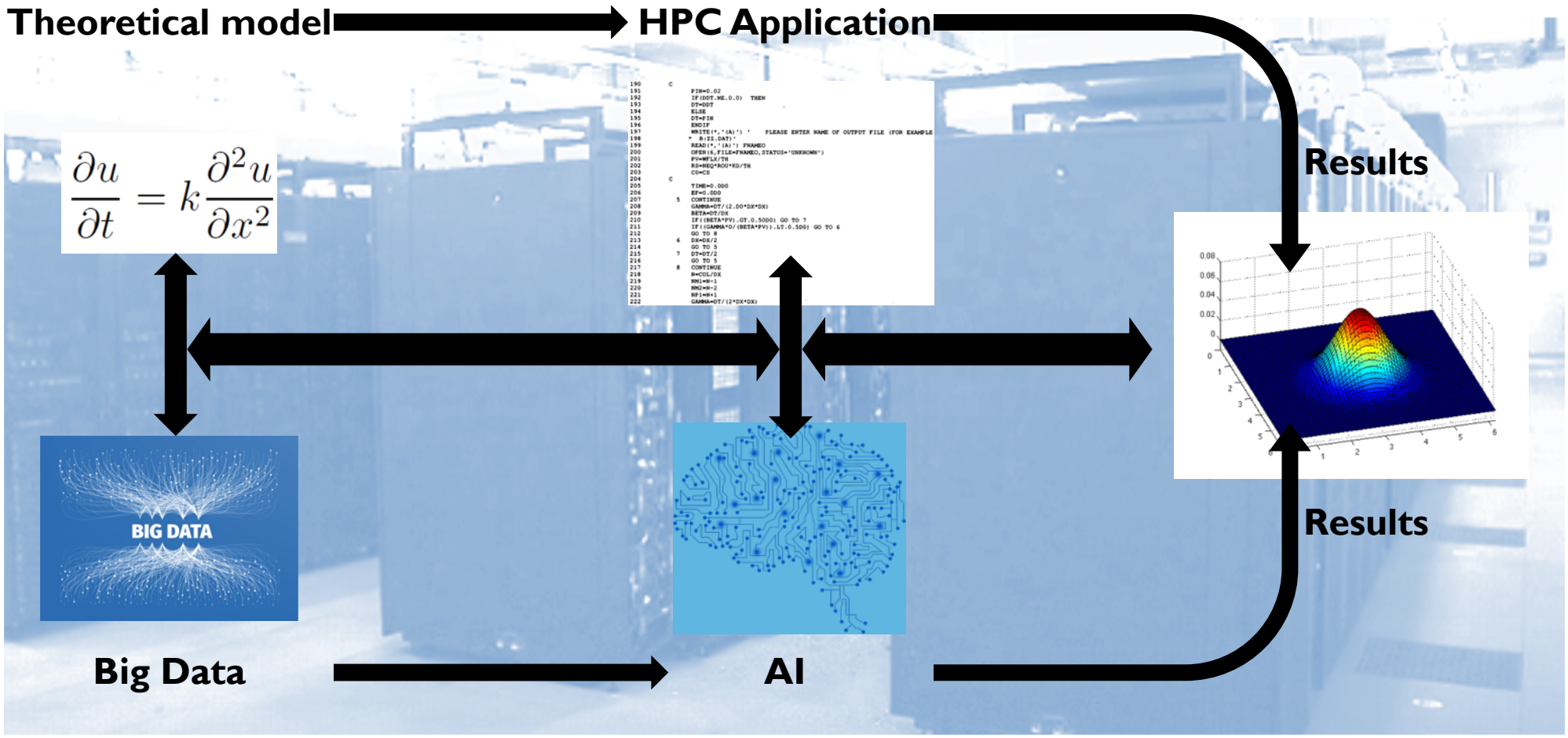
**Theoretical model** → **HPC Application** → **Results**

$$\frac{\partial u}{\partial t} = k \frac{\partial^2 u}{\partial x^2}$$

```
      C
            PIN=0.02
            IF(DDT.NE.0.0)  THEN
            DT=DDT
            ELSE
            DT=PIN
            ENDIF
            WRITE(*,'(A)') '    PLEASE ENTER NAME OF OUTPUT FILE (FOR EXAMPLE
           *  B:ZZ.DAT)'
            READ(*,'(A)') FNAMEO
            OPEN(6,FILE=FNAMEO,STATUS='UNKNOWN')
            PV=WFLX/TH
            RS=NEQ*ROU*KD/TH
            CO=CS
      C
            TIME=0.0D0
            EF=0.0D0
        5   CONTINUE
            GAMMA=DT/(2.D0*DX*DX)
            BETA=DT/DX
            IF((BETA*PV).GT.0.5D0) GO TO 7
            IF((GAMMA*D/(BETA*PV)).LT.0.5D0) GO TO 6
            GO TO 8
        6   DX=DX/2
            GO TO 5
        7   DT=DT/2
            GO TO 5
        8   CONTINUE
            N=COL/DX
            NM1=N-1
            NM2=N-2
            NP1=N+1
            GAMMA=DT/(2*DX*DX)
```



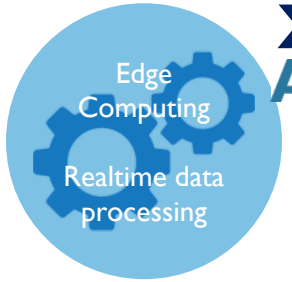
# HPC WITH ARTIFICIAL INTELLIGENCE



# HPC & AI AT EXASCALE: IT'S ALL ABOUT WORKFLOWS (1/3)

ARM


X86
ARM

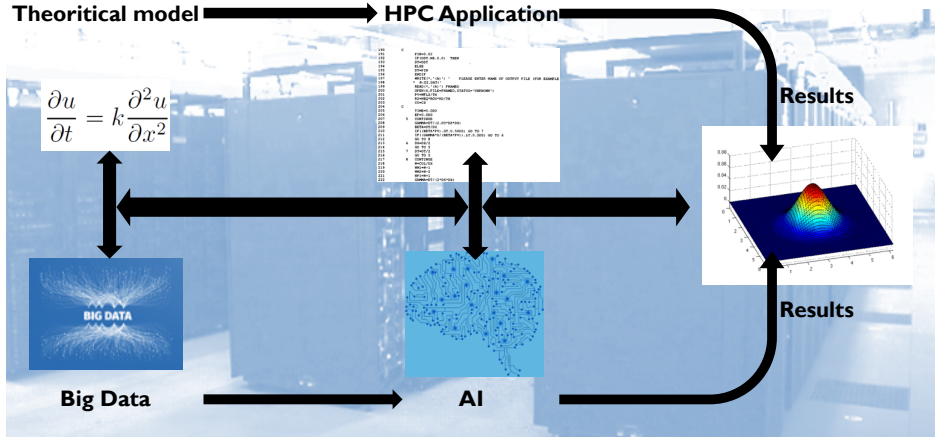



X86
ARM



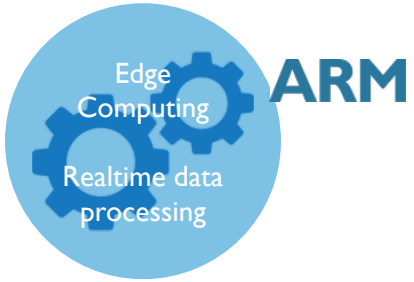
**SUMMIT**

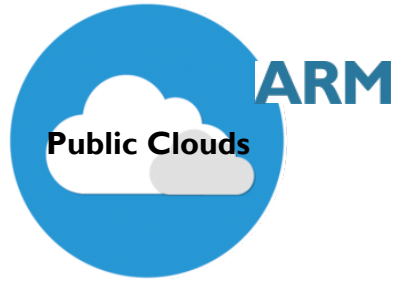
**sunway taihulight**




**FUGAKU**

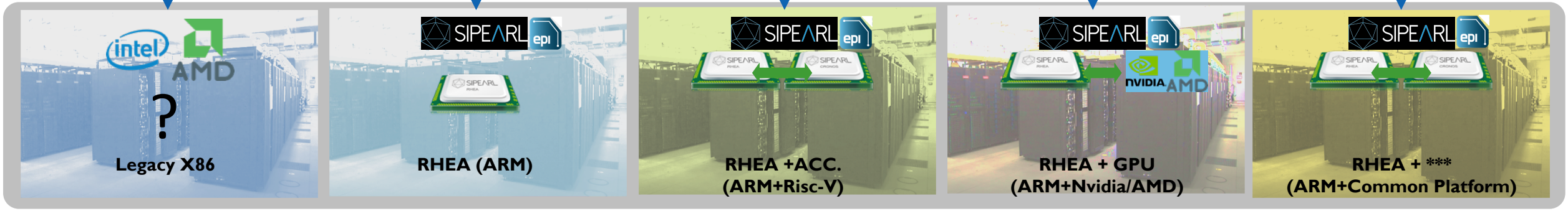
# HPC & AI AT EXASCALE: IT'S ALL ABOUT WORKFLOWS (2/3)

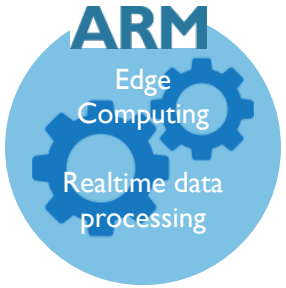




European approach


- ✓ EU Architecture
- ✓ EU HW
- ✓ EU SW
- ✓ Handle all complexity the others don't know how to



# HPC & AI AT EXASCALE: IT'S ALL ABOUT WORKFLOWS (3/3)



European approach

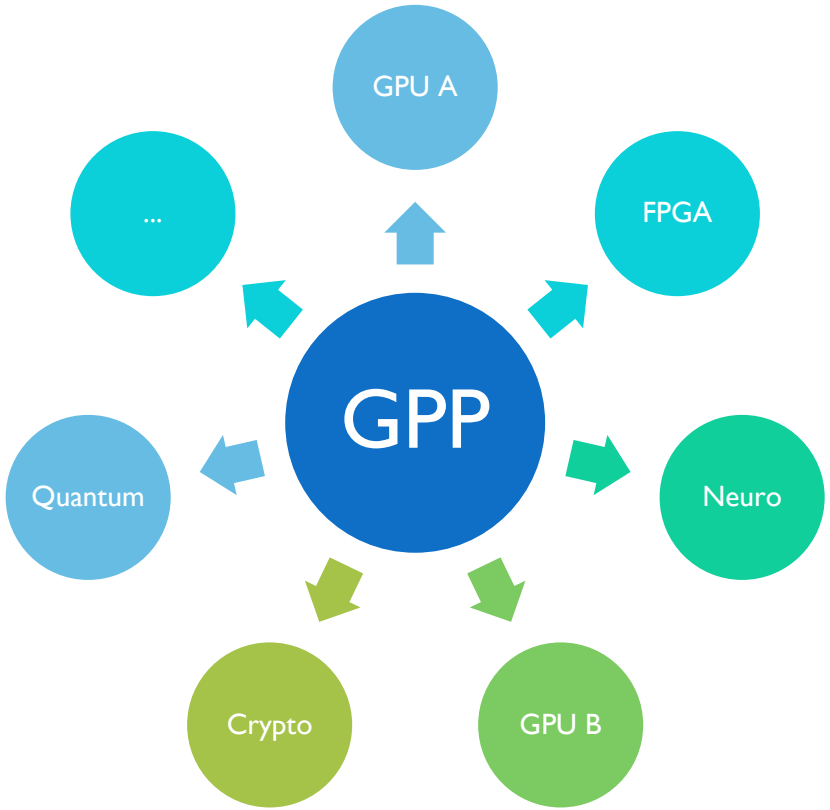

- ✓ EU Architecture
- ✓ EU HW
- ✓ EU SW
- ✓ Handle all complexity in a unified environment

**Unified environment: Compilers / programming languages / libraries**

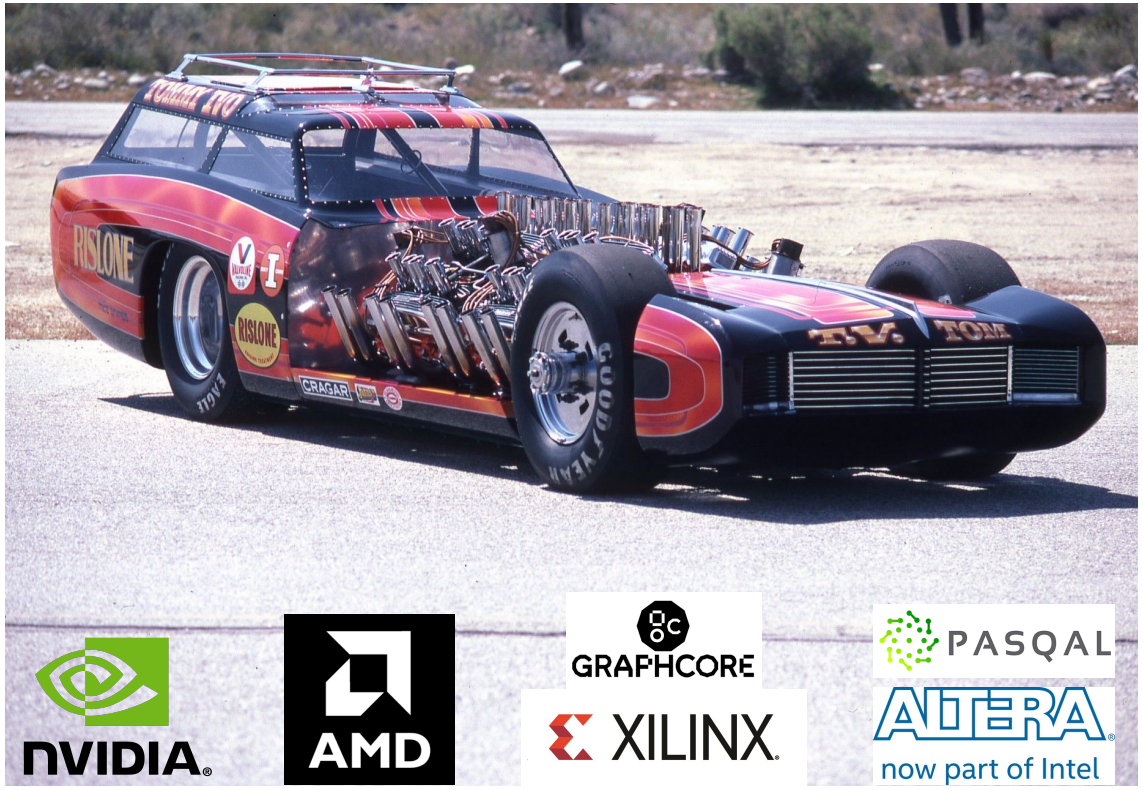
# TECHNOLOGY
# PART II – EXASCALE MICROPROCESSORS

# CONSEQUENCES

## General Purpose Processors have to be more open



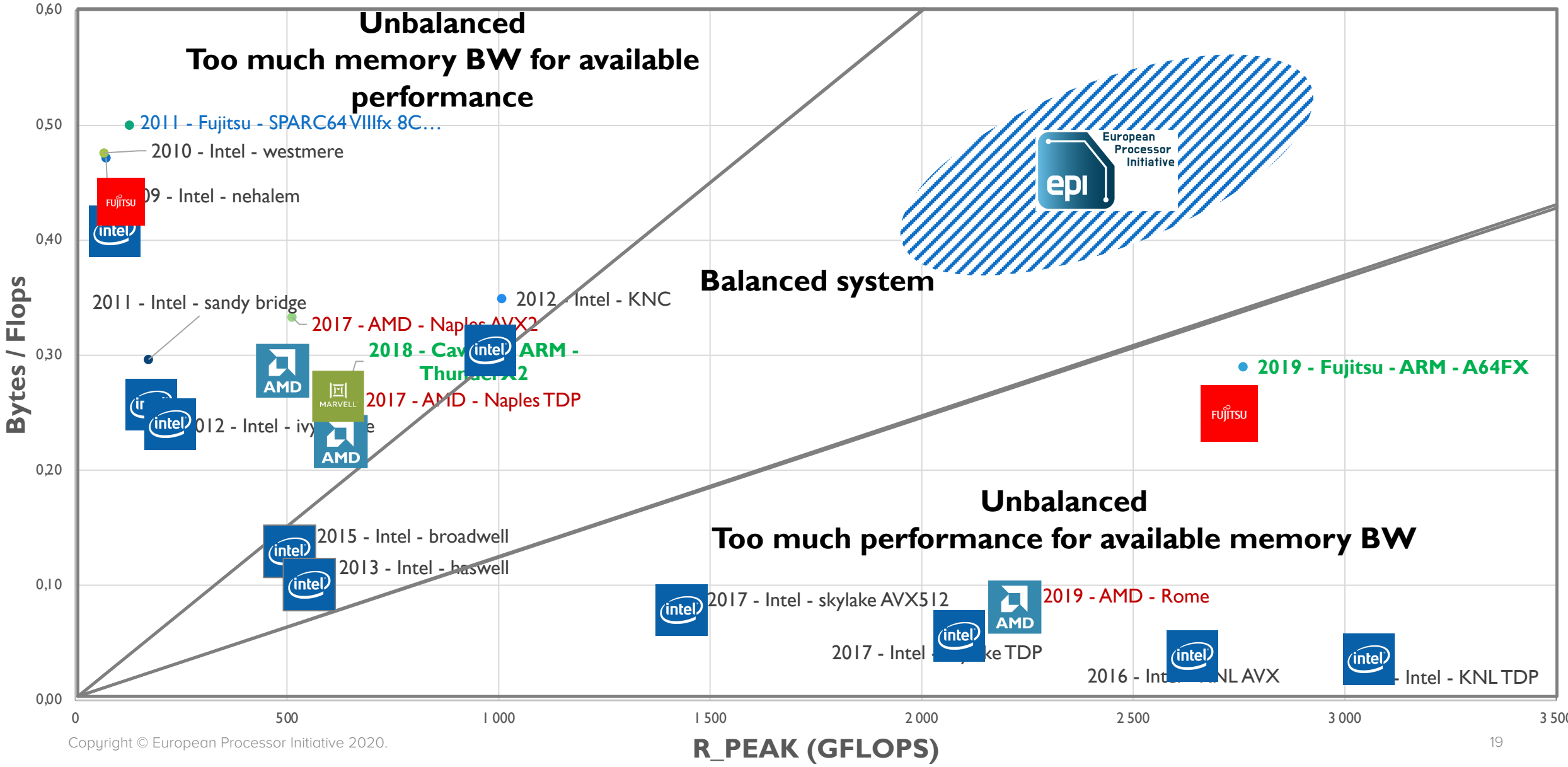

## The race to FLOPS is now in the accelerators area



# SO… WHAT TO EXPECT FROM AN EXASCALE GENERAL PURPOSE PROCESSOR?

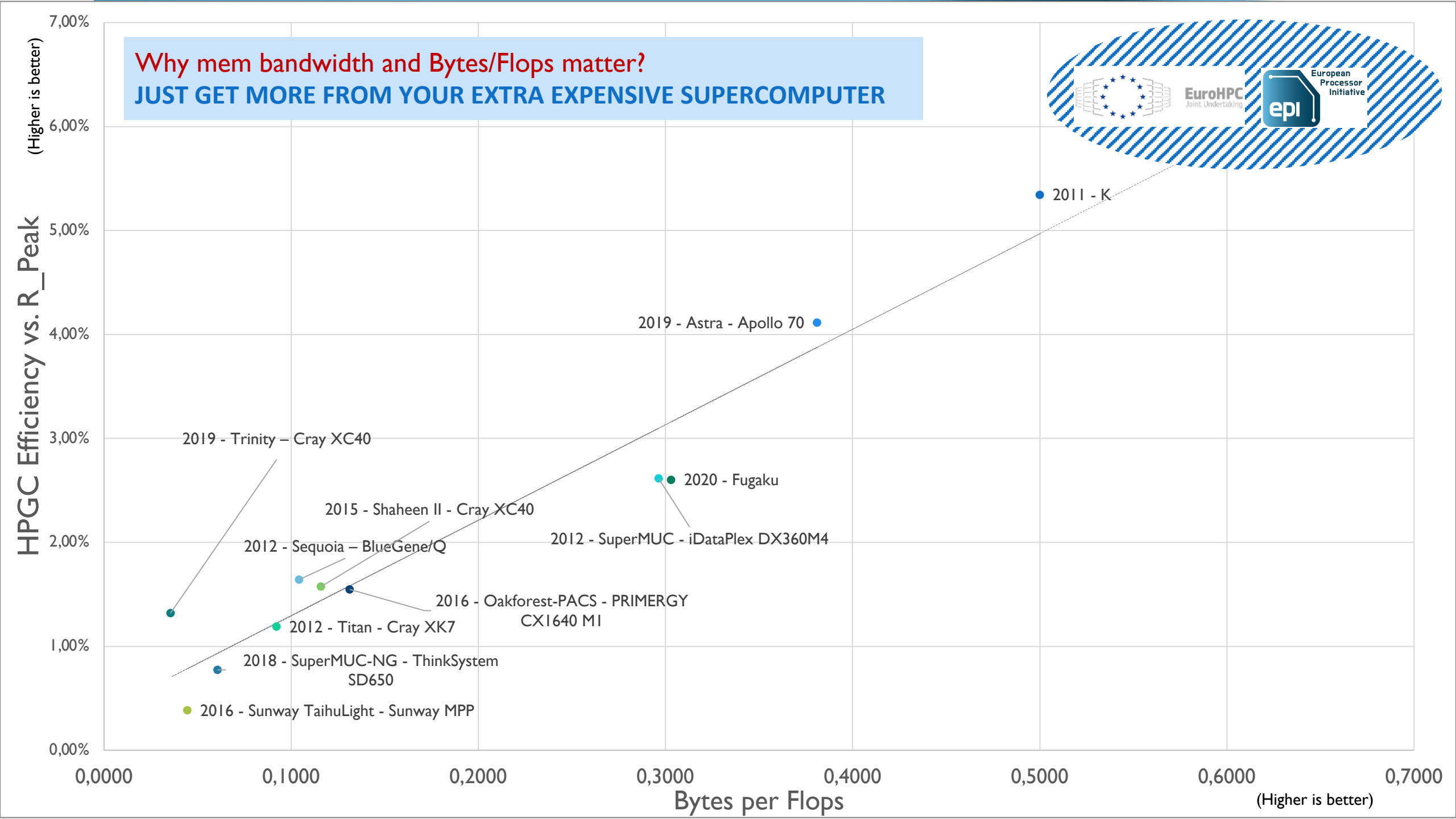
- World class manufacturing process (7nm or better)
- Need ~~best~~ excellent FP64 performances. But no need to try to compete with specialized devices like GPUs
- Need extreme flexibility and performances on external links
  - HBM 2e / 3
  - *and* DDR 5
  - *and* PCIe G5
  - *and* CXL
- Transparent integration in end-to-end dataflow : IoT ←→ Edge ←→ Datacenter ←→ Cloud
  - Easy to port / optimize
  - Opensource tools
  - Unified development tools

# CURRENT LANDSCAPE FOR HPC GPP

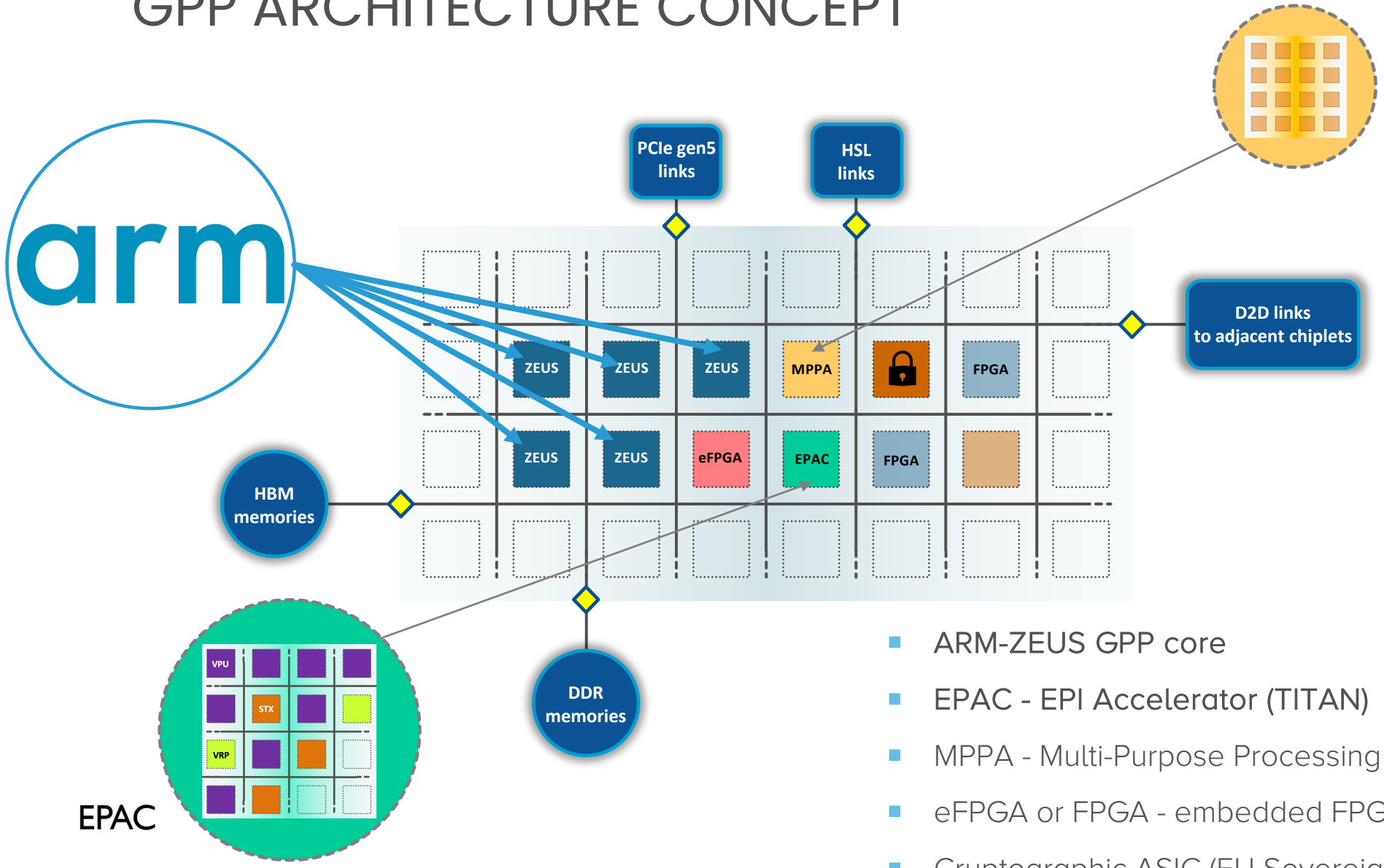


# Why mem bandwidth and Bytes/Flops matter?

## JUST GET MORE FROM YOUR EXTRA EXPENSIVE SUPERCOMPUTER



# GPP ARCHITECTURE CONCEPT



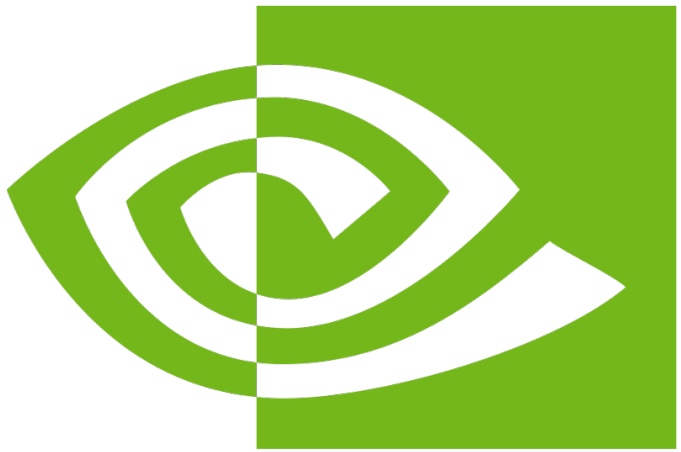

- ARM-ZEUS GPP core
- EPAC - EPI Accelerator (TITAN)
- MPPA - Multi-Purpose Processing Array
- eFPGA or FPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)

# PERSPECTIVES AND CHALLENGES

# EPI DELIVERS!

- The expertise for developing high-end and complex processing units in Europe, after decades of dis-investment
- A General Purpose Processor for HPC machines can be developed in EU by a EU Company (SiPearl)
- We'll be ready to move to the next step: engage on the development on a general purpose processor.

# CHALLENGES?

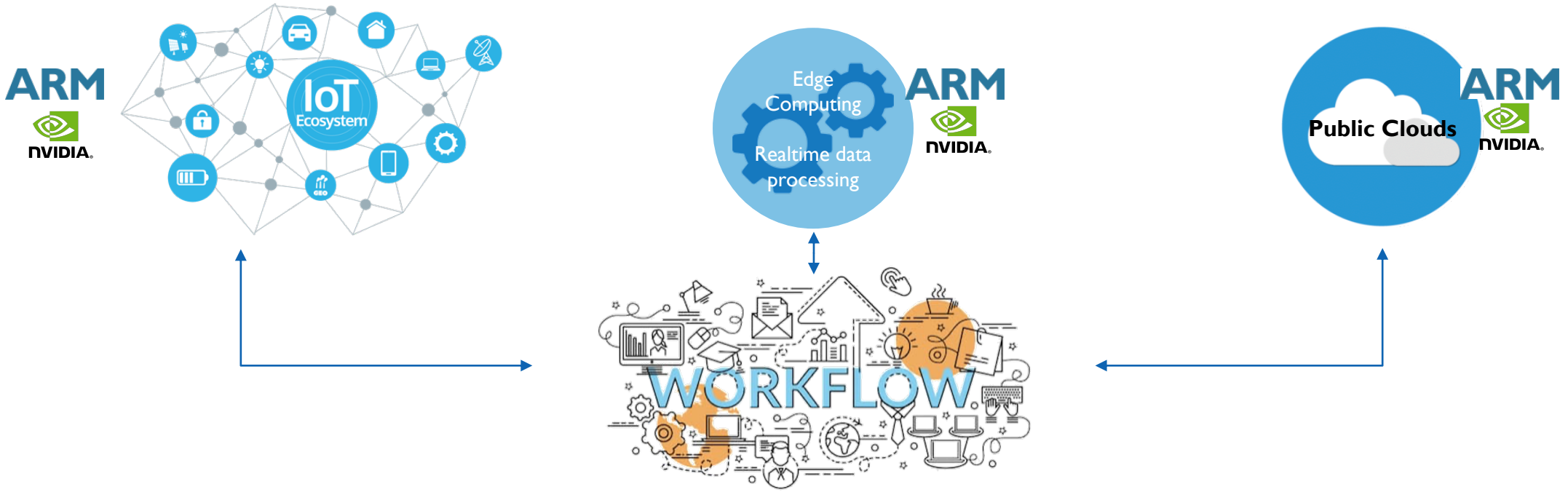


arm

NVIDIA®

# DATAFLOW

*UNIQUE ARM/NVIDIA COMBINATION FROM DATA CREATION UP TO DATACENTER AND CLOUD?*



# THANK YOU FOR YOUR ATTENTION


European Processor Initiative

- www.european-processor-initiative.eu
- @EuProcessor
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