Building flexible SoCs

Menta eFPGA technology for a changing world

SEMISRAEL

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www.menta-efpga.com

Corporate Presentation

Menta: The eFPGA IP leader
Multiple customers and years of experience

17 employees – Sophia Antipolis, France

Some Customers

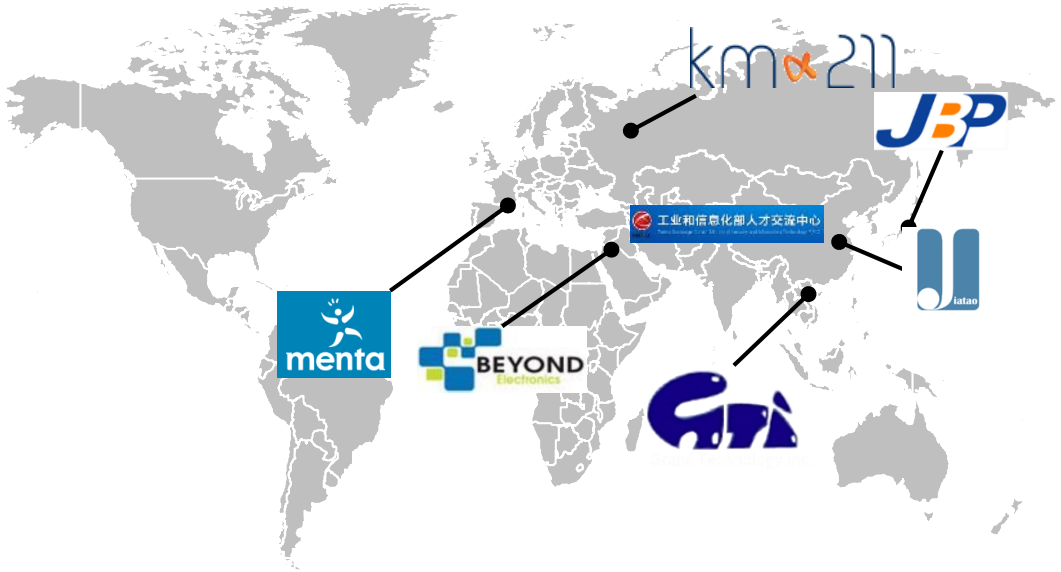
EUROPEAN DEFENCE AGENCY

ThalesAlenia Space

CHX

DGA

epi European Processor Initiative



HQ and R&D: Sophia-Antipolis, France

Sales representatives & Business Development in China, Taiwan, Israel, Japan, North America and Russia

12+ years of R&D

Patented third party standard cells IP

Supported silicon technology

Digital IP – we support **any** CMOS Foundry and Node

From 350nm to 6nm and less

GLOBALFOUNDRIES	STM	TSMC	XFAB
32 SOI*	130	28 HPC+	XH018***
22FDX**	65LP	12LP	
12LP*	28 FDSOI***	N6***	

* Qualified
** Menta is a FDX'celerator partner
*** Delivery in progress

Partners eco-system

eFPGA usage per market segment

	 Aerospace & Defense	 IoT/IIoT	 Automotive	 Networking & servers
Artificial intelligence	✓	✓	✓	✓
Security	✓	✓	✓	✓
Computing acceleration			✓	✓
Flexibility over lifetime	✓	✓	✓	✓
Reduction of number of variants		✓	✓	
Platform cost reduction		✓		

Technology enablers by market segment

Aerospace & Defence

- Trusted
- CDSP
- Rad-Hard by design
- National foundries
- Export regulations

IoT / IIoT

- Any foundry
- Low cost
- SW as an API
- Tiny eFPGA IPs
- Custom blocks
- CDSP
- Soft IP

Automotive

- DfT
- Qualified standard cells & foundries
- No SRAM bitcells
- Verification flow
- CDSP
- Soft IP

Networking / HPC

- Any foundry
- Custom blocks

eFPGA Example of Applications

eFPGA IPs for a changing world

“we do not know the future but we are ready to face it !”

Menta eFPGA IP is optimized for general purpose HPC and Automotive applications like:

- Image-processing using machine-learning (ML)
- Face recognition
- Data Prefetching and reconfigurable DMA Engine

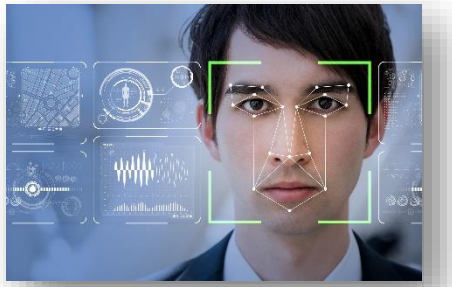
It is allowing post-production functions such like:

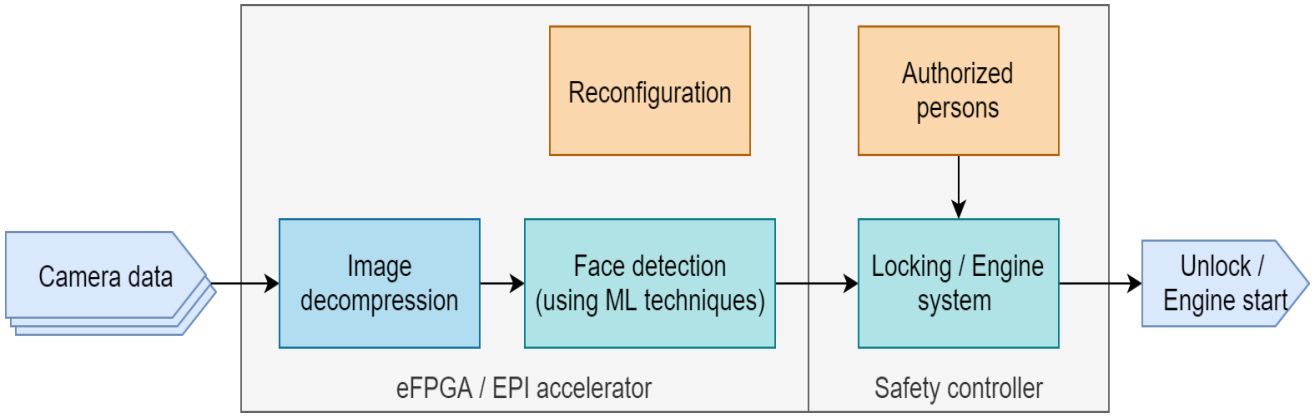
- Bug fixes
- Customer customization and proprietary elements

In addition, it is ensuring strengthen consideration of security aspects, like:

- Run-time reconfigurable crypto
- Post quantum public crypto key

Autonomous Driving: Image Processing & Face Recognition





Objectives:

- Unlock the car as soon as an authorized person approaches the car
- Start the engine if an eligible person takes place on the driver seat
- Example scenario: your child is able to unlock the car and take place inside; however, you want to prevent him or her from starting the engine

Menta Selected as Sole Provider of Embedded FPGAs for European Processor Initiative

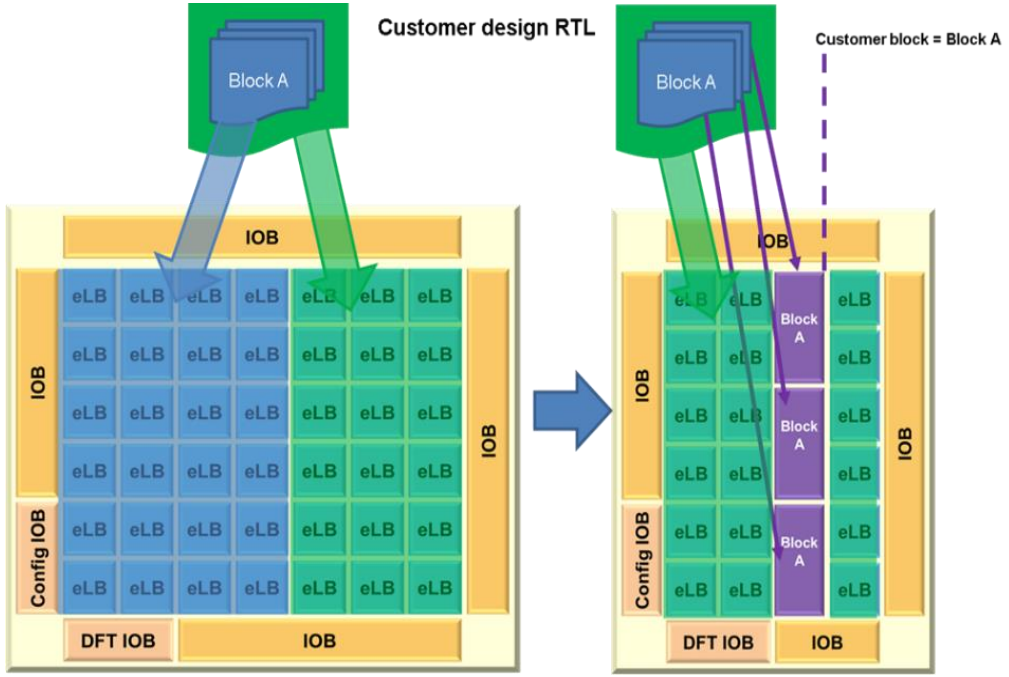
https://www.embedded-computing.com/processing/european-processor-initiative-designates-menta-provider-of-efpga-ip

"Our participation in this consortium really highlights the ability of our eFPGAs to be provided on any process technology, even the most advanced, such as 7nm, thanks to our third-party standard cells approach," says Vincent Markus, CEO of Menta.

Other example: Cryptographic Hardware Accelerator

- Implementation **Arithmetic IP-core** like into an eFPGA core
- eFPGA offer flexible cryptography algorithms during the product lifetime
- This is performed by establishing specific crypto custom blocks dedicated to the targeted security algorithms, using Menta's unique capability to integrate any arithmetic block.

Up to 20x performances increase expected – vs FPGA
Direct impact on the power consumption and cost of the system



Allow several variants of a security algorithms
Add features or customize crypto applications according to your needs

Rambus

https://d0b09575-47ef-4593-917a-aa075efa25aa.filesusr.com/ugd/f4a843_429fa11337cf4dcdb0eb71b95c6632b6.pdf

SECURE-IC

http://www.globenewswire.com/news-release/2020/02/26/1990734/0/en/Menta-and-Secure-IC-partner-to-optimize-embedded-cybersecurity.html

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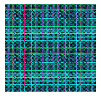
Products & Business Model

Products offering

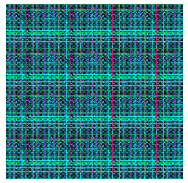
One scalable IP, multiple product offering

SMALL
[100 - 2K] LC

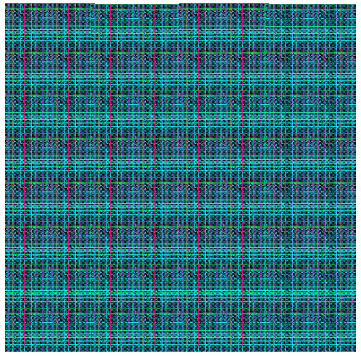
MEDIUM
]2K to 6K[LC



LARGE
]6K to 60K[LC



XLARGE
[60K to 200K] LC



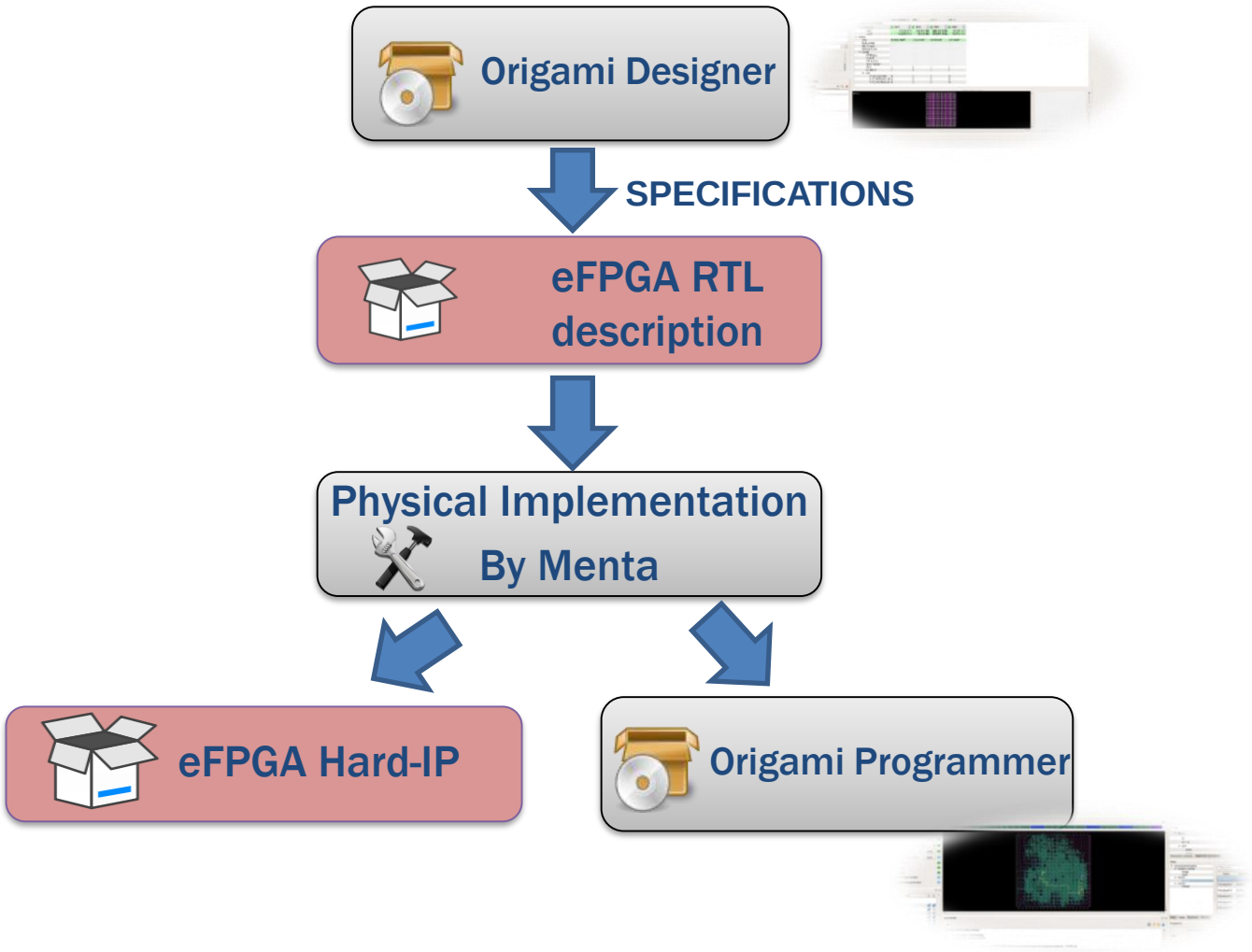
eFPGA IPs examples

	Small		Medium	Large		XLArge		Dedicated
Feature	**M5S0.5**	**M5S2**	**M5M5**	**M5L15**	**M5L40**	**M5XL65**	**M5XL130**	**?**
# LC	596	1 605	4 815	14 884	40 128	65 664	130 000	?
# Adaptive DSP	0	6	11	24	60	25	1000	?
# Specific arithmetic block	-	-	-	-	-	-	-	?
SRAM (kb)	0	0	1 442	0	1 966	2 425	5 252	?
# IOs	667	844	1 388	3 436	3 808	4 770	6 500	?

Design Adaptive eFPGA IP

1 LC = 1 LUT4 + FF

eFPGA IP delivery flow



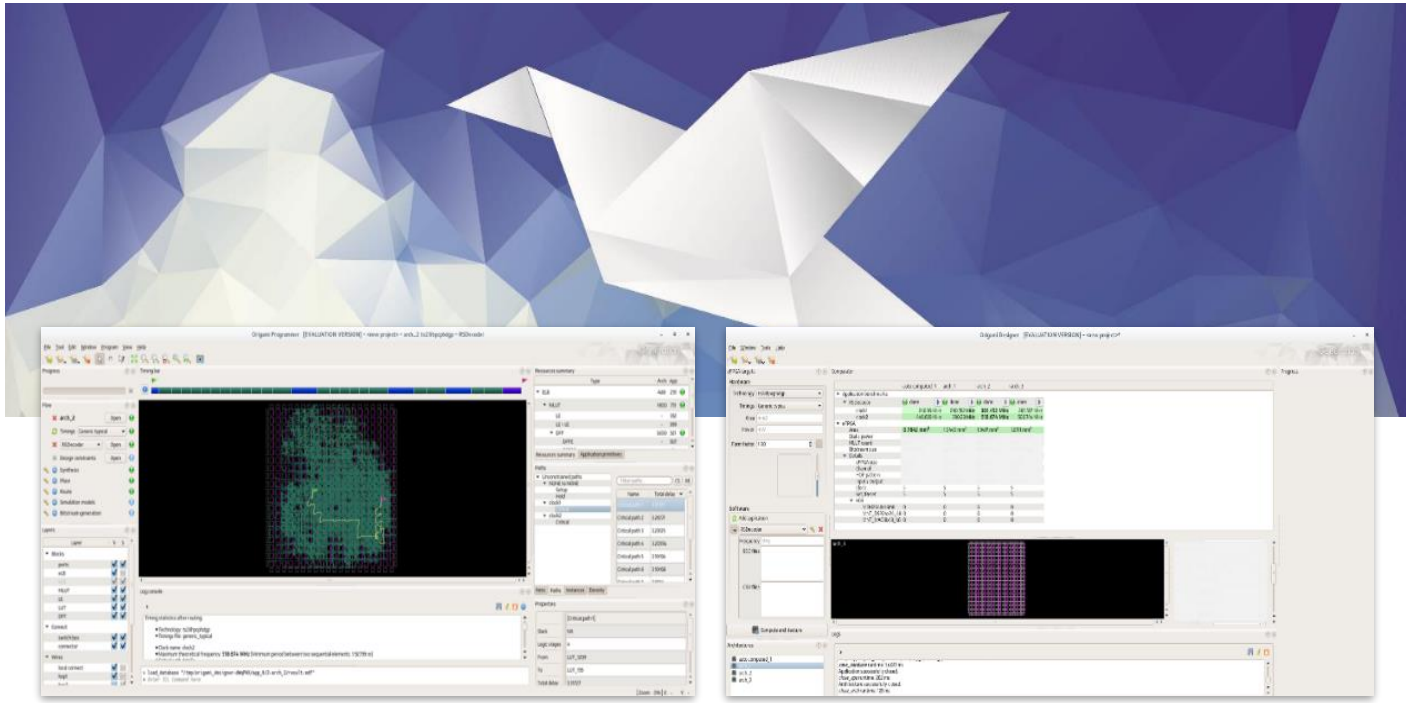
Fully flexible standard cells eFPGA

Origami Tool suite

The technology does not rely on 3rd party software tools which target “generic” FPGA architectures, thus delivering suboptimal results.

- Menta software is self contained
- It can be provided as an API to be integrated into customer SW framework
- It could be directly called by Mentor A Siemens Business **Graphics Catapult HLS** tool in a transparent way

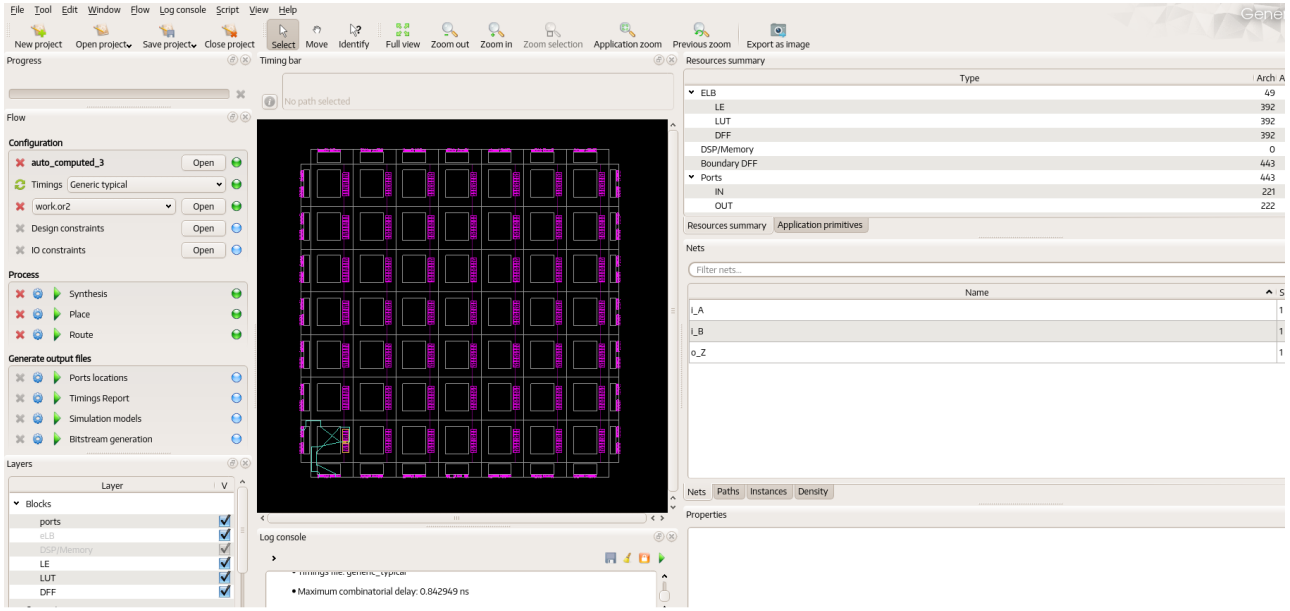
Unified Software Platform



Origami Programmer
From RTL to bitstream

Origami Designer
eFPGA IP definition

Origami Programmer – From RTL to bitstream



- Inputs:
  - Application RTL
    - IEEE Verilog / SystemVerilog / VHDL
  - Constraints: timing & IOs
- Outputs:
  - Bitstream
  - Simulation model
  - Timing reports
- GUI interface:
  - STA
  - Resources visualisation
  - Congestion maps
  - Move and reallocate resources
- From synthesis to bitstream generation: Menta development

Various distribution models possible

5th generation DESIGN ADAPTIVE eFPGA IP

- High density & performances
  - Patented MLUTs - LUT6 based
- Fully flexible
  - Number of eLBs
  - ASIC like eMBs: type, quantity & size
  - eCBs:
    - Adaptive CDSP blocks
    - Custom blocks
  - Number of IOs
- No specific interface
  - Data: AXI, AHB, proprietary buses, direct connections, etc.
  - Configuration: SPI, AXI/AHB, JTAG, etc.

- Various ASIC like power management options
- Standard scan chain. TC > 99.7%
- 100% 3rd party standard cells based
- Robust verification flow
- Bitstream storage: no SRAM bitcells. Using DFF

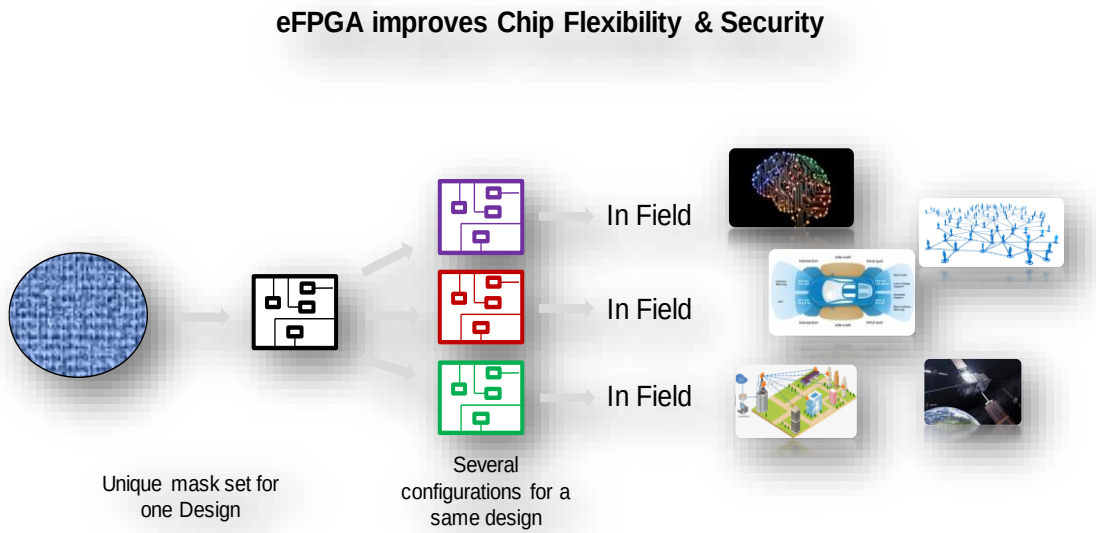
Conclusion

Decrease risk and ensure Design Flexibility with Menta embedded FPGA

More generic and customized SoCs
- Reconfigurable State Machines, complex and specific PMW functions, etc…
- Programmable and reconfigurable GPIO subsystem

Reduce power consumption and increase performance
- Offloads the Main Processor
- Plays as an Hardware Accelerator Companion

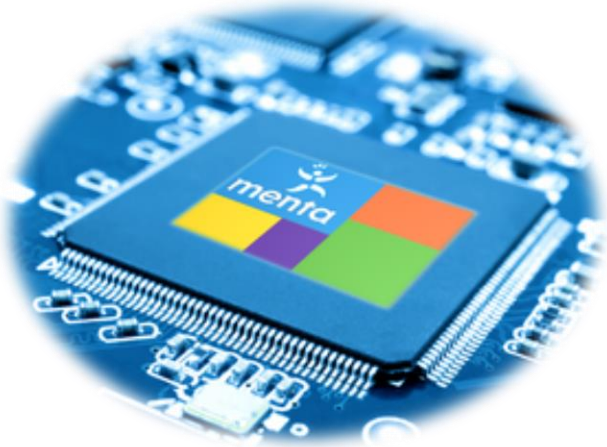
Post Tapeout features customization
- Multiple geographies – multiple crypto security algorithms
- End users “secret sauce”



Contacts

Imen Baili
Sales Application Engineer
imen.baili@menta-efpga.com

Yoan Dupret
Managing Director & VP of Business Development
yoan.dupret@menta-efpga.com



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