European Processor Initiative

SIPEARL
The Silicon Pearl

AHPC 2020

Klosterneuburg 21-02-2020

sipearl.com
European-processor-initiative.eu

P. Notton, Bio : EPI G.M. / SiPearl CEO

https://www.linkedin.com/in/pnotton/

- **Academic**
  - Engineer, **Supelec** (FR) (1993, Major in Signal Processing)
  - Executive MBA **Essec** (FR) & Mannheim (DE) (2008)

- **Business**
  - 1994-2000: HW, SW, Design, Integration for Digital TV - **Thomson**, **Canal+** - *France, USA*
  - 2000-2005: Support, Marketing- **LSI Logic**, now Avago – **Zarlink Semi**., now Intel. *France, UK*
  - 2006-2014: ***VP Marketing, Associate***, SetTopBox and TV, **Mstar Semi.** (now Mediatek). *UK, Taiwan*. From Startup to IPO and M&A with Mediatek of US$4B
    - #1 WW on TV (>200Mu per year). #3 WW on STB. 1st Secure chips in Asia.
  - 2014-2016: **ST Micro**, ***Group VP and GM Consumer Products Division*** (2400pers, WW P&L).
    - STB (Audio/Video/CPU/GPU/Security/Heavy SW and ecosystem)
    - Consumer Asics
    - 150mm2 Docis3.1 (28FD) / 90mm2 UHD STB (28FD) / 40mm2 HD STB (28FD)

Directly involved or in charge of more than 1 Billion chips with an $4-$20 ASP

Left an Exec position in ST to drive the next big Adventure in Europe and lead the future European Intel

Semiconductor industry background

Market Size	Around $400B and growing
Selected Numbers	Intel : $70B in sales TSMC (#1 foundry) : Market cap = US$B260 ASML (Tools for foundries) : Market cap = US$70B (google “Trump ASML Huawei”)

2019F Top 15 Semiconductor Sales Leaders ($M, Including Foundries)

2019F Rank	2018 Rank	Company	Headquarters	2018 Total IC	2018 Total O-S-D	2018 Total Semi	2019F Total IC	2019F Total O-S-D	2019F Total Semi	2019/2018 % Change
1	2	Intel	U.S.	69,880	0	69,880	69,832	0	69,832	0%
2	1	Samsung	South Korea	75,698	2,843	78,541	51,750	3,860	55,610	-29%
3	4	TSMC (1)	Taiwan	34,208	0	34,208	34,503	0	34,503	1%
4	3	SK Hynix	South Korea	36,200	567	36,767	22,291	595	22,886	-38%
5	5	Micron	U.S.	30,930	0	30,930	19,960	0	19,960	-35%
6	6	Broadcom Inc. (2)	U.S.	16,454	1,735	18,189	15,917	1,789	17,706	-3%
7	7	Qualcomm (2)	U.S.	16,385	0	16,385	14,300	0	14,300	-13%
8	8	TI	U.S.	13,908	946	14,854	12,705	842	13,547	-9%
9	9	Toshiba/Kioxia (3)	Japan	12,293	1,508	13,801	9,839	1,437	11,276	-18%
10	10	Nvidia (2)	U.S.	11,951	0	11,951	10,514	0	10,514	-12%
11	15	Sony	Japan	627	7,088	7,715	878	8,674	9,552	24%
12	11	ST	Europe	6,628	2,991	9,619	7,241	2,215	9,456	-2%
13	13	Infineon	Europe	5,465	3,745	9,210	5,366	3,580	8,946	-3%
14	12	NXP	Europe	8,429	978	9,407	7,969	888	8,857	-6%
15	14	MediaTek (2)	Taiwan	7,891	0	7,891	7,948	0	7,948	1%
—	—	Top-15 Total		346,947	22,401	369,348	291,013	23,880	314,893	-15%

(1) Foundry (2) Fabless (3) Formerly Toshiba Memory

Source: Company reports, IC Insights' *Strategic Reviews* database

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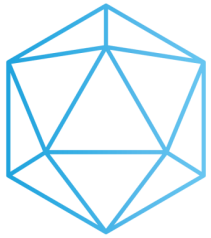
EPI UPDATE

AHPC2020



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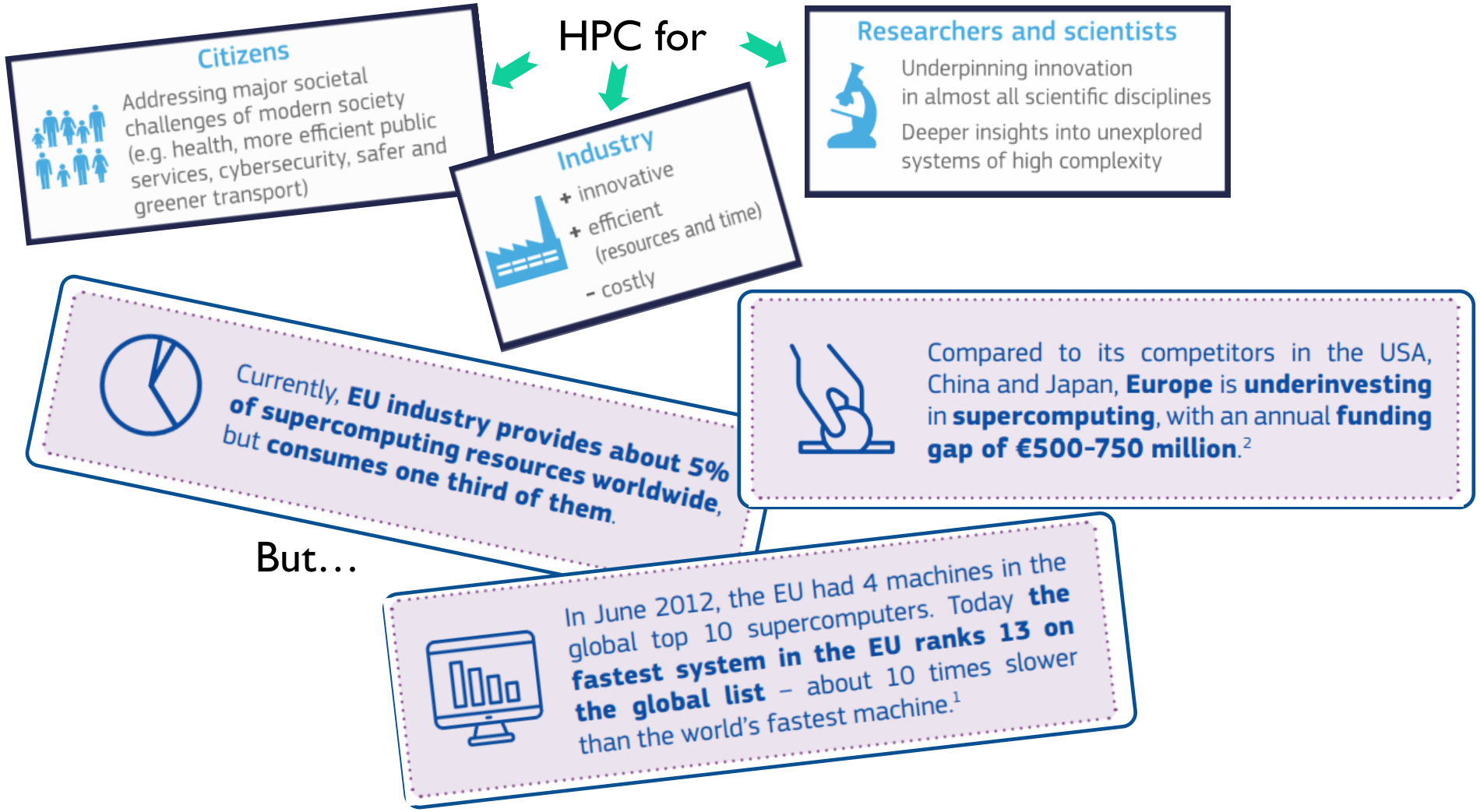
PHILIPPE NOTTON / GM EPI – SIPEARL CEO

Trump administration pressed Dutch hard to cancel China chip-equipment sale: sources

entities to a United States blacklist on Friday,
China's access to American technology and stoking already high tensions before a planned meeting between President Trump and President Xi Jinping of China in Japan next week.

Smart City-Datenplattformen



Source: https://ec.europa.eu/newsroom/dae/document.cfm?doc_id=54437

EUROPEAN PROCESSOR INITIATIVE

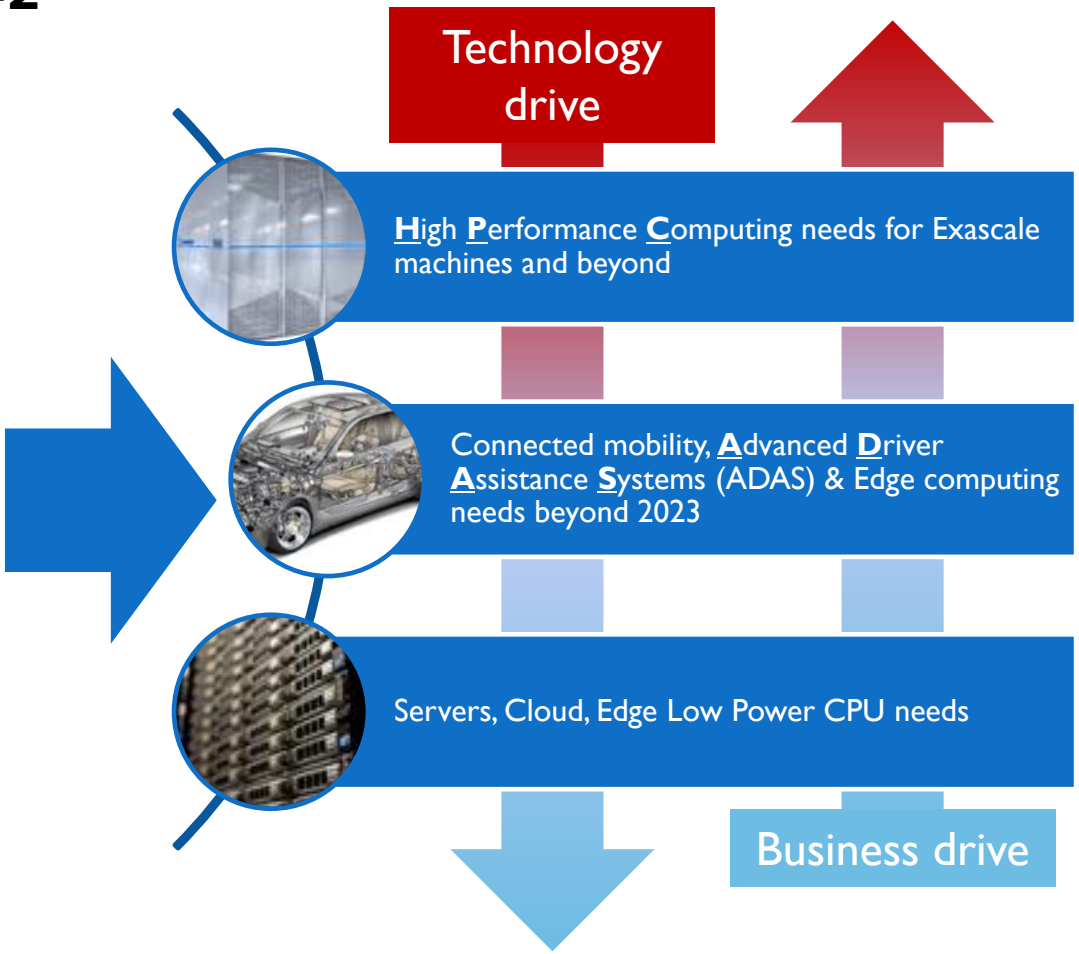
- Started officially in dec 2018
- 80M€ of EU H2020 budget for phase 1:
- Moving toward:
  - High Performance General Purpose Processor for HPC, ARM based
  - High-performance EPI-made accelerator
  - Computing platform for edge and autonomous cars

EC expectations from ICT-42 & EPI value proposal

EPI expected impacts (as per EC request)

- Get a world class processor for the Exascale machines supplied by EuroHPC in 2023
- Develop a sustainable economic model

EPI is an H2020 program but with industrial mindset & product delivery oriented



THE EPI STORY, PART 1

- Having 10 countries, 27 partners working together to win such a large EU call ?

THE EPI STORY, PART 2

- Sharing all together a common technical vision in terms of architecture and product ?

THE EPI STORY, PART 3

- Giving an industrial vision and industrial hand to EPI

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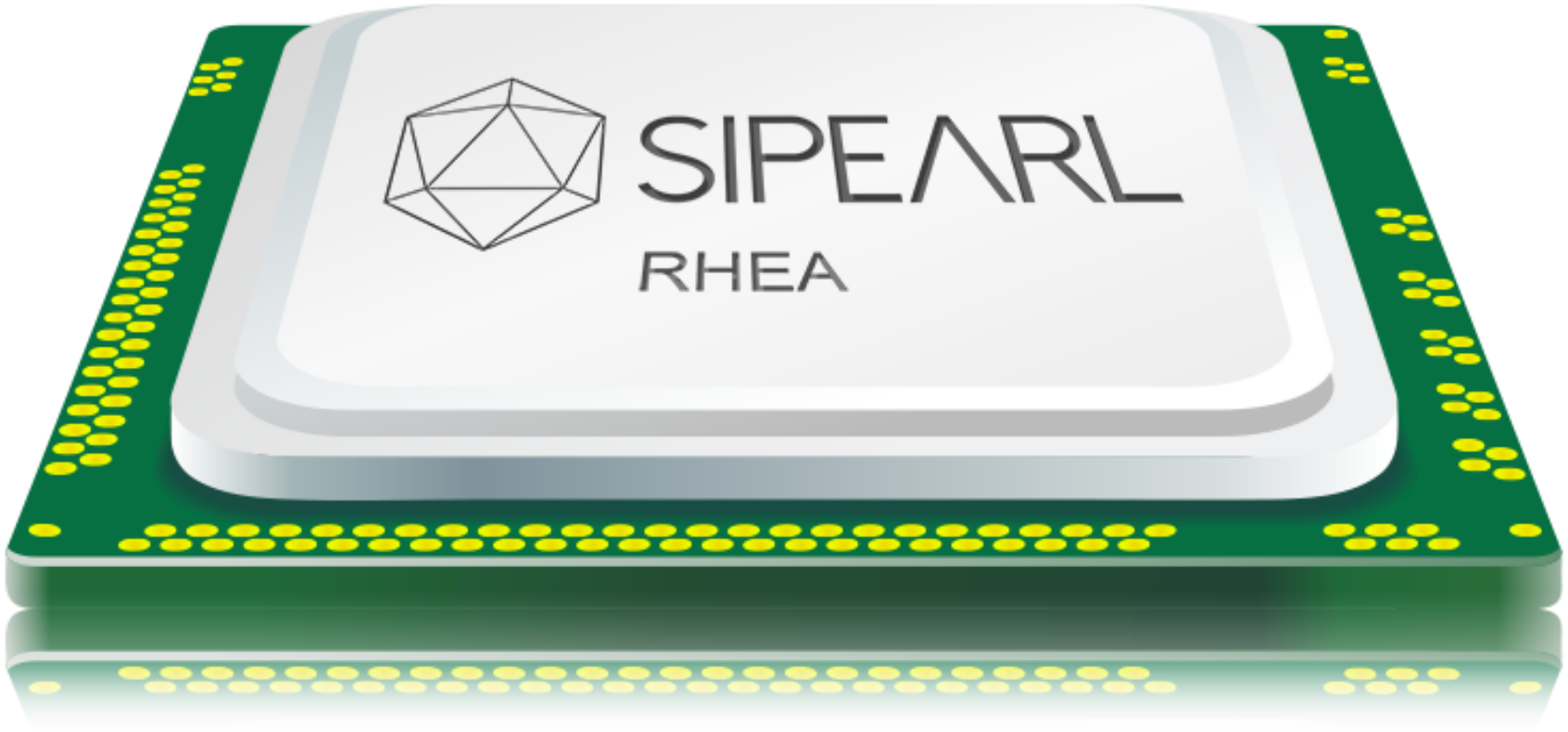
THE EPI STORY, PART 4

- Having access to ARM top notch technology for reasonable time to market

SO NOW LET'S HAVE THIS EU SOLUTION READY !



WHAT IS BEHIND EPI AND WHERE ARE WE GOING ?

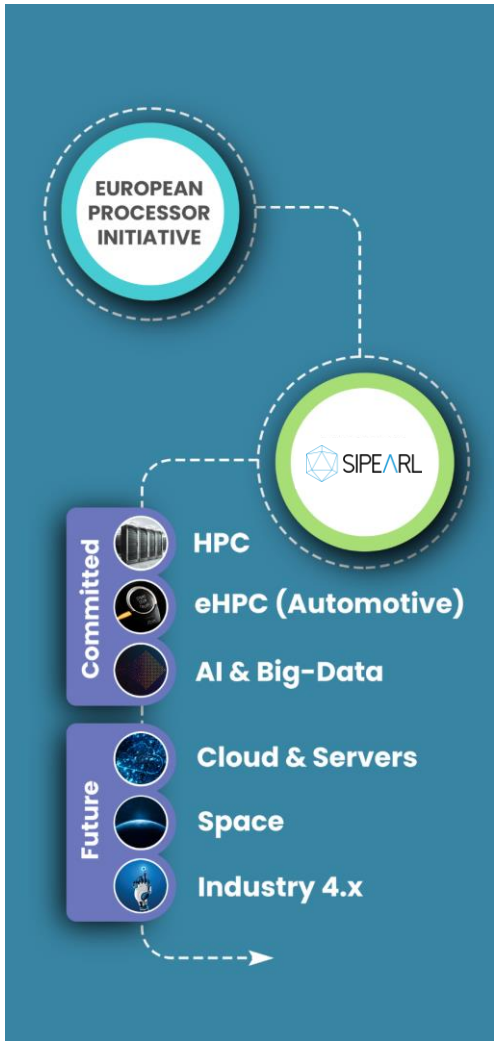
27 EPI PARTNERS

SIPEARL = EPI FABLESS COMPANY

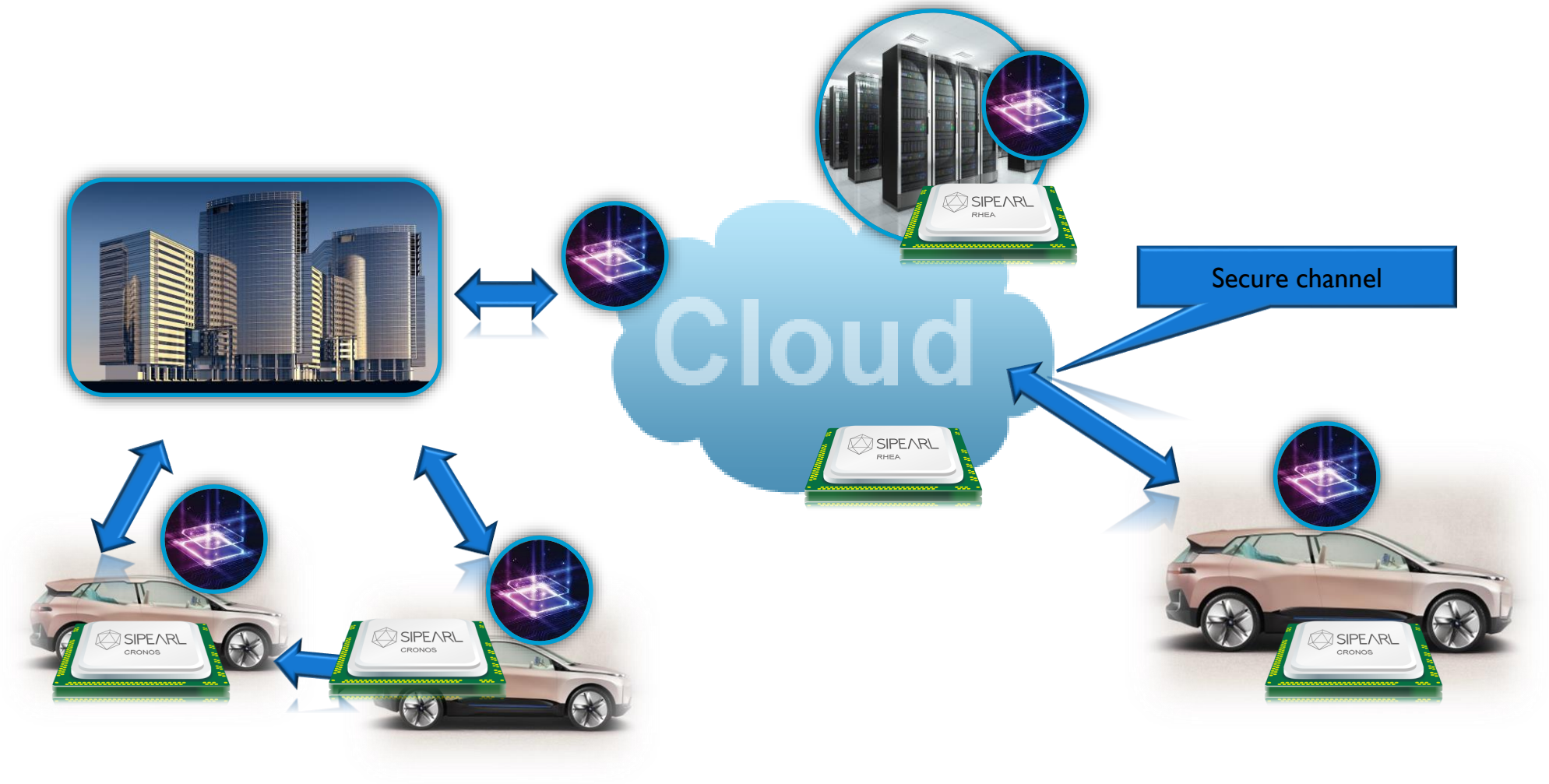
- Semiconductors company are:
  - ‘integrated’ or own their own fabs : such as Intel, Samsung, ST
  - ‘Fabless’ and oursource their production (to TSMC, Samsung, or others) : such as Amd, Qualcomm, NVIDIA

- Fabless company
  - licence of IPs from the partners
  - develop its own IPs around it
  - licence the missing components from the market (such as ARM IP’s)
  - Incorporated now as SIPEARL

  - integrate, market, support & sales the chip
  - generate revenue from both the HPC, IA, server and eHPC markets
  - work and drives the next generations
  - The industrial ‘hand’ of EPI



ONE OF THE LONG TERM VISION: FAR BEYOND HPC: END2END SECURITY - FROM THE AUTOMOTIVE SYSTEM TO THE CLOUD



WHAT ARE THE CHALLENGES ? (BEYOND THE INITIAL « MISSION IMPOSSIBLE » ITEMS)

What is “really” good

Semiconductor Companies value	Intel bought MobileEye for $15B (2017) Intel bought Habana Labs for $2B (2019) Nvidia bought Mellanox for $6.9B (2019)
In Semiconductor engineering	Microprocessor is THE big cookie in terms of engineering Very complex development Top Notch technology … and Europe is out of it , for finished goods (at least up to now)
Part of our Key Words	CyberSecurity, BigData, AI, **Sovereignty**, DeepLearning, Quantum, Adas, Edge
Our supporters	EU (>1B€) budget for EuroHPC Actual geo-politics in favour of data protection and sovereignty

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What is “tough”

Combined “Research” and “Industrial project”	While Research has…. … tons of idea to rebuild the world … working in a different time dimension Semiconductor industry is… … over expensive and not doing anything for free … not really “startup” centric in Europe … seen as technology for “grand’pa” and dirty (i.e, let’s do SW and Web SW)
The fun of “deep-tech” like semiconductor	You **burn** cash for years Product **may** work Product **may** have the expected performance Product **may** have a customer
The fun of “semiconductor investment”	Investors are running away… in Europe But in USA over the past years, $4B invested for AI hardware…. (not to mention SW budget) China invested $150B to develop a real semiconductor industry
European market	Is wide open to non-European competitors (example of solar panels)
The budget	EPI EU H2020 budget has to be completed with private budget (>100M€+)

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But it happens….

Q2-2020	Closure of 1st financial round
Q1-2020	Exec team is joining SiPearl Major announcement with Arm
Sept-2019	SiPearl becomes EPI industrial hand 6,2M€ raised
June-2019	SiPearl is incorporated
Dec-2018 **EPI kick off** **80M€ allocation**	EPI kick-off 80M€ H2020 allocations IP / Architecture initiated
2017-2018	European Processor Initiative consortium setup

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HPC wire

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SiPearl Begins Development of Europ Processor with €6.2M

February 12, 2020

MAISONS-LAFFITTE, France, Feb. 12, 2020 – SiPearl free) company that will design, market and distribute the low-power microprocessor to secure Europe's technolog independence on the strategic markets for high perform artificial intelligence and connected mobility.

SiPearl was created in June 2019 by Philippe Notton to project of the 27 members of the European Processor In consortium selected by the European Union to support t European microprocessor. Based on a roadmap that is the European Union's goals, the company is targeting a 2022 for its first range of microprocessors.

In the space of a few months, its CEO and founder has built the solid foundations that will support SiPearl's development:

- A powerful ecosystem bringing together its 26 partners within the European Processc
- A leadership team with complementary areas of exper records,
- Best-in-class industrial and technological suppliers se
- €6.2m of European subsidies to launch its developme followed by a major round of fundraising.

The European Processor Initiative consortium meml ecosystem of 26 partners for SiPearl

proprietary technologies, working closely with

- Driving high performance computing's transition to exascale,

EN24

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Tech News

SiPearl: Company founded for European CPU with ARM and RISC-V technology

January 21, 2020 22 0

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Liquid Cooling Trends in HPC

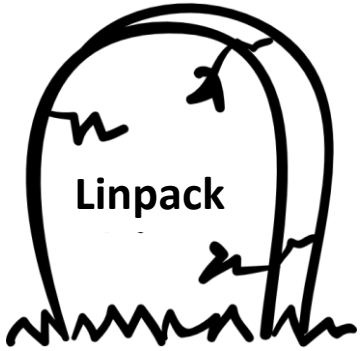
BUT, WHAT'S THE TECH' AND HPC STRATEGY BEHIND EPI ?

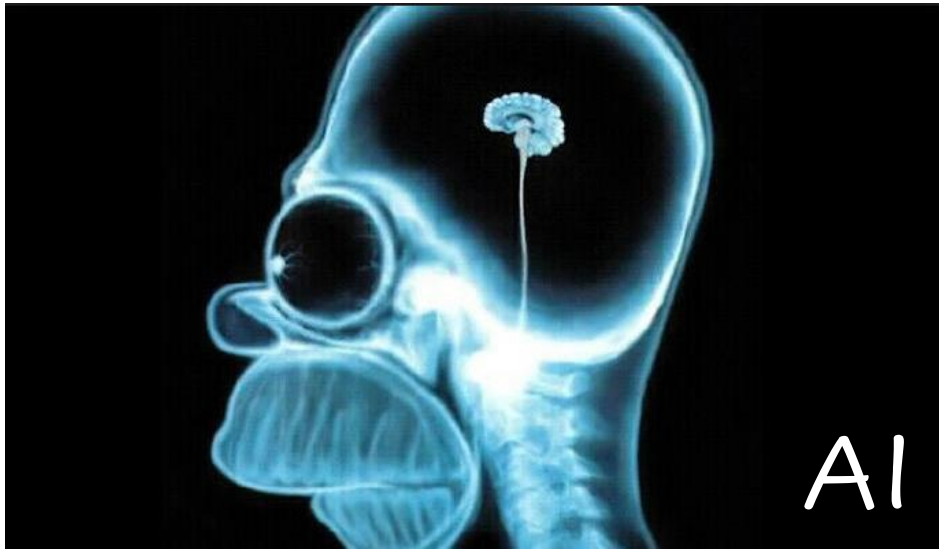

Cambrian explosion
Achieving performance through specialization
Courtesy Steve Scott
Cray CTO

TOP10 OVER THE LAST 10 YEARS

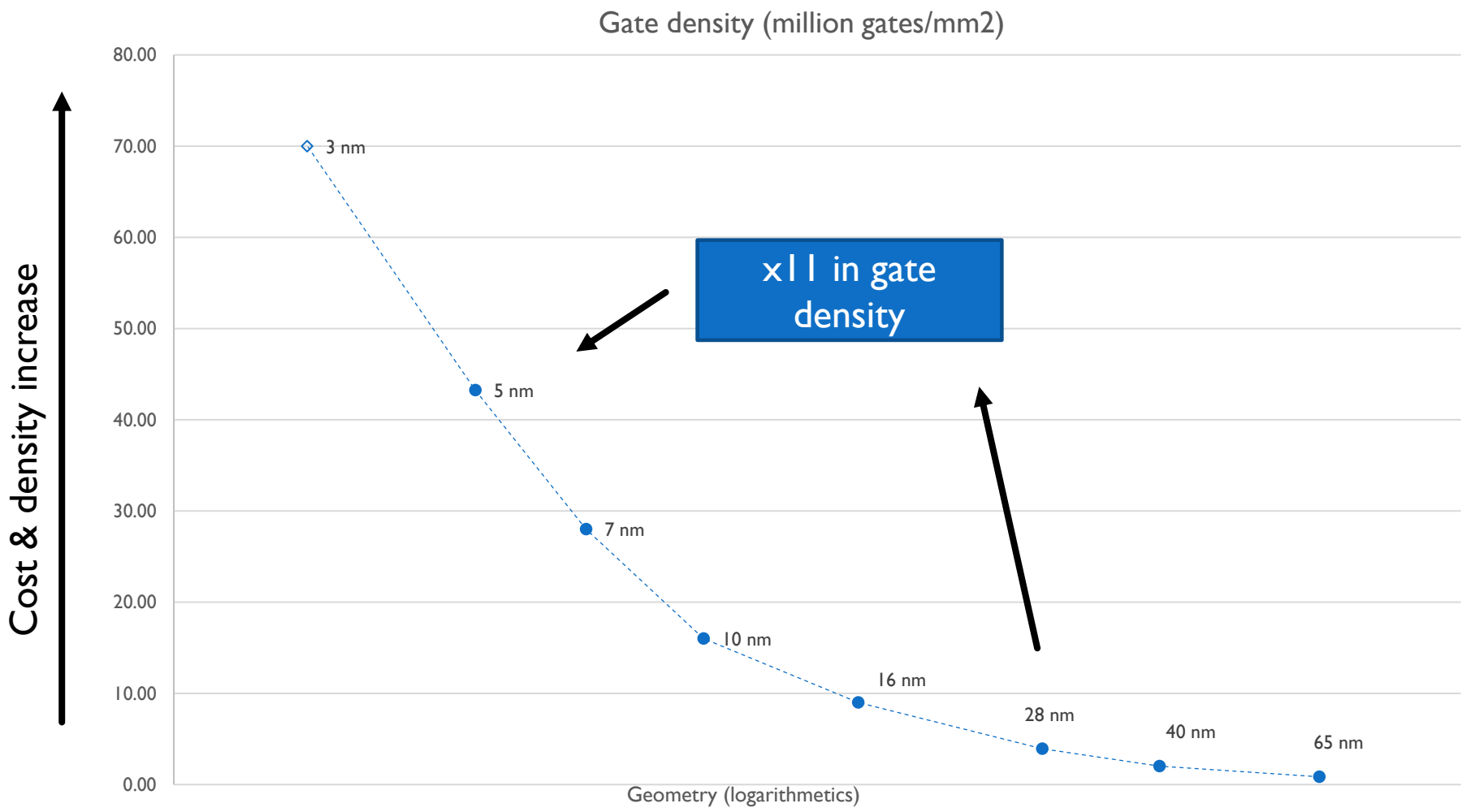
	2009 – Nov.	2014 – Nov.	2019 – Nov.	*(Post)* Exascale
CPU **only**	9	5	2	0
CPU + ACC.	1	5	8	10

WHY? SOME OBVIOUS REASONS…

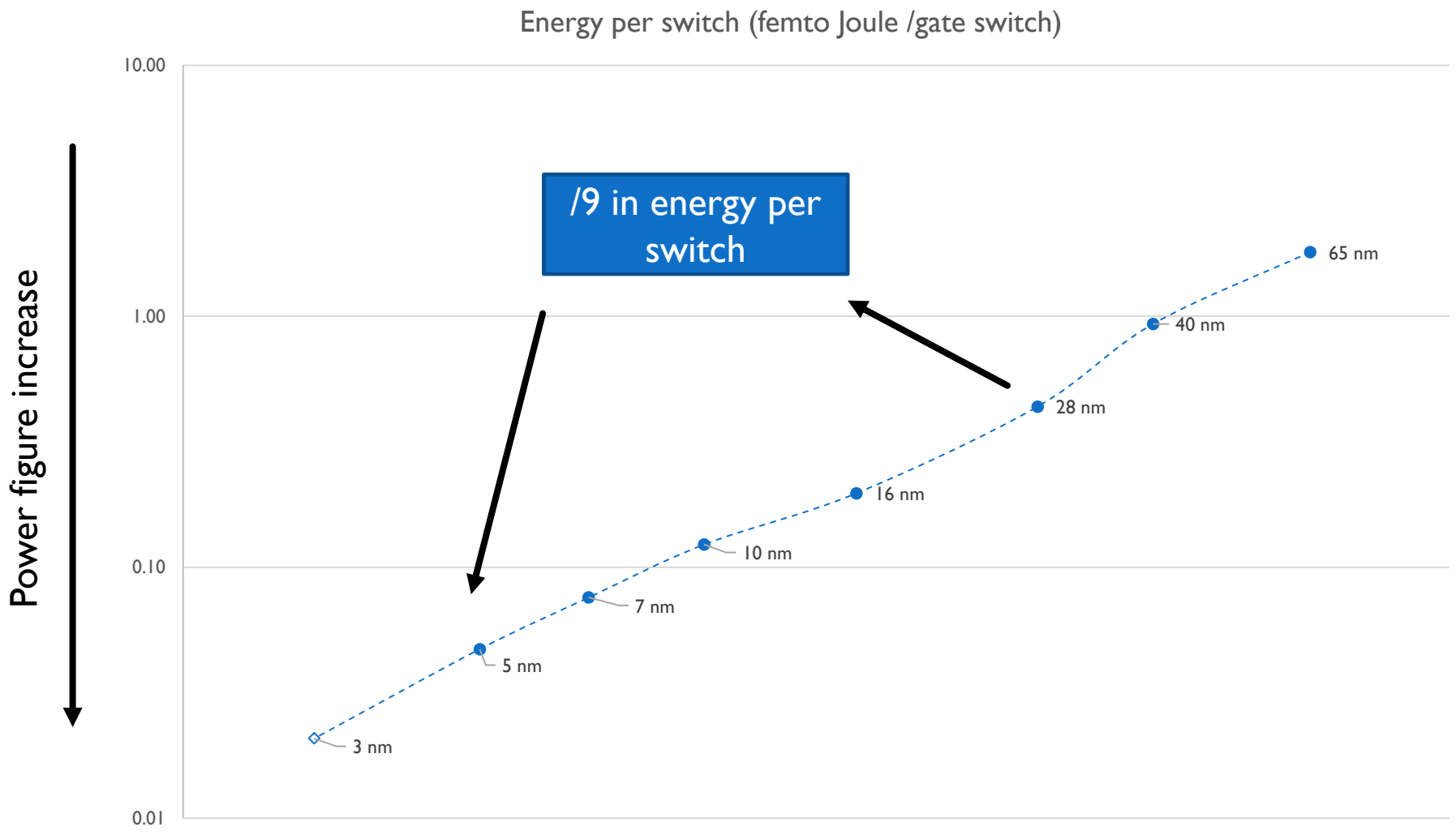




END OF MOORE' LAW 1/



END OF MOORE' LAW 2/



END OF MOORE' LAW & NEEDS FOR DATA PROCESSING 3/

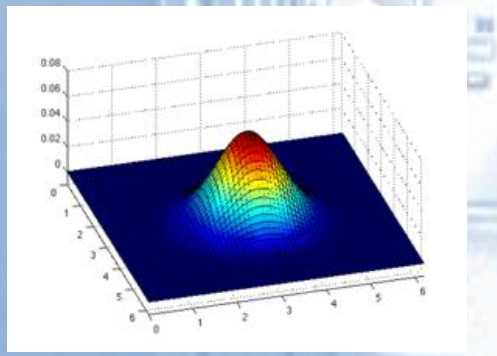
Basic Needs	More Computing Power: → Higher density (more gates) Less power consumption → Newer silicon process per gate
Impact 1	Development cost higher and higher to cover density need and power consumption
Impact 2	Find more money, engineers and development time
Impact 3	Or be creative and move to 2.5D design ?

HPC BEFORE ARTIFICIAL INTELLIGENCE

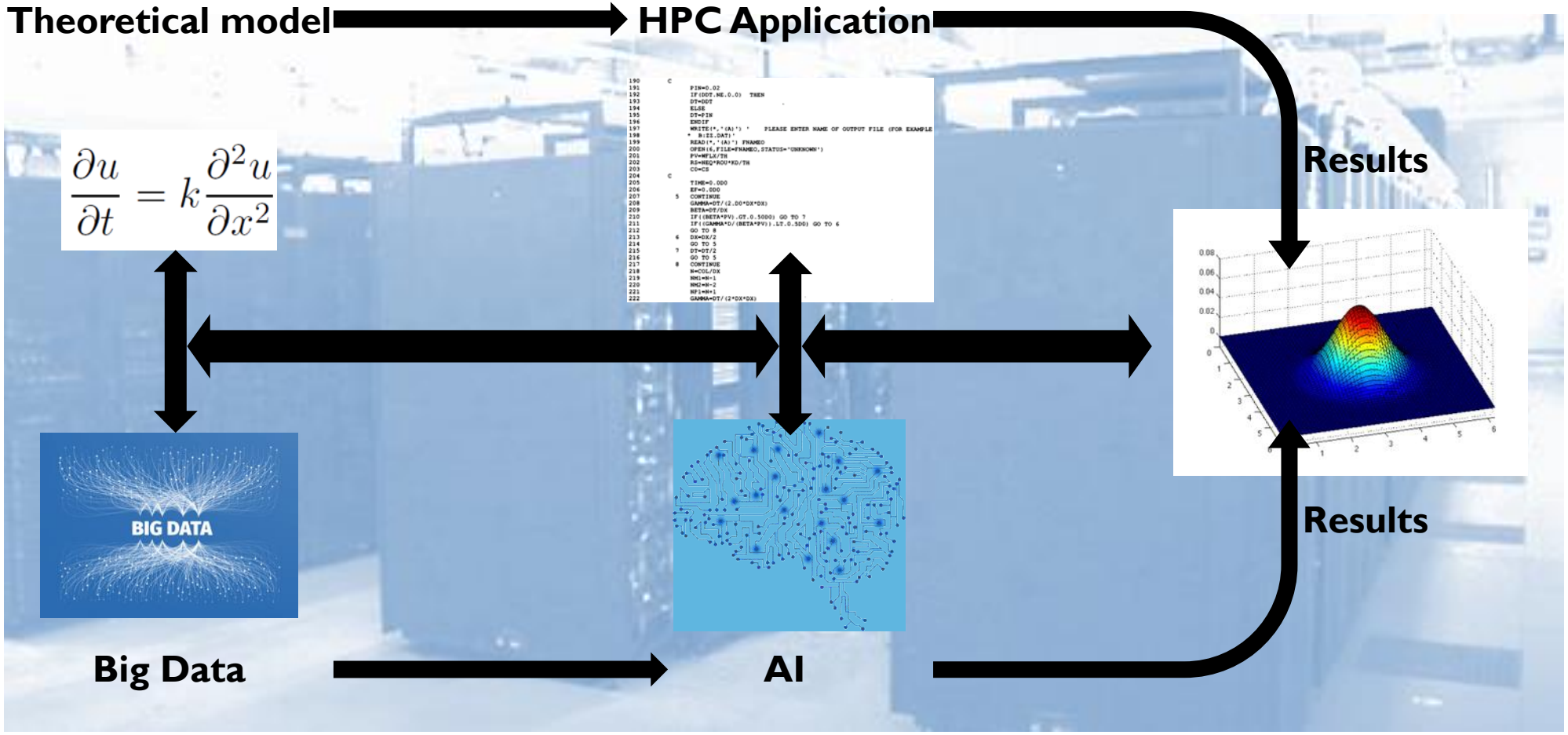
Theoretical model → **HPC Application** → **Results**

$$\frac{\partial u}{\partial t} = k \frac{\partial^2 u}{\partial x^2}$$

```
      C
            PIN=0.02
            IF(DDT.NE.0.0)  THEN
            DT=DDT
            ELSE
            DT=PIN
            ENDIF
            WRITE(*,'(A)') '    PLEASE ENTER NAME OF OUTPUT FILE (FOR EXAMPLE
           *  B:IS.DAT)'
            READ(*,'(A)') FNAMEO
            OPEN(6,FILE=FNAMEO,STATUS='UNKNOWN')
            PV=WFLX/TH
            RS=NEQ*ROU*KD/TH
            CO=CS
      C
            TIME=0.0D0
            EF=0.0D0
        5   CONTINUE
            GAMMA=DT/(2.D0*DX*DX)
            BETA=DT/DX
            IF((BETA*PV).GT.0.5DD0) GO TO 7
            IF((GAMMA*D/(BETA*PV)).LT.0.5DD) GO TO 6
            GO TO 8
        6   DX=DX/2
            GO TO 5
        7   DT=DT/2
            GO TO 5
        8   CONTINUE
            N=COL/DX
            NM1=N-1
            NM2=N-2
            NP1=N+1
            GAMMA=DT/(2*DX*DX)
```



HPC WITH ARTIFICIAL INTELLIGENCE



HPC & AI AT EXASCALE: IT'S ALL ABOUT WORKFLOWS (1/2)

arm

Edge Computing

Realtime data processing

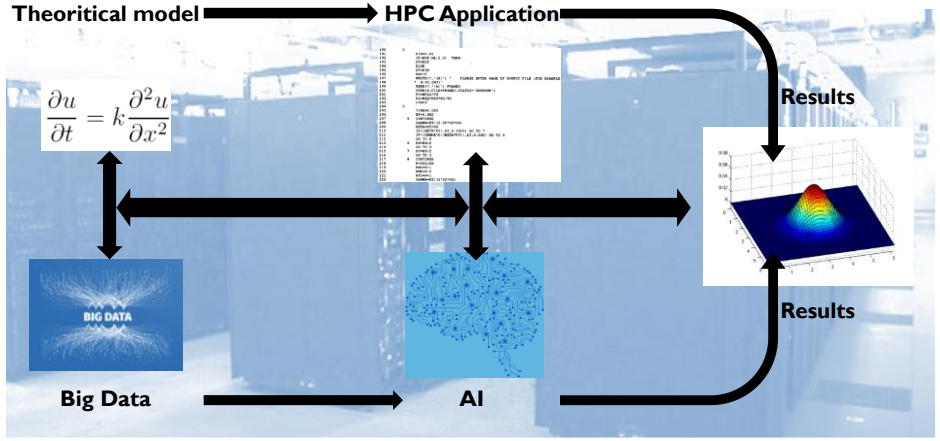
X86 arm

Public Clouds

X86 arm

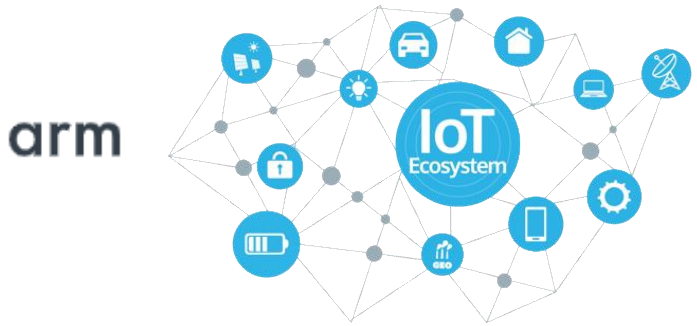
SUMMIT

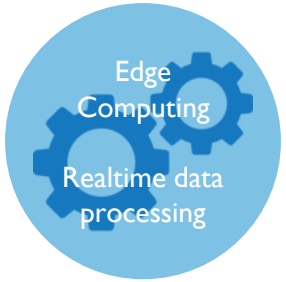
sunway taihulight



FUGAKU

HPC & AI AT EXASCALE: IT'S ALL ABOUT WORKFLOWS (2/2)



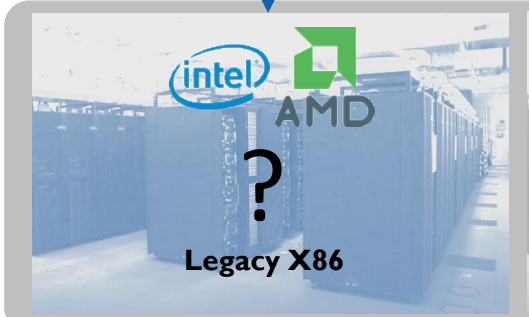


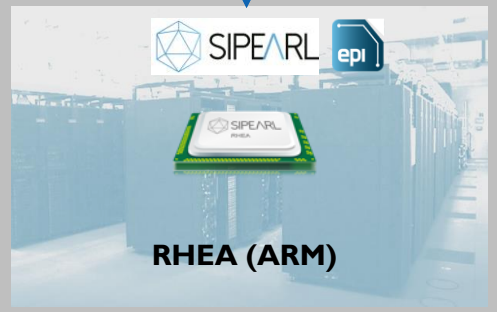
arm

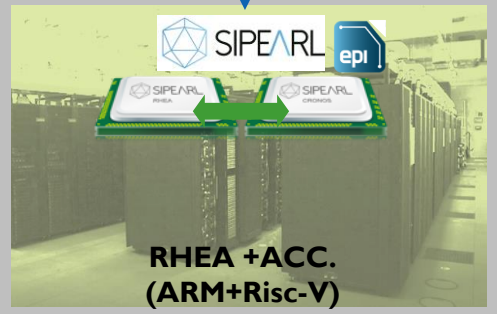
arm

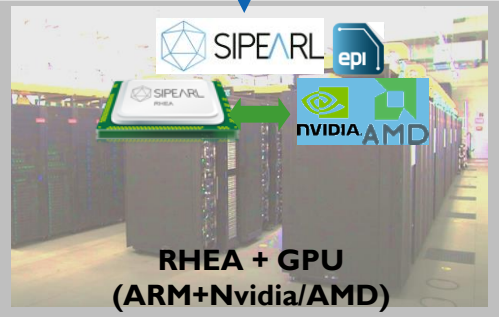
European approach

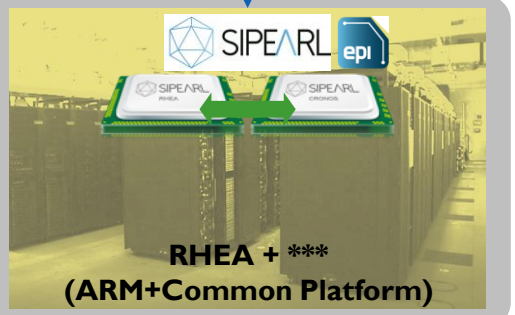
- ✓ EU Architecture
- ✓ EU HW
- ✓ EU SW
- ✓ Handle all complexity the others don't know how to











HPC & AI AT EXASCALE: IT'S ALL ABOUT WORKFLOWS (2/2)

arm

Edge Computing

Realtime data processing

arm

Public Clouds

arm

European approach

- ✓ EU Architecture
- ✓ EU HW
- ✓ EU SW
- ✓ Handle all complexity the others don't know how to

Compiler

CPU ARM Legacy X86 — ACC.A

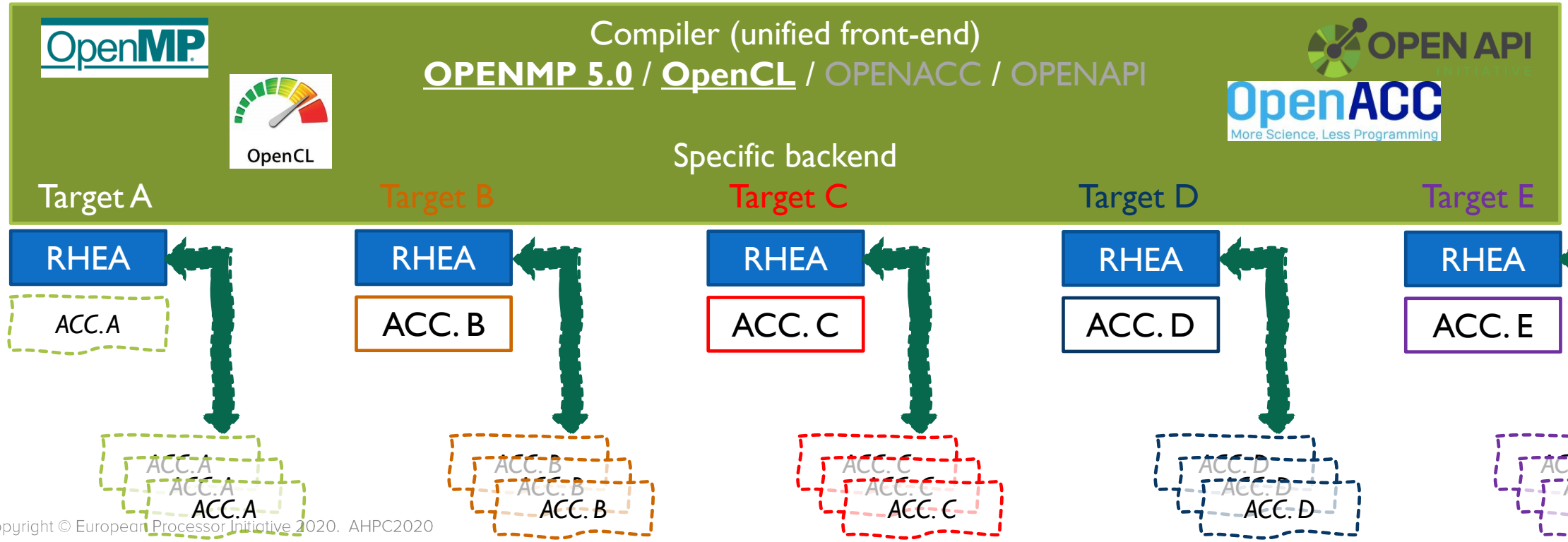
CPU ARM RHEA (ARM) — ACC. B

CPU ARM RHEA +ACC — ACC. C

CPU ARM RHEA + GPU — ACC. D

CPU ARM RHEA + (ARM) — ACC. E

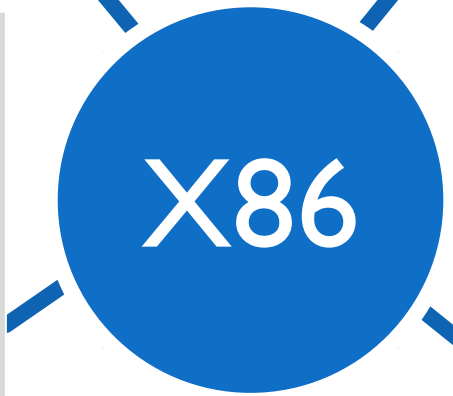
THE DEVELOPER / USER STANDPOINT



EVIDENCE: INTEL OVERALL STRATEGY IN HPC, CLOUD, EDGE

Intel own accelerator developments:
- GPU (Artic Sound)
- CSA

Accelerator companies acquired by Intel or with intel in their Capital, in the last years:
- Altera
- Habana
- Mobileye
- Untether AI* (Toronto, Ontario, Canada)
- SambaNova Systems* (Palo Alto, California, U.S.)
- Zhuhai EEasy Technology Co. Ltd.* (Zhuhai, China)
- …



CPU - Accelerator interface:
- CXL

User environment:
- Intel Compiler
- OneAPI

LESSONS LEARNED
PROFILE FOR EXASCALE SOLUTIONS

Main changes
- Holistic view of data from IoT to Supercomputers.
- Hybrid in-house / cloud
- Workflow everywhere

Modularity is a must have. One does not fit all

Several accelerators, typically one per module

Performance comes from accelerators

The CPU has to be well balanced
- peak performance is not important
- Agility (FP64 for HPC, BF16 for deep learning) is crucial
- Data transfer is crucial

➔ Cover day to day needs and for all compute not fitting well in ACC

Keep overall architecture simple
➔ one CPU to unify all accelerators

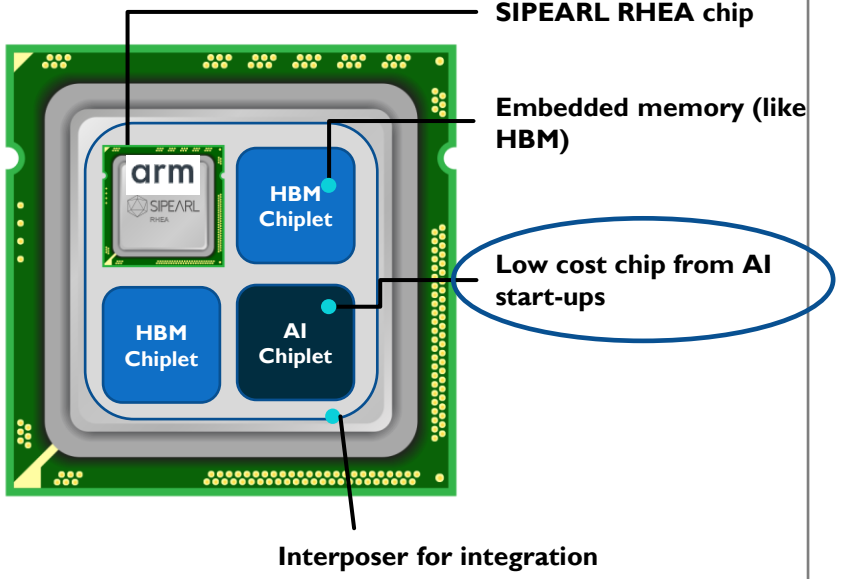
Keep end user life simple

- 1 CPU only
- LLVM + GCC + OPENMP 5.0
- Keep it open!

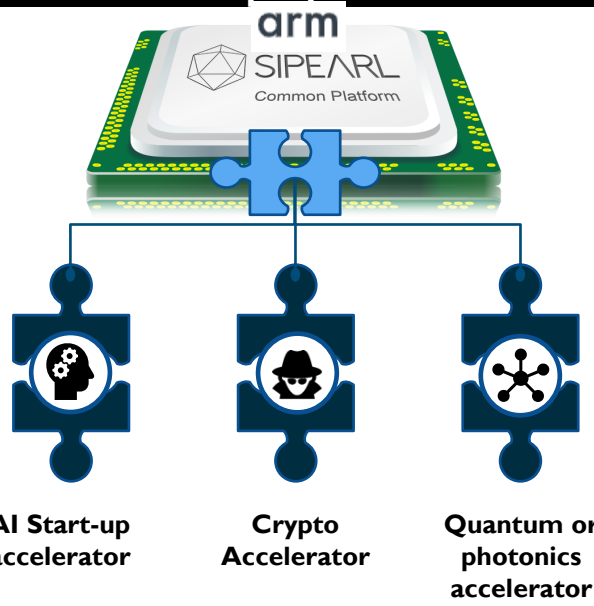
TECHNOLOGY & ROADMAP

COMMON PLATFORM VISION: FEDERATE ACCELERATORS

Interposer function



Value proposition

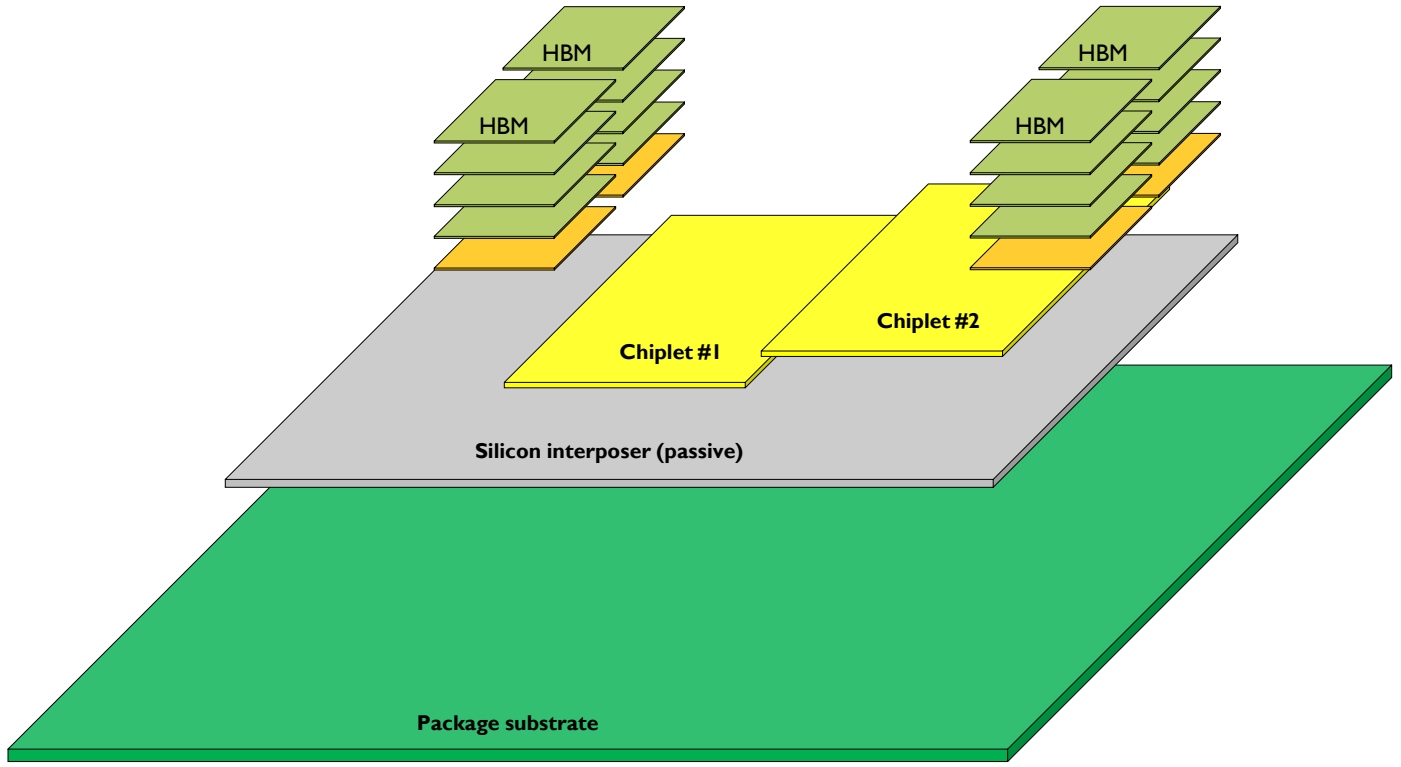


+60 potential ACC. (non exhaustive)

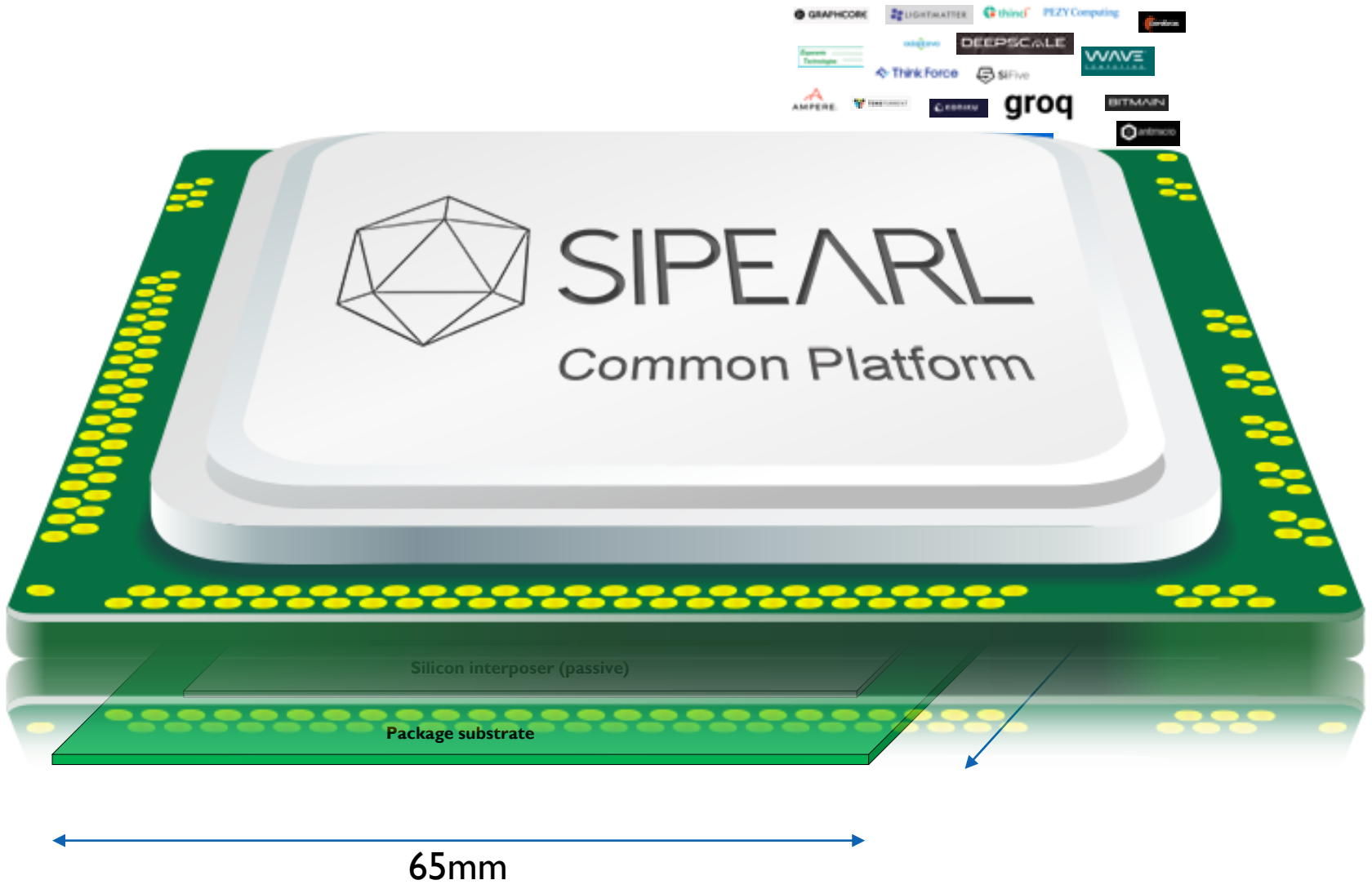
GRAPHCORE, LIGHTMATTER, thinci, PEZY Computing, cerebras, Esperanto Technologies, adapteva, DEEPSCALE, WAVE COMPUTING, Think Force, SiFive, AMPERE, TENSTORRENT, KONIKU, groq, BITMAIN, antmicro, GREENWAVE SYSTEMS, KALRAY, Tachyum, SambaNova SYSTEMS, krtkl, TERADEEP, ChipIntelli MAKE AI REAL, KNOWM, AMOTIVE, DEEP VISION, Kneron, LIGHTELLIGENCE, GREENWAVES TECHNOLOGY, MYTHIC, Cambricon, gyrfalcon technology, another brain, NOVUMIND, brainchip

THE COMMON **OPEN** PLATFORM IS THE EUROPEAN STANDARD FOR MANAGING EXTREME SPECIALIZATION

CONCEPT OF COMMON PLATFORM : INTERPOSER & MULTI-CHIPLET

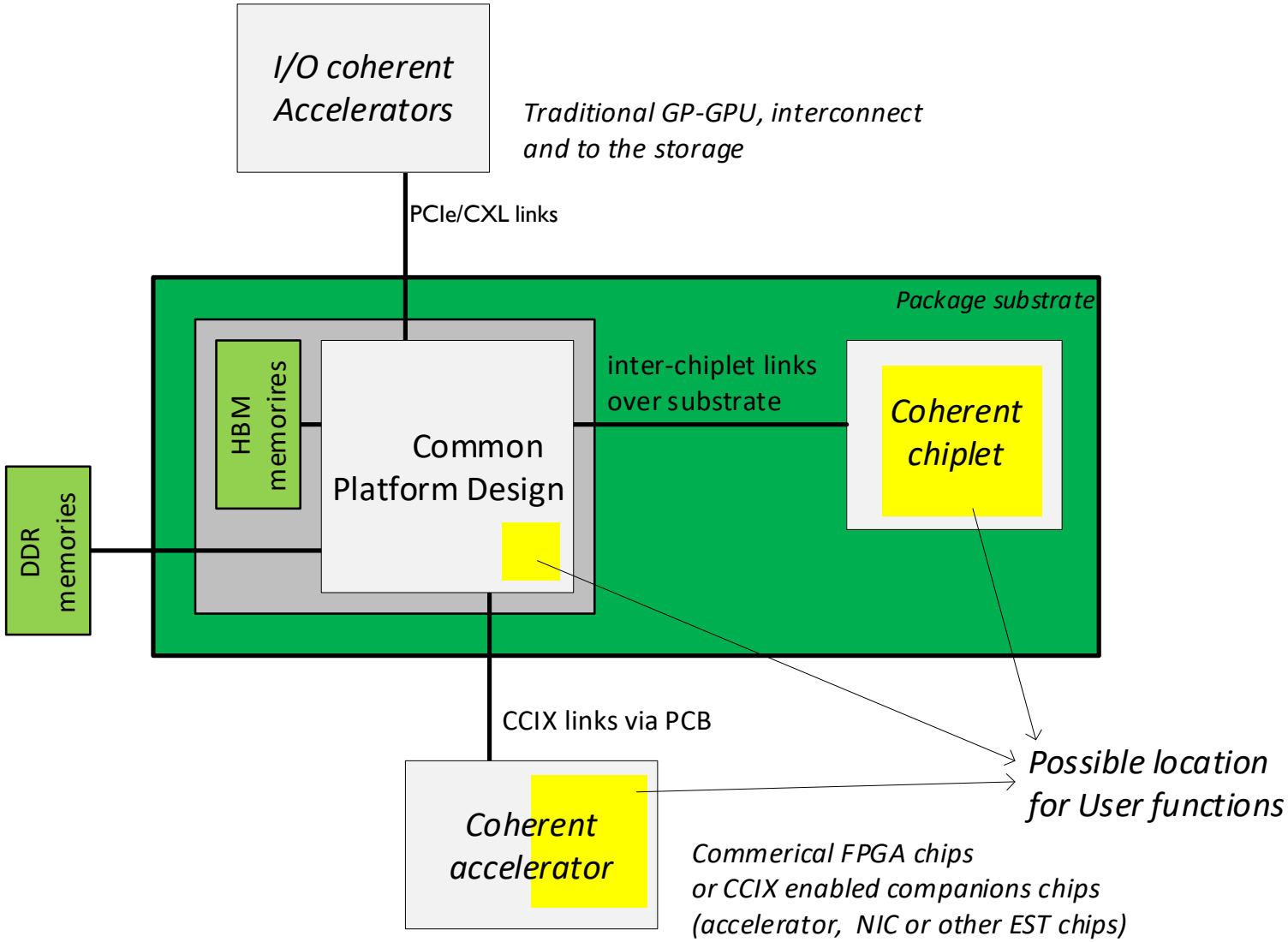


CONCEPT OF COMMON PLATFORM : INTERPOSER & MULTI-CHIPLET

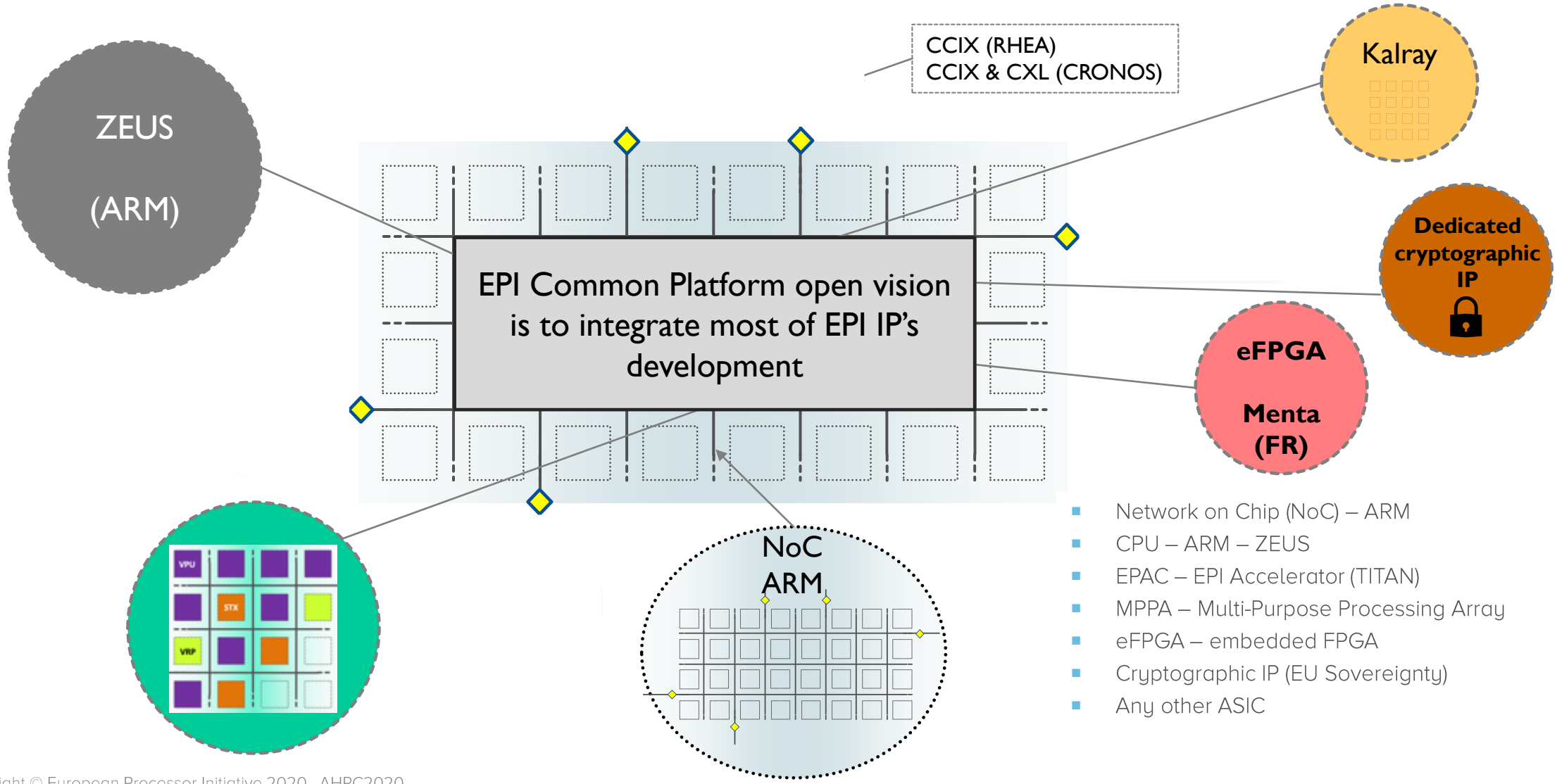


HETEROGENEOUS INTEGRATION

- Integrating customized functions at different levels
- EPI accelerator IPs today are integrated in Rhea design



GENERAL PURPOSE PROCESSOR (GPP) AND COMMON OPEN ARCHITECTURE

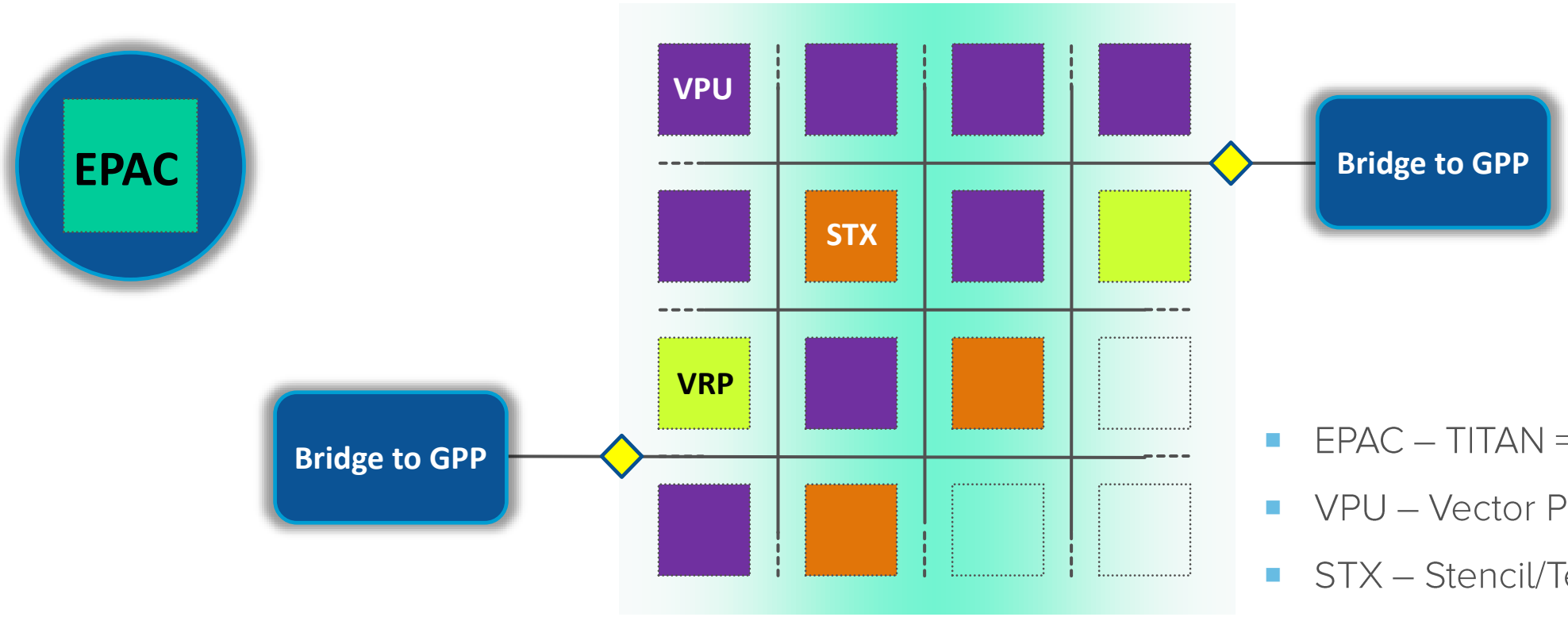


- Network on Chip (NoC) – ARM
- CPU – ARM – ZEUS
- EPAC – EPI Accelerator (TITAN)
- MPPA – Multi-Purpose Processing Array
- eFPGA – embedded FPGA
- Cryptographic IP (EU Sovereignty)
- Any other ASIC

CPU (RHEA) DESIGNS

- Multi-core Armv8.x processor for both computing and control flow (features to be announced)
- Very high Byte/FLOP ratio
- EPI Accelerators work in I/O coherent mode and share the same memory view
- Coherent NoC with system level cache to keep the data local
- HBM2e, DDR5 and PCIe gen5
- Very Low core voltage to improve the energy efficiency / N6 process

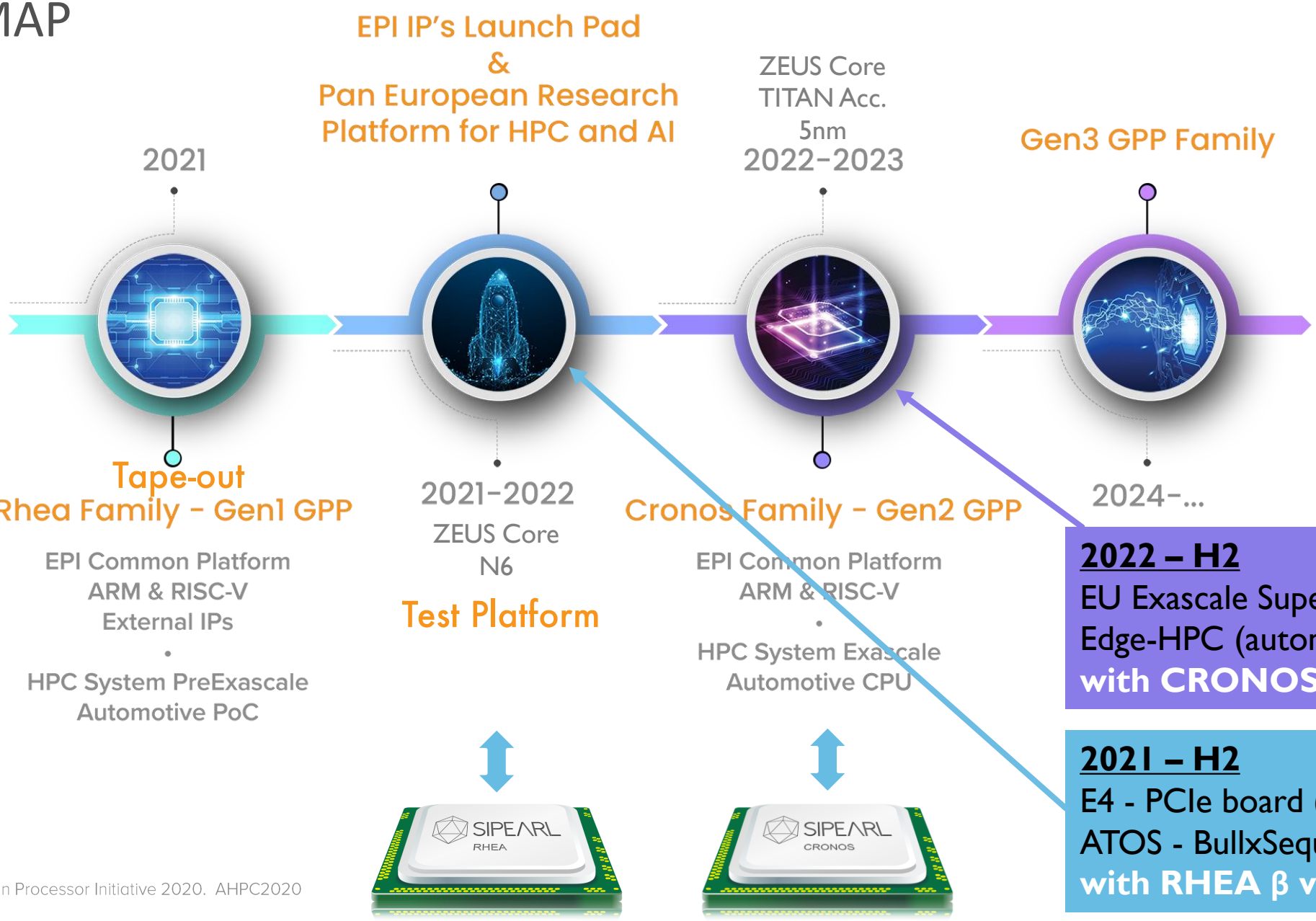
EPAC – RISC-V ACCELERATOR FOUNDATIONS



- EPAC – TITAN = EPI Accelerator
- VPU – Vector Processing Unit
- STX – Stencil/Tensor accelerator
- VRP = Variable Real Precision

THIS IS ONE OF THE FUNDAMENTAL RESEARCH DIMENSION IN EPI !!!
IT WILL END ONCE MATURE INTO A FULLY DEDICATED CHIP

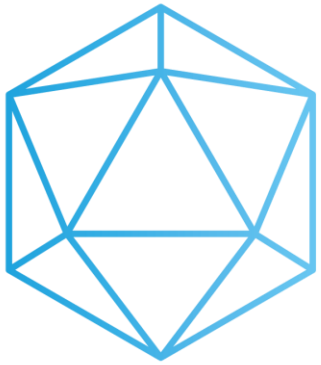
ROADMAP



2022 – H2
EU Exascale Supercomputer
Edge-HPC (autonomous vehicle)
with CRONOS & TITAN

2021 – H2
E4 - PCIe board (WS compatible)
ATOS - BullxSequana Board
with RHEA β version

CONCLUSION



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EUROPEAN APPROACH FOR (POST) EXASCALE CHALLENGES

Technology

- One CPU to rule all accelerators
- ARM is the best choice: performances, openness, unique IoT to Supercomputer ecosystem
- Chiplet based approach
- Common Open Platform

Open

- Common Open platform
- Open programming model
- Aim open hardware

Ecosystem (holistic)

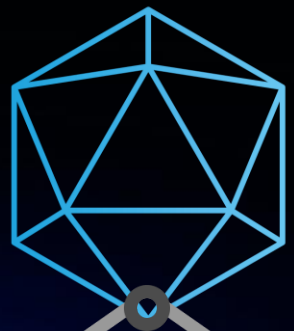
- ARM from IoT to HPC
- GCC and LLVM
- OPENMP 5
- OPENCL
- …

Business pragmatism

- From Research to Production → One vision but both feet on ground → SiPearl industrial hand
- Sustainable
- Profitable


TO MEET THE TEAMS
TO KNOW MORE ABOUT EP AND IT'S ECOSYSTEM
TO KNOW MORE ABOUT SILICON TECHNOLOGIES FOR DATA PROCESSING
Save the date
1st EPI Forum
March, 16-17th, 2020

European Processor Initiative



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WE'RE HIRING

Thank You for your attention

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