EPI Talks – EPIsode 1 of podcast, E4 and PCIe

AR: hi everybody, and welcome to this podcast. Let me introduce myself: my name is Agnese Reina, Communication Manager of E4 Computer Engineering. E4 is a technology provider and system integrator based in Emilia Romagna, Italy. E4's overall mission is designing, building and servicing the best HPC solutions for technical and scientific users, and leverage its technological leadership for developing solutions for AI, big data and emerging applications. E4 is a member of the European Processor Initiative (EPI). The core objective of the European Processor Initiative is the development of a European processor. Participating in the European Processor Initiative enables E4 to apply its skills and know-how towards the realization of an advanced, efficient processor and demonstrate in operational environments the successful integration of European HPC technology's building blocks, covering the full value chain developed in previous R&I actions. Fabrizio Magugliani, E4's Project Manager for EPI, is here with me

FM: hello everybody

AR: and he is the point of contact between E4 and the EPI organization and its members, taking care of the interactions with the consortium's members and of the deliverables. Fabrizio, can you tell us how E4 is contributing to the objectives of EPI?

FM: thanks Agnese for the introduction. First of all, I join Agnese in welcoming you to this podcast and please do not hesitate to contact me via email at fabrizio.magugliani@e4company.com for any questions. Within the European Processor Initiative, E4 has the primary task to develop the PCIe daughter board hosting the Test Chip and the first version of EPI's GPP (General-Purpose Processor). Let me talk about the broader picture of the EPI strategy and then I'll position the rationale for a PCIe daughter board within the broader picture. EPI intends to develop the IPs for a low-power design approach encompassing massive parallelism, specialized architecture, low-voltage operating point, and fine grain power management. The software stack will be designed for integrating and taking advantage of these features to achieve high-energy efficiency and maximize overall performance across a wide range of layers from the low-level firmware, all the way up to system software and application run-times. For this purpose, EPI will harmonize the heterogeneous computing environment by defining a common approach: the so-called Common Platform (CP). The Common Platform will include the global architecture (hardware as well as software) specification, common design methodology, and a global approach for power management and security. Before beginning the design and production of the HPC board hosting the GPP/Common Platform, it has been deemed important to develop a smaller, easy to build and easy to use but realistic preparatory testbed for allowing a wider set of users and developers to have access to the components and starting the testing of the components in a realistic user environment. To enable the widest diffusion of the testbed, E4 proposed to develop a PCIe-based daughter board hosting the components. Because almost all the servers, workstations, nodes currently deployed have a PCIe interface, the daughter board hosting the Test Chip and the GPP can be easily plugged in these servers without any additional interface, thus enabling the users to start their testing of the components and developing the applications.

AR: I see. What is the first component to be hosted on the PCIe daughter board?

FM: as of today, the Test Chip is the first component that will be implemented on the PCIe daughter card. The E4 design team is actively working within the Test Chip Work Package for designing the first version of the PCIe daughter board for the Test Chip. The Test Chip team is led by Fraunhofer and the other members of the Work Package are Extoll, Semidynamics, E4, ETHZ, FORTH, BSC, CEA, Chalmers. On the market side, E4 is working with SiPearl, who has the objective to develop, manufacture and sell the processor(s) based on EPI developments. As of today, there are still a number of technological challenges to be met and decisions to be taken about the optimal layout of the Test Chip and of the PCIe daughter board, but the objective looks doable, and let me say

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that I'm optimistic about the possibility that we will bring the PCIe daughter board into the market in 2021 as planned.

AR: looks interesting, and I am glad to see that the members of the Test Chip Work Package are coming from many European countries. Is also the European Processor Initiative a European-wide effort?

FM: sure, the whole EPI project is a truly European-wide initiative, involving 27 members and 10 countries. Actually, the objective of EPI is the successful integration of European HPC technology's building blocks, covering the full value chain (e.g. microprocessor, software, applications, interconnects) developed in previous R&I actions.

AR: who are the envisioned users of the PCIe daughter board?

FM: we think that there is a wide range of users who may be interested in the PCIe daughter board hosting the Test Chip and the GPP, primarily all those users working in institutions, enterprises, SMEs developing their own ecosystem and looking for having access to a preliminary version of the processor or components of it, as well as the developers of applications, either in-house applications as well as Independent Software Vendors, looking for the porting of their packages against the processor, in order to have their packages already available and fully tested when the processor is released.

AR: what is the best way to stay in touch with the progresses of EPI?

FM: the EPI web site https://www.european-processor-initiative.eu/ is the best way. The site is kept up-to-date with the latest progresses of the project. Also, an excellent opportunity to learn about the EPI is the EPI Forum which will take place in 2021. We envision the EPI forum as an event where the partners of the consortium and the interested institutions, enterprises and developers come together to mix and match.

AR: thanks, Fabrizio. As mentioned by Fabrizio, I encourage you all to check at the EPI web site https://www.european-processor-initiative.eu/ for the latest updates. With this, this podcast concludes. Thank you all for having participated and stay tuned for the updates.

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