European Processor Initiative

EPI PCIE DAUGHTER CARD AS SOFTWARE DEVELOPMENT VEHICLE

FABRIZIO MAGUGLIANI (E4 COMPUTER ENGINEERING)

EPI TUTORIAL

FIRST STEPS TOWARDS A MADE-IN-EUROPE HIGH-PERFORMANCE MICROPROCESSOR

HIPEAC, BOLOGNA, ITALY, 14:00 TO 17:30 JANUARY 22, 2020,
BOLOGNA POLO CONGRESSUALE, ROOM BIANCA B

The tutorial/training will provide most up-to-date information on European Processor Initiative project and its activities.

SECTION	FROM	TO	TOPIC	SPEAKER
Intro, General Overview, Accelerator, PCIe	14:00	14:15	Introduction to tutorial	Josip Knezovic, University of Zagreb
	14:15	14:30	General EPI overview	Denis Dutoit, CEA
	14:30	14:45	Common Platform & Rhea 1st implementation	Denis Dutoit, CEA
	14:45	15:10	Accelerators & Power aspects	Mauro Olivieri, BSC & Andrea Bartolini, University of Bologna,
	15:10	**15:30**	EPI PCIe daughter card as software development vehicle	Fabrizio Magugliani, E4
	15:30	16:00	BREAK	
EPI and RISC-V	16:00	17:30	EPI RISC-V Vector Compiler explorer, Emulator Visualizer + Hands-on	Filippo Mantovani, BSC & Roger Ferrer Ibanes, BSC

WHY A PCIE DAUGHTER CARD?

For the development , testing and ‘stress’ of the design.

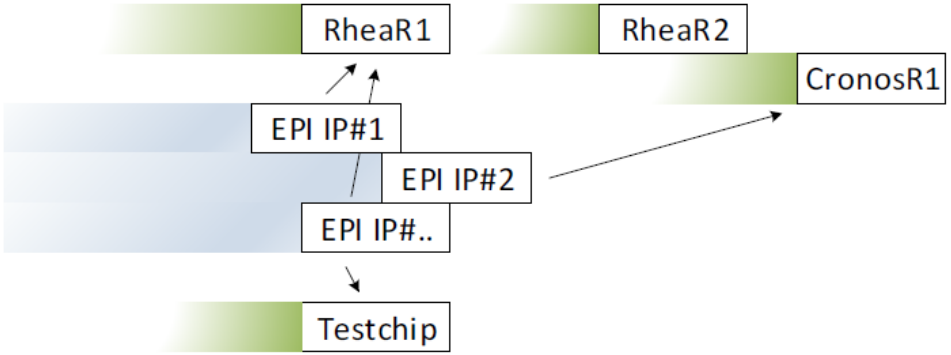
For validating the hardware units, develop the software, and run applications

A PCIe daughter card hosting the GPP, test chip is

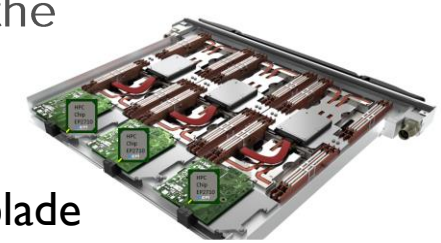
- (relatively…) Easy to design
- Easy to install on any platforms having a PCIe slot (who doesn’t???)
- Easy to change configuration/set-up/update system software & drivers
- (relatively…) Affordable (targeting a large potential market)
- Providing key feedback to the design team
- Providing an ideal development platform to developers, ISVs,

WHERE A PCIE DAUGHTER CARD FITS IN THE OVERALL EPI PICTURE?

- Rhea will be the first EPI General Purpose Processor
- Rhea targets HPC application
- Rhea is the first « instantiation » of EPI Common Platform
- Rhea design is lead by SiPEARL (the EPI fabless company) and joint-developed by EPI partners.

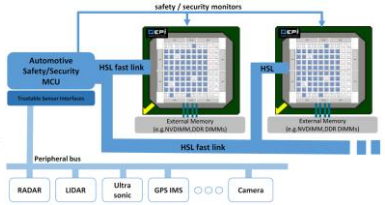


- Rhea chip will be integrated into test platforms in order to validate the hardware units, develop the software, and run applications.



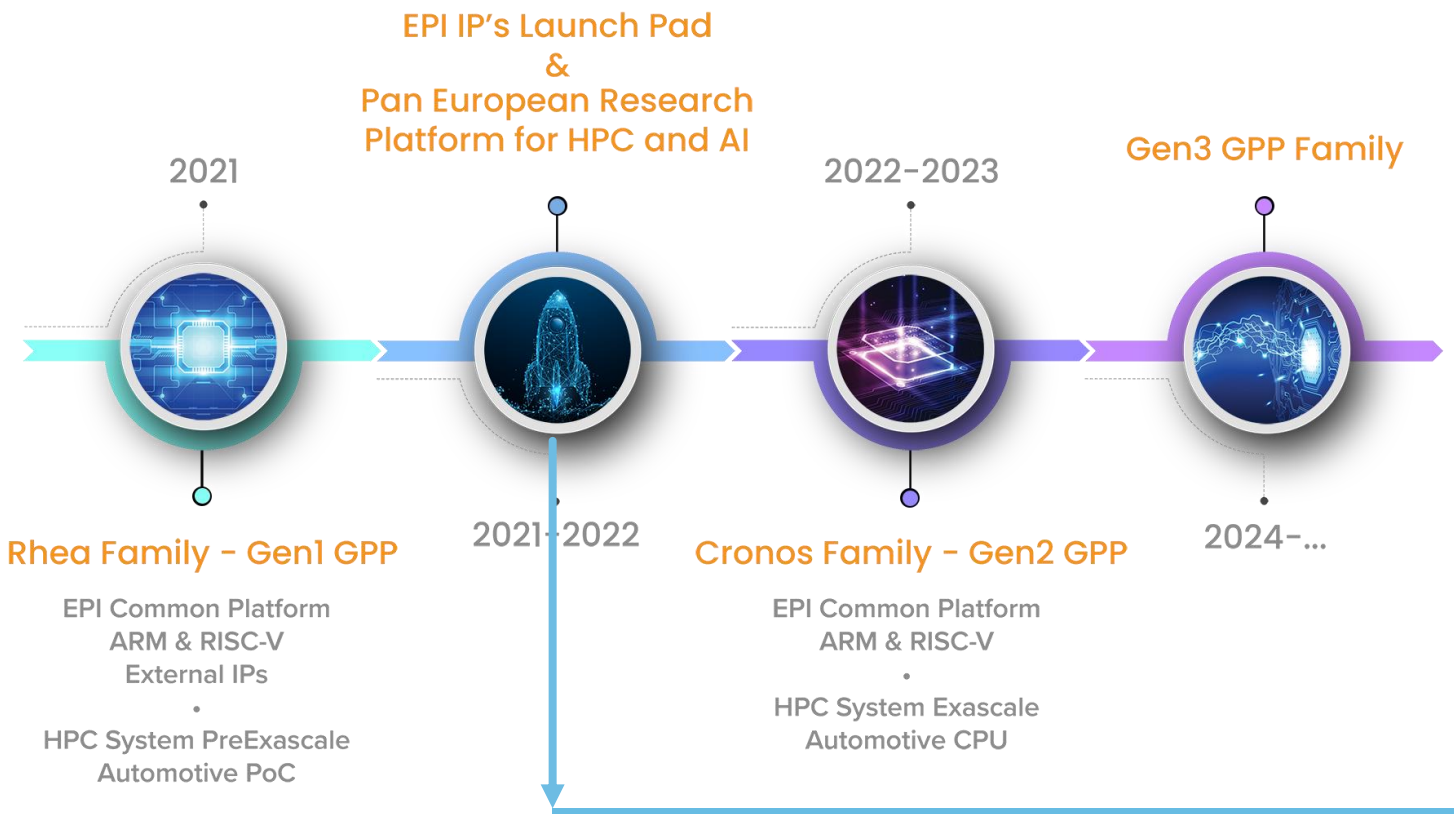
HPC blade

Automotive PoC



PCIe daughter card

WHEN A PCIE DAUGHTER CARD?



E4 Computer Engineering
2021 – H2
PCIe daughter board with < RHEA β version

CURRENT STATUS OF THE PCIE DAUGHTER CARD

Design in progress:

- Functional specs defined
  - Mechanical layout. ✔
  - Electical layout ✔ (almost…)

- Work in progress
  - Thermal profile 
  - Pin out 

CONCLUSION

- The PCIe daughter board is instrumental for the development , testing and ‘stress’ of the design of the EPI
- When the board has reached a production quality, it will represent the ideal hardware and software development platform
- Stay tuned….

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COFFEE BREAK

GET BACK AT 16:00