WORKSHOP ON RECONFIGURABLE COMPUTING: ROLE OF THE EMBEDDED FPGA CORE INTO EPI CHIP

HIPEAC 2020

BOLOGNA, ITALY

IMEN BAILI (MENTA)

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European Processor Initiative

HIPEAC

menta

FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES

THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION'S HORIZON 2020 RESEARCH AND INNOVATION PROGRAMME UNDER GRANT AGREEMENT NO 826647

FPGA ?

- Field Programmable Gate Array
- Widely used in electronic circuits
- Contains programmable logic blocks and interconnection circuits
- It can be programmed or reprogrammed to the required functionality after manufacturing
- Performs any logic function

It is a scalable, and optimized solutions for the server market

FPGA Board example

FPGA APPLICATIONS ?

- Random logics, SPLDs, device controllers, communication encoding and filtering
- The emulation of entire large hardware systems via the use of many interconnected FPGAs
- They offer a powerful solution for meeting machine vision, motor control and video surveillance
- FPGAs are used in custom computing machines
- Server applications such as:
  - Industrial network and fabric I/O
  - Intelligent NIC functions
  - Machine learning scoring acceleration
  - Data encryption
  - System management
  - And base-board management control server applications

Inside the Microsoft FPGA-based configurable cloud

Microsoft has been deploying FPGAs in every Azure server over the last several years, creating a cloud that can be reconfigured to optimize a diverse set of applications and functions.

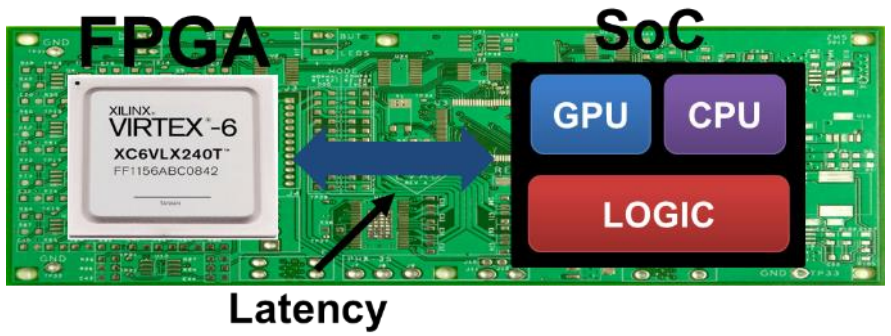
Deep Dive into Alibaba Cloud F3 FPGA as a Service Instances

Altera and Intel announced on June 1, 2015 that they had agreed that Intel would acquire Altera

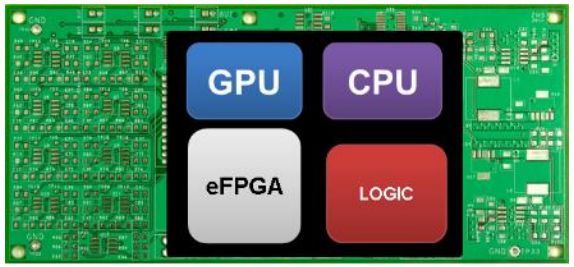
It is a scalable, and optimized solutions for the server market

MENTA EFPGA VS FPGA ?

	Menta eFPGA	FPGA
Size (eq. LCs)	0.05K to 200K per IP (with roadmap to increase that number)	Xilinx & Altera: 52K to 3M Microsemi: 5K to 500K Lattice: 0.6K to 40K
IO interconnect	Within SoC / ASIC	Through package (PCIe, SERDES, etc.)
GPIO (pins for eFPGA)	Up to 10 000	Up to ~400
Total interface bandwidth	Up to 12 000 Gb/s (14LPP)	~ up to 500 Gb/s
Latency	<1ns	30 to 50ns for most expensive FPGAs
DSPs	Custom	Fixed
Memory	Custom (can be 0)	Fixed amount: 2Mb to 54Mb
Foundry	At customer choice	Fixed
Radiation ready	At customer choice	Chose within a catalogue
Temperature range	At customer choice	Chose within a catalogue
Production volume	Mid to High	Low to Mid



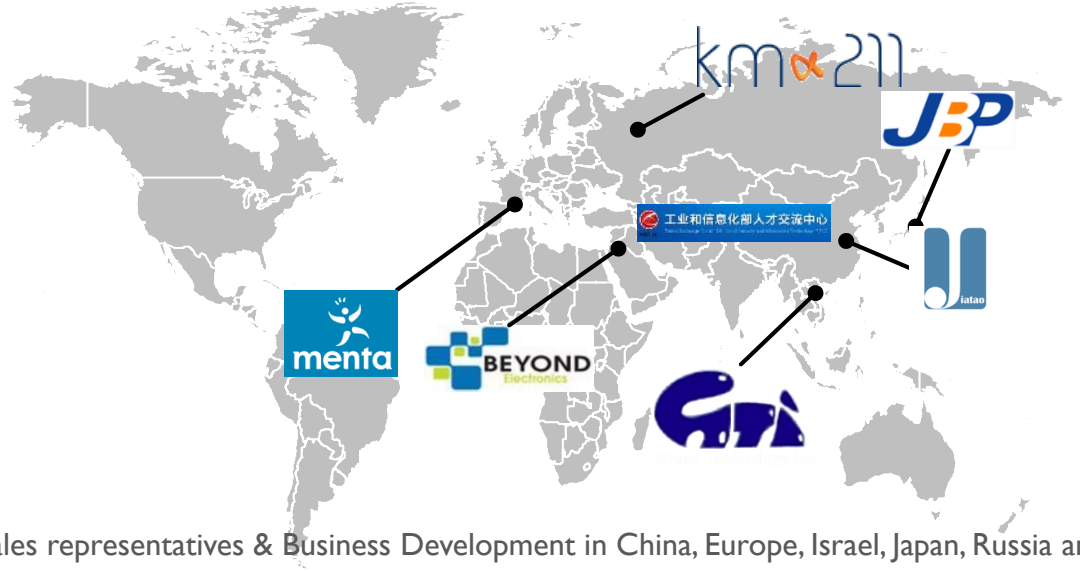
Improved performances
Lower power consumption
Lower BoM & board size



MENTA: THE EFPGA IP LEADER

MULTIPLE CUSTOMERS AND YEARS OF EXPERIENCE

17 employees – Sophia Antipolis, France



Sales representatives & Business Development in China, Europe, Israel, Japan, Russia and Taiwan

Some Customers

EUROPEAN DEFENCE AGENCY
ThalesAlenia Space
CHX
DGA
European Processor Initiative

HQ and R&D: Sophia-Antipolis, France

Sales representatives & Business Development in China (incl. Taiwan), Israel, Japan, North America and Russia

12+ years of R&D

Patented third party standard cells IP

5TH GENERATION DESIGN ADAPTIVE EFPGA IP

- High density & performances
  - Patented MLUTs - LUT6 based
- Fully flexible
  - Number of eLBs
  - ASIC like eMBs: type, quantity & size
  - eCBs:
    - Catalogue of DSP blocks (MAC, CDSP)
    - Custom blocks
  - Number of IOs
- No specific interface
  - Data: AXI, AHB, proprietary buses, direct connections, etc.
  - Configuration: SPI, AXI/AHB, JTAG, etc.

- Various ASIC like power management options
- Standard scan chain. TC > 99.7%
- 100% 3rd party standard cells based
- Robust verification flow
- Bitstream storage: no SRAM bitcells. Using DFF

EFPGA FOR EUROPEAN PROCESSOR INITIATIVE CHIP

- Fully European embedded field programmable gate arrays “eFPGA”, based on Menta version 5 architecture technology.
- Pure digital IP guarantees a very fast delivery,
- Menta’s standard-cell based approach enables rapidly porting the eFPGA IP to whatever new process geometry/variant desired, using the same automated, standard EDA flow as for the rest of the SoC.
- It offers the most robust verification flow as well as a standard scan chain DfT
- It offers the best possible yield by avoiding using SRAM bitcells to store the bitstream

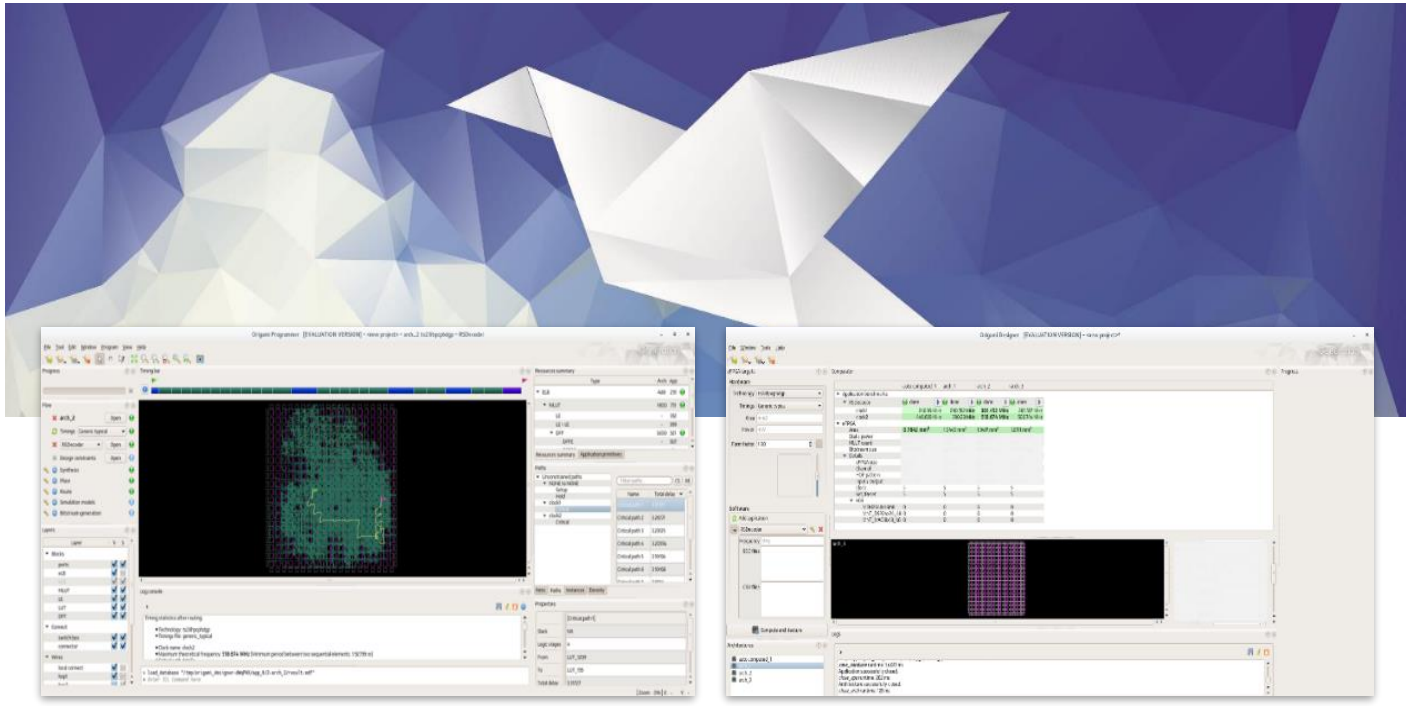
MENTA'S UNIQUE EFPGA IP SPECIFICATION SOFTWARE

Origami Tool suite

The technology does not rely on 3rd party software tools which target "generic" FPGA architectures, thus delivering suboptimal results.

- Menta software is self contained
- It can be provided as an API to be integrated into customer SW framework
- It could be directly called by customer HLS in a transparent way

Unified Software Platform



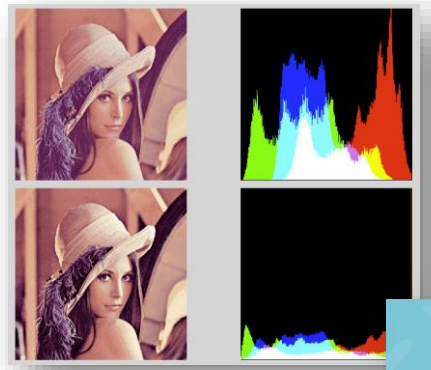
Origami Programmer
From RTL to bitstream

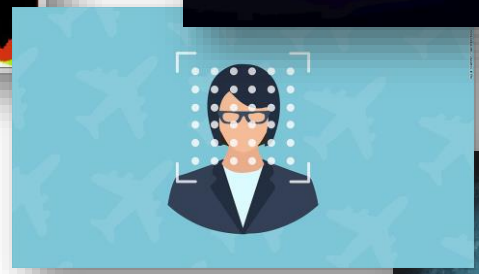
Origami Designer
eFPGA IP definition

EFPGA FOR EUROPEAN PROCESSOR INITIATIVE CHIP

Menta eFPGA IP is optimized for general purpose HPC and Automotive applications like:

- Image-processing using machine-learning (ML)
- Face recognition
- Data Prefetching and reconfigurable DMA Engine





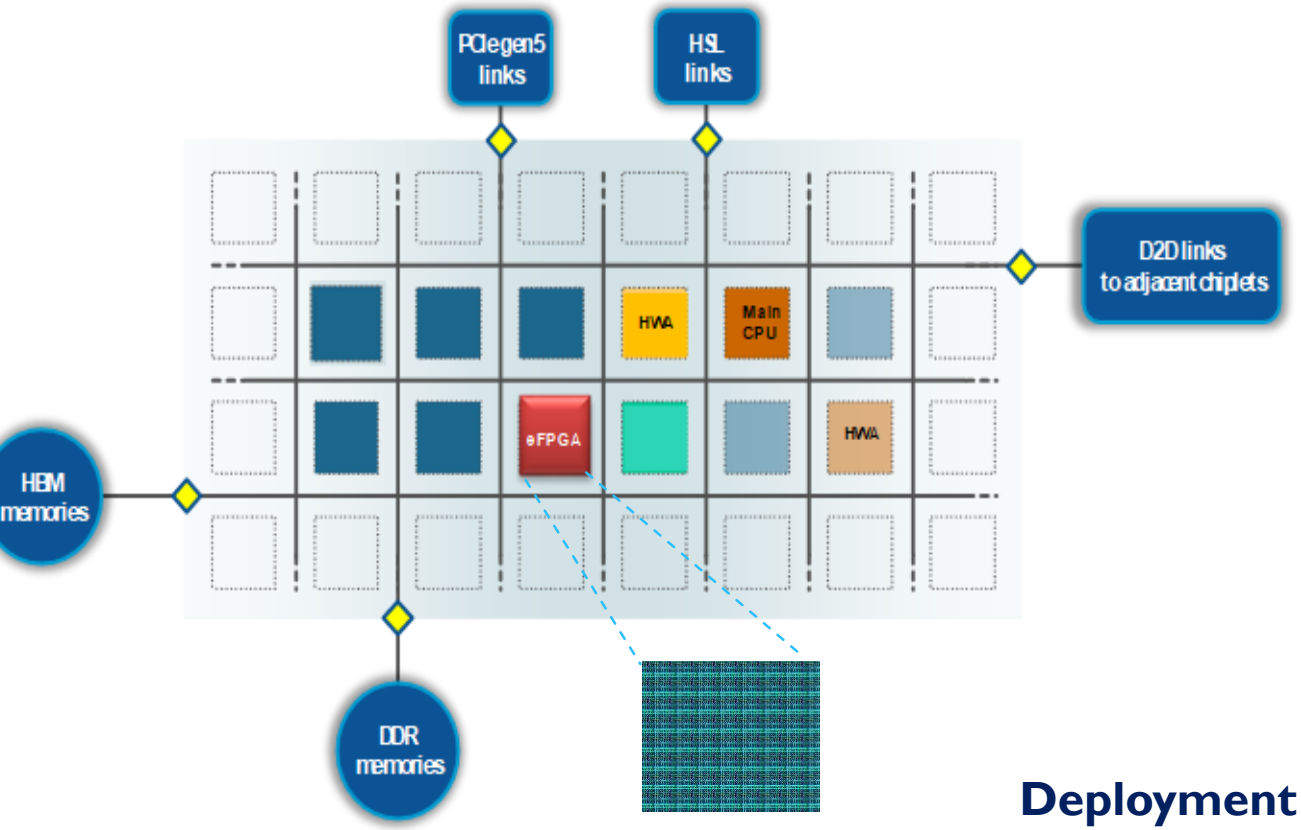
It is allowing post-production functions such like:

- Bug fixes
- Customer customization and proprietary elements

In addition, it is ensuring strengthen consideration of security aspects, like:

- Run-time reconfigurable crypto
- Post quantum public crypto key

EFPGA FOR HPC APPLICATIONS



- The eFPGA is a Key differentiator IP of the GPP Chip, which is integrating high-performance computing requirements of exascale machines.
- The eFPGA is allowing intensive computing and is allowing re-programmability of the SoC for high-performance computing applications
- HPC functions, like hardware acceleration, Machine learning acceleration, crypto security, are moved on-chip, without the limitations/overhead due I/O pad-count or chip-to-chip communication interfaces.

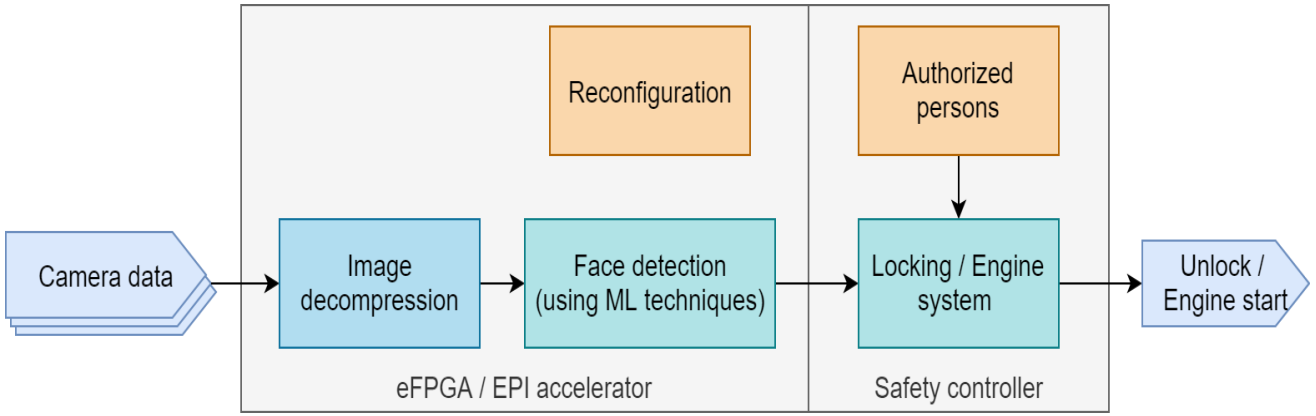
Deployment of Menta eFPGA technology to researchers and academicians, in addition to HPC Industrials

Menta Selected as Sole Provider of Embedded FPGAs for European Processor Initiative

"Our participation in this consortium really highlights the ability of our eFPGAs to be provided on any process technology, even the most advanced, such as 7nm, thanks to our third-party standard cells approach," says Vincent Markus, CEO of Menta.

https://www.embedded-computing.com/processing/european-processor-initiative-designates-menta-provider-of-efpga-ip

AUTONOMOUS DRIVING:
IMAGE PROCESSING & FACE RECOGNITION



Objectives:

- Unlock the car as soon as an authorized person approaches the car
- Start the engine if an eligible person takes place on the driver seat
- Example scenario: your child is able to unlock the car and take place inside; however, you want to prevent him or her from starting the engine

CONCLUSION

- Menta eFPGA is Key part of an optimal hardware/software codesign system composition, bringing reconfiguration options for the next generation of European HPC and Automotive industry
- Pure European IP, enabling to support future applications and customisations of the General Purpose Processor of EPI
- The unique EPI Chip with eFPGA solution targeting AI, ML networking and data-center applications
- eFPGA blocks allowing an attractive compromise between flexibility and efficiency
- Ideally suited as co-processor blocks for efficient acceleration of challenging arithmetic tasks on SW-programmable kernels

EPI PARTNERS