

## **EUROPEAN PROCESSOR INITIATIVE**

FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES

## EPI embedded FPGA (eFPGA) core

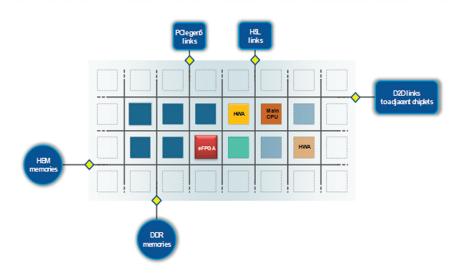
- European embedded field programmable gate arrays "eFPGA" is provided by Menta now in the fifth architecture generation.
- Pure digital IP guarantees a very fast delivery; Menta's standard-cell based approach enables a rapid port of the eFPGA IP
  to a new process geometry/variant, while using the standardized and automated tool flow for SoCs.
- It is a key differentiator IP of the GPP Chip integrating high-performance computing requirements of exascale machines with dynamic configurability.
- It enables hardware accelerators improving density, intensive computing and programmability of SoCs for high-performance computing applications as well as automotive applications.
- The technology is provided with an ASIC-like design for test and verification methodology that is crucial to enabling the first success of IPs in the most advanced process nodes.
- The IP is supported by Menta's unique eFPGA IP specification software, Origami Designer which enables silicon architects
  to fine-tune the eFPGA fabrics to the requirements of high-performance computing and automotive control unit
  applications.

The eFPGA tile, which is integrated into the General Purpose Processor Chip (GPP), contributes to an energy-efficient allocation of the necessary performance by an optimal interaction with the main CPU and the dedicated Hardware Accelerators (HWA).

Menta eFPGA IP is optimized for general purpose HPC and automotive applications such as image-processing using machine-learning (ML). It allows post-production functions like customer customization and proprietary elements. In addition, it can consider emerging security aspects, like run-time reconfigurable crypto and post quantum public crypto accelerators.

The eFPGA core plays a key role in an optimal hardware/software codesign system, enabling reconfiguration options for the next generation of European HPC and automotive industry.

Hardware acceleration features are moved on-chip, without the limitations or overhead due I/O pad-count or chip-to-chip communication interfaces. The eFPGA core is provided to EPI customers with the corresponding programming software-tool. Origami Programmer, generates the bitstream that targets and optimizes RTL to the needs of Menta eFPGA architecture. The technology does not rely on third party software tools, which target generic FPGA architectures and thus deliver suboptimal results.







www.european-processor-initiative.eu





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