

**27**  
Partners

**10**  
Countries

## EUROPE'S AMBITION

Design a roadmap of future European low power processors targeting

- Extreme scale computing,
- High performance big data,
- Emerging applications
- Sovereignty (data, economical, embargo)

### MISSION

- European independence in High Performance Computing Processor Technologies
- EU Exascale machine based on EU processor by 2023
- Based on solid, long-term economic model, go beyond the HPC market
- Address the needs of European Industry (Car manufacturing market)
- End-to-end security
- Sovereignty (data, economical, embargo)

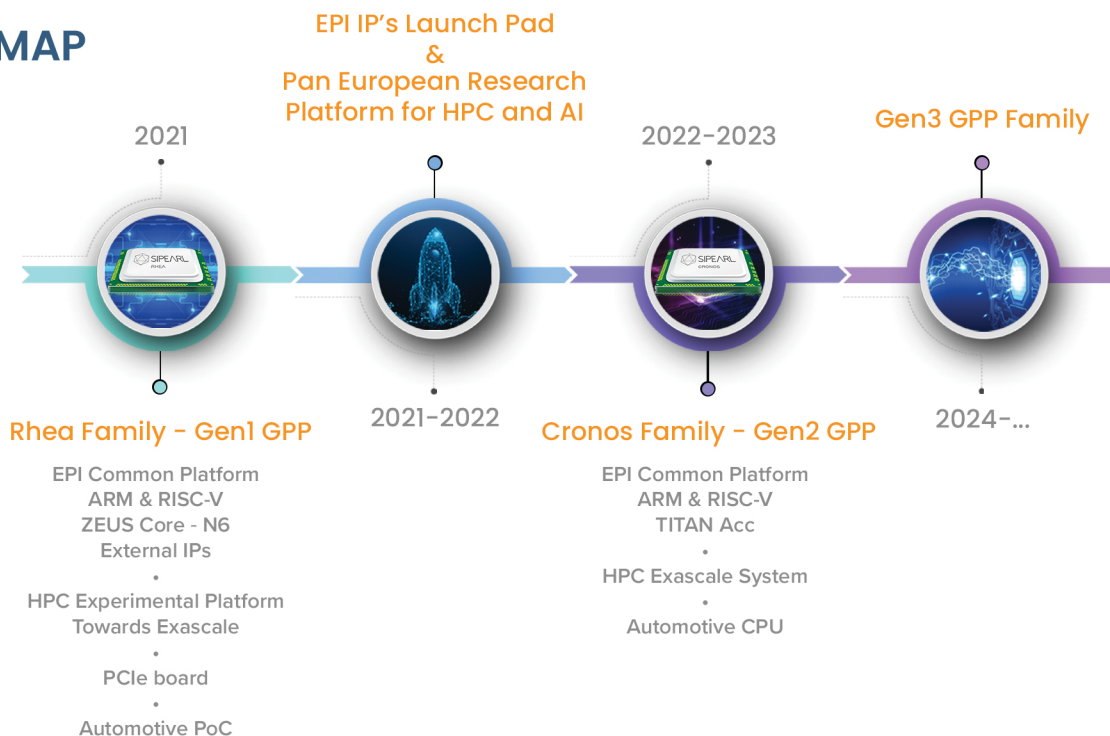
### VISION

- High Performance Computing needs for Exascale machines beyond 2022
- Connected mobility and Autonomous Driving computing needs beyond 2023
- Low power CPU needs for Servers and Cloud
- Other markets under exploration (Server, Cloud)

### IMPACT

- Strengthening the competitiveness and leadership of European industry and science
- European microprocessor technology with drastically better performance/power ratios
- Tackling important segments of broader and/or emerging HPC and Big-Data markets

## ROADMAP



### Common platform

Codesign, Architecture, System software and key technologies for the Common Platform

### General purpose processor

Design and implement of the processor chip(s) and PoC system

### Accelerator

Foster acceleration technologies and create building blocks IPs

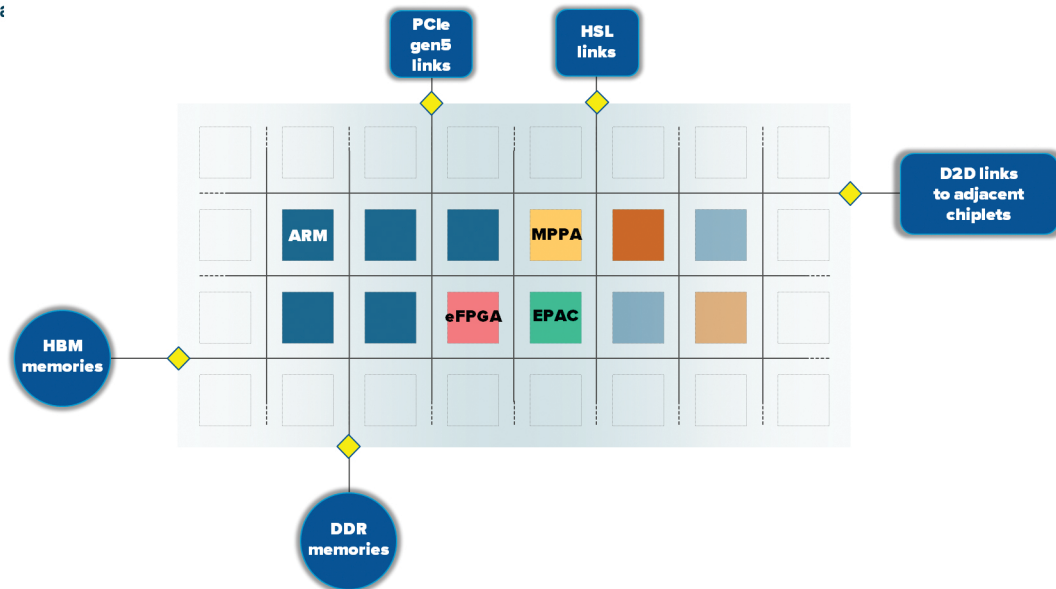
### Automotive

Address automotive market needs and create a pilot eHPC system

### Coordination

Management and support activities

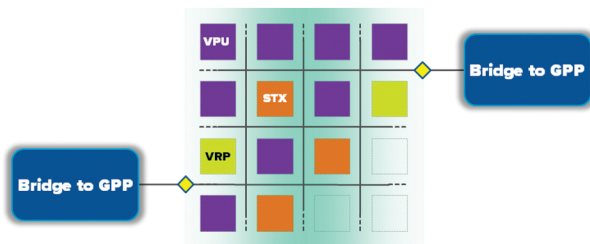
## COMMON PLATFORM



## OBJECTIVES

- Common Platform (CP) architecture to accommodate the developed technologies that will include the global architecture specification (hardware and software), common design methodology and global approach for power management and security
- General Purpose Processor (RheaR1), based on ZEUS core from Arm, ready for Exascale pilot machines
- Accelerator technologies (EPAC) based on RISC-V ISA accommodating HPC workloads
- Post-production dynamic hardware updates using programmable logic (eFPGA)
- Real-time acceleration PoC based on MPPA core
- Interfacing with the Automotive MCU
- Efficient power conversion technologies
- PoC systems (test-chip, ref. board, HPC blades, PCIe card and automotive PoC)
- Software activities based on the platform built
- Related research around the EPI project scopes

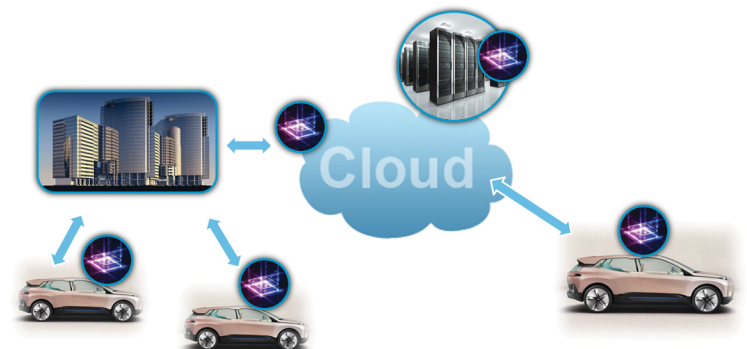
## ACCELERATOR



## TARGETS

- Energy efficiency for exascale level with general-purpose CPU core in the first EPI GPP chip
- Acceleration technologies for better DP GFLOPS/Watt performance
- Ease of use with adoption of Arm general-purpose CPU cores
- Best memory bandwidth and Byte per Flops ratio to maximize performance and efficiency for any application

## AUTOMOTIVE



## PARTNERS

