

European Processor Initiative: First year of activities

The project is finishing its first year with introduction of a new EPI Common Platform, an updated roadmap and presence at key events

The European Processor Initiative (EPI) <https://www.european-processor-initiative.eu/>, a project with 27 partners from 10 European countries, with the goal of helping the EU achieve independence in HPC technologies, is approaching the closure of the first year in its three-year cycle.

During that time, the consortium has submitted several architectural designs to the European Commission and is now ready to show its updated roadmap to the public.

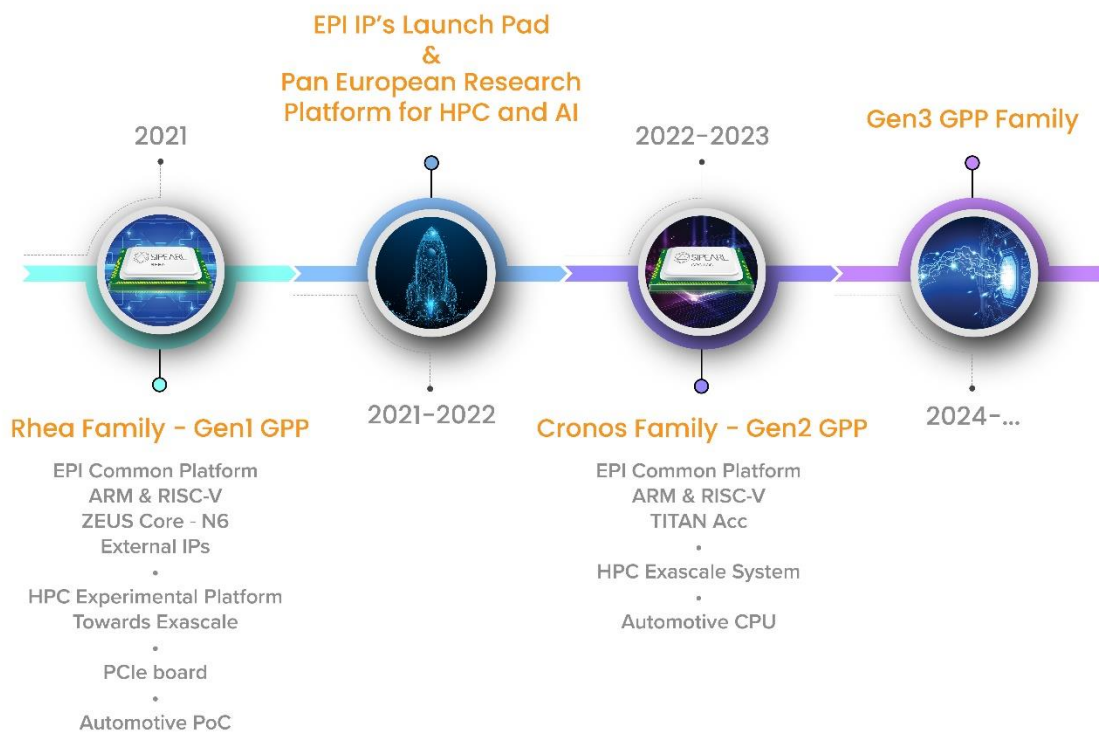


Figure 1. EPI Roadmap

The first-generation chip family, named Rhea, will include Arm ZEUS architecture general purpose cores and prototypes of high energy-efficient accelerator tiles: RISC-V based (EPAC), Multi-Purpose Processing Array (MPPA), embedded FPGA (eFPGA) and cryptography HW engine. First Rhea chips will be fabricated in N6 technology aiming at the highest processing capabilities and energy efficiency.

The Rhea chips will be integrated into test platforms, both in workstations and supercomputers in order to validate the hardware units, develop the necessary software interfaces, and run applications. Rhea aims to be the European processor for several experimental platforms towards exascale HPC and future automotive designs.

Today we also announce our long-term commitment to our recently introduced initiative to harmonize the heterogeneous computing environment by defining a common approach: the EPI Common Platform (CP). The EPI CP is in early development but will include the global architecture specification (hardware and software), common design methodology, and global approach for power management and security, in the future.

The CP in the Rhea family of processors will be organized around a 2D-mesh Network-on-Chip (NoC) connecting computing tiles based on general purpose Arm cores with previously mentioned accelerator tiles.

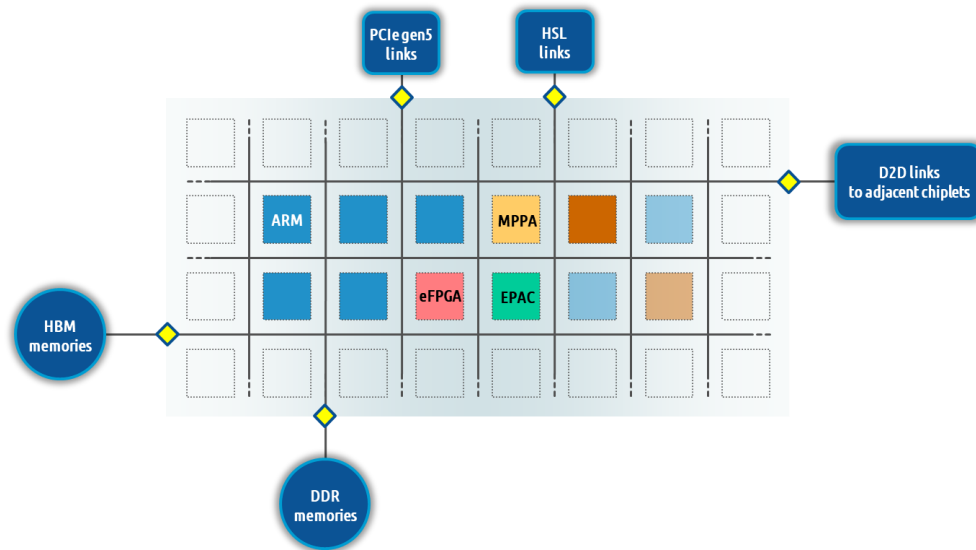


Figure 2. EPI Common Platform

A common software environment between heterogeneous computing tiles will harmonize the system, acting as a common backbone of IP components for IO connection with the external environment such as memories and interconnected or loosely coupled accelerators.

With this CP approach, EPI will provide an environment that can seamlessly integrate any computing tile. The right balance of computing resources matching the application needs will be defined through the carefully designed ratio of the accelerator and general-purpose tiles.

These important developments and more will all be presented at high-profile events the Initiative is attending, announced on EPI's web: <https://www.european-processor-initiative.eu/events/>.

We invite all interested parties to visit our exhibition booths at upcoming events, with special focus on the Supercomputing Conference in Denver, USA (Nov 17-22, 2019), booth #895, and the European Forum for Electronic Components and Systems in Helsinki, Finland (Nov 19-21, 2019).

Meet us there to discuss EPI's future!