EUROPEAN PROCESSOR INITIATIVE: FIRST STEPS TOWARDS A MADE-IN-EUROPE HIGH-PERFORMANCE MICROPROCESSOR

SCIENTIFIC DAY IRT ST-EXUPÉRY & GDR SOC2: RISC-V FOR CRITICAL EMBEDDED SYSTEMS

JUSSIEU CAMPUS, PARIS, FRANCE

3 OCTOBER 2019

DENIS DUTOIT CEA

European Processor Initiative

The RISC-V Week
Paris • October 1 to 3

October 1 – 2
2nd RISC-V Meeting

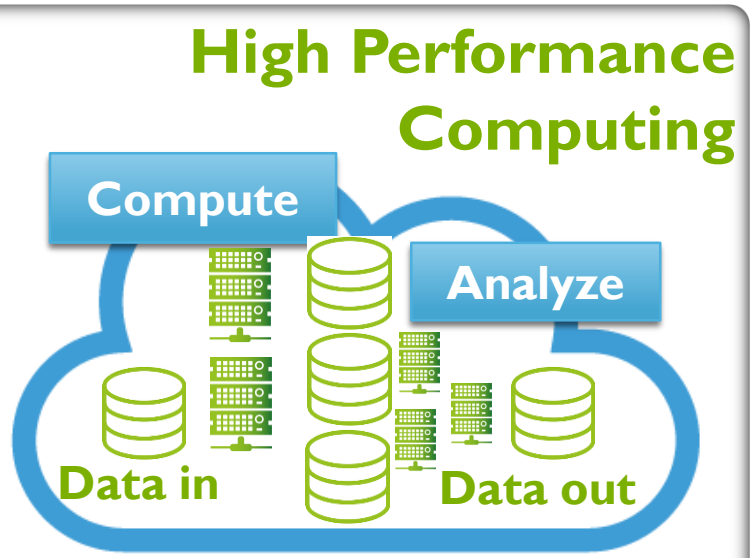
October 3
Scientific Day

AGENDA

- HPC challenges and associated architecture evolution
- European Processor Initiative (EPI):
  - General purpose Processor (GPP)
  - Accelerator
  - Automotive
- EPI Fabless Company
- Conclusion

HPC CHALLENGES AND ASSOCIATED ARCHITECTURE EVOLUTION

HIGH PERFORMANCE COMPUTING EVOLUTION



- **Starting from high performance compute only, HPC evolves towards:**
  - New workloads
  - Massive volume of data

New drivers	Requirements	Solutions
New workloads	More computing performance (Ops per second), also for simple operations (FP16, FP8, INT…). Energy efficiency (Ops per Watt).	***Heterogeneity: Generic processing + accelerators Low power design***
Massive volume of data	Increased Bytes per Flops. High bandwidth/low latency access to all data.	***High Bandwidth Memories and 2.5D integration***

➡ 10x energy efficiency improvement every 4 years

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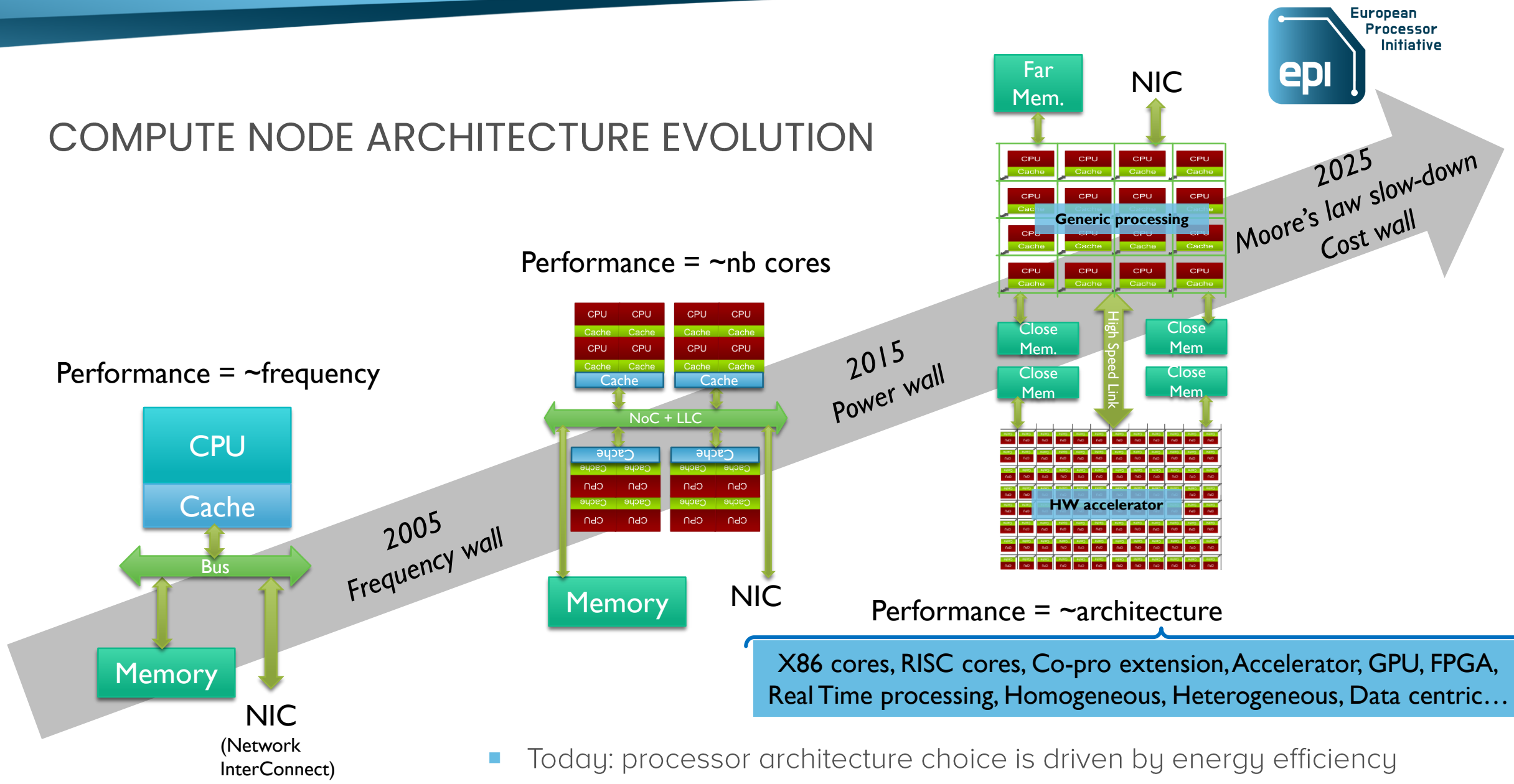
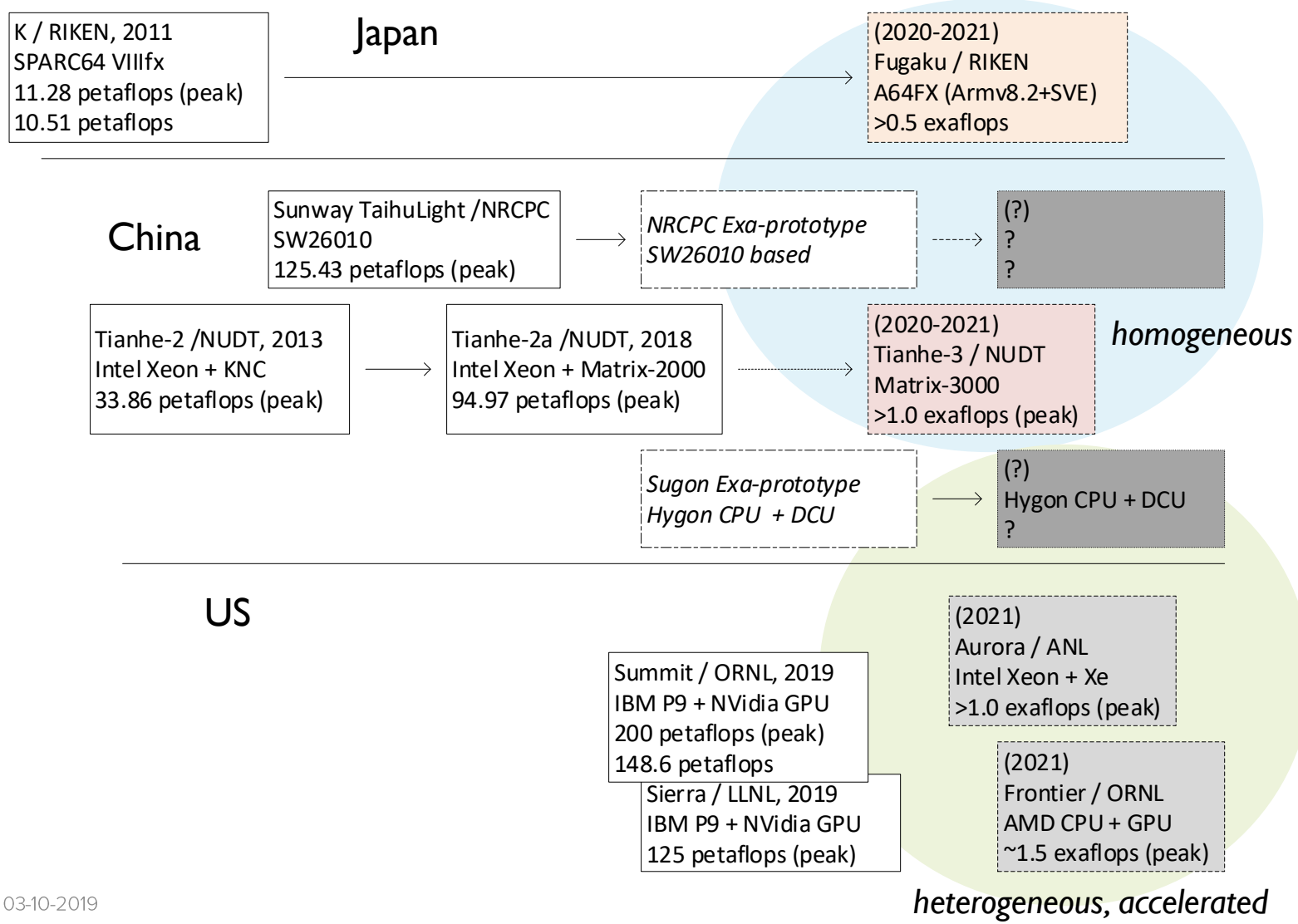
COMPUTE NODE ARCHITECTURE EVOLUTION



- Today: processor architecture choice is driven by energy efficiency

RACE TO EXASCALE

- CPU architecture choice:
  - Japan approach: Arm/SVE (homogeneous)
  - China approach: Custom many-cores (homogeneous)
  - US approach: x86 + GPU (heterogeneous)



EUROPEAN PROCESSOR INITIATIVE (EPI)

EPI – EUROPE'S AMBITION

- Design a roadmap of future European low power processors targeting
  - Extreme scale computing,
  - High performance big data,
  - Emerging applications

- FPA answering EU Horizon 2020 (FP8) ICT-42-2017 call

  * FPA : Framework Partnership Agreement
  * FP8 : Framework Programmes 8 for 2014-2020, succeeding FP7 (2007-2013)

EPI – MISSION

- European Independence in High Performance Computing Processor Technologies
  - Goal: EU ExaScale machines based on EU processor by 2023

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AND

- Based on a **solid, long-term economic model**
  - Go beyond the HPC market (not large enough)
  - Address the needs of European Industry ➔ Car manufacturing market

EPI – OUTCOMES

- High Performance General Purpose Processor for HPC (GPP)
- High-performance RISC-V based accelerator
- Computing platform for autonomous cars
- Common Platform to foster EPI roadmap (CoDesign Methodology, Platform for hardware and software, Power management, Modeling and Simulation)

European Processor Initiative

EPI IP's Launch Pad
&
Pan European Research Platform for HPC and AI

2021

Rhea Family - Gen1 GPP

EPI Common Platform
ARM & RISC-V
External IPs

2021-2022

RHEA
ZEUS Core - n6
•
HPC Experimental Platform
Towards Exascale
PCIe board
•
Automotive PoC

2022-2023

Cronos Family - Gen2 GPP

EPI Common Platform
ARM & RISC-V
ZEUS Core
TITAN Acc
5nm
•
HPC Exascale System
•
Automotive CPU

Gen3 GPP Family

2024-...

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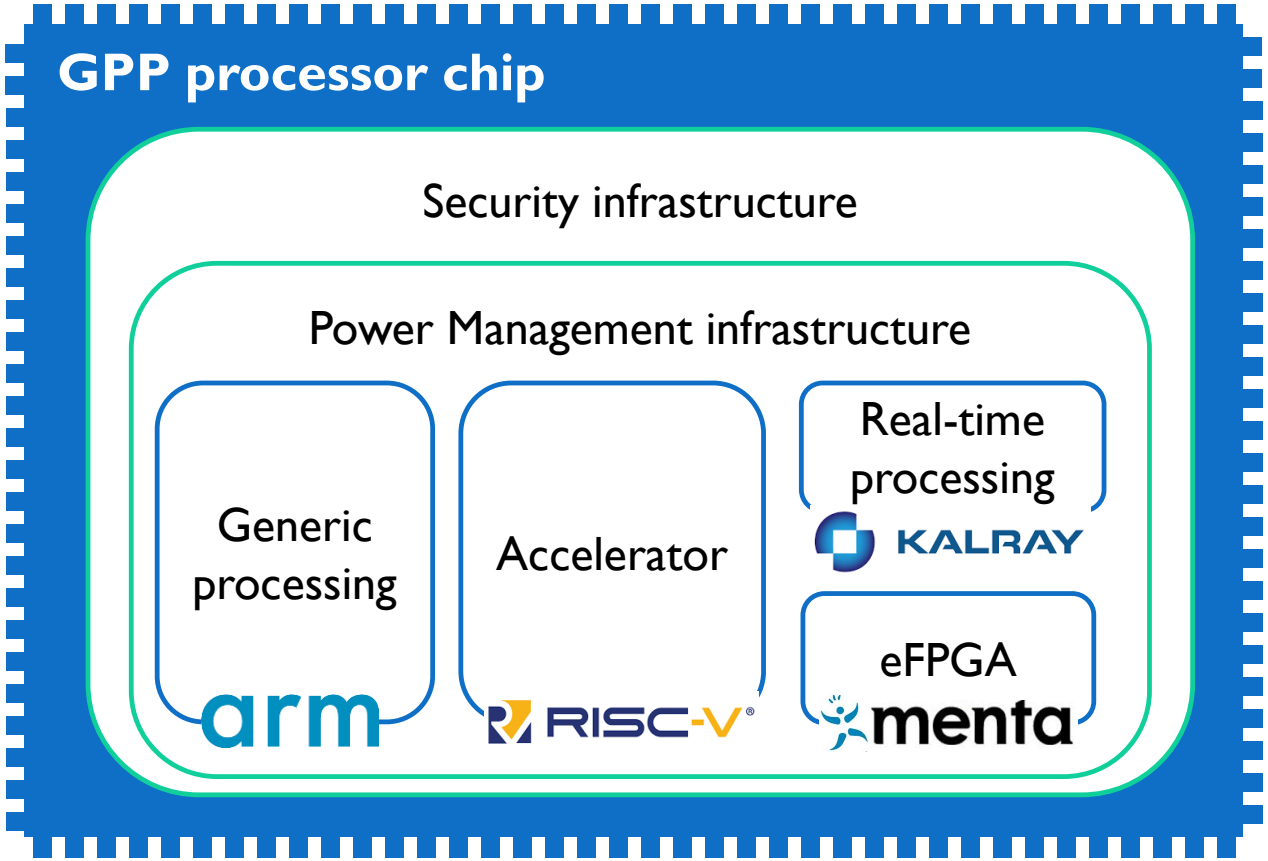
PROJECT PILLARS

- Common platform and global architecture stream
- HPC general purpose processor stream
- Accelerator stream
- Automotive platform stream

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 826647

GENERAL PURPOSE PROCESSOR (GPP)

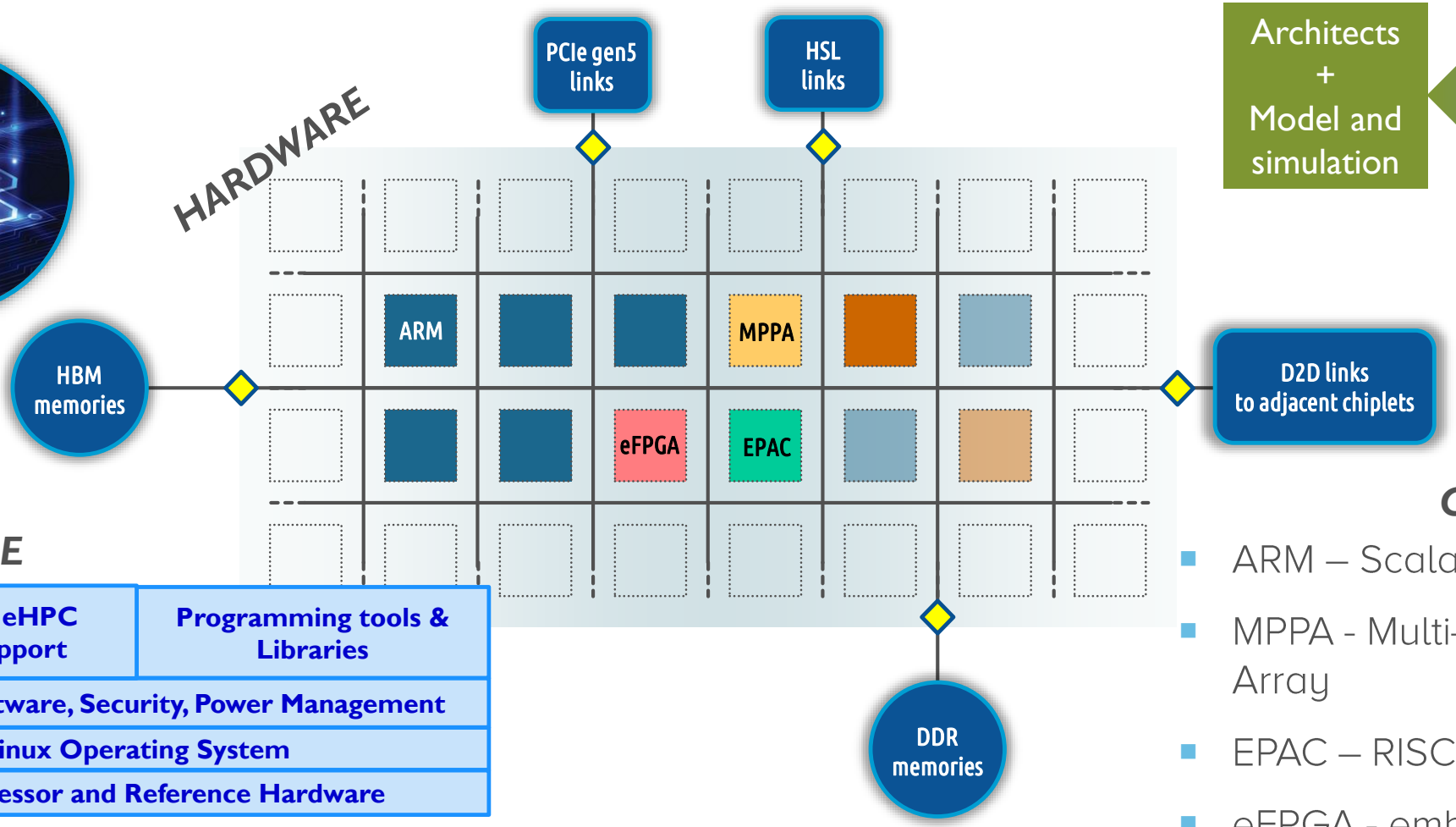
EPI POSITION STATEMENT ON PROCESSOR CORE SELECTION



- To adopt Arm general-purpose CPU core with SVE in the first EPI chip for pre-ExaScale level generic processing
- To develop RISC-V based acceleration technologies for better GFLOPS/Watt performance
- To include MPPA (Kalray) for real-time application acceleration
- To include eFPGA (Menta) reconfigurable logic for flexibility

COMMON PLATFORM TO ENABLE EASY TO USE ACCELERATORS

HARDWARE



METHODOLOGY

Architects + Model and simulation ⟷ Co-design ⟷ Application Experts

SOFTWARE

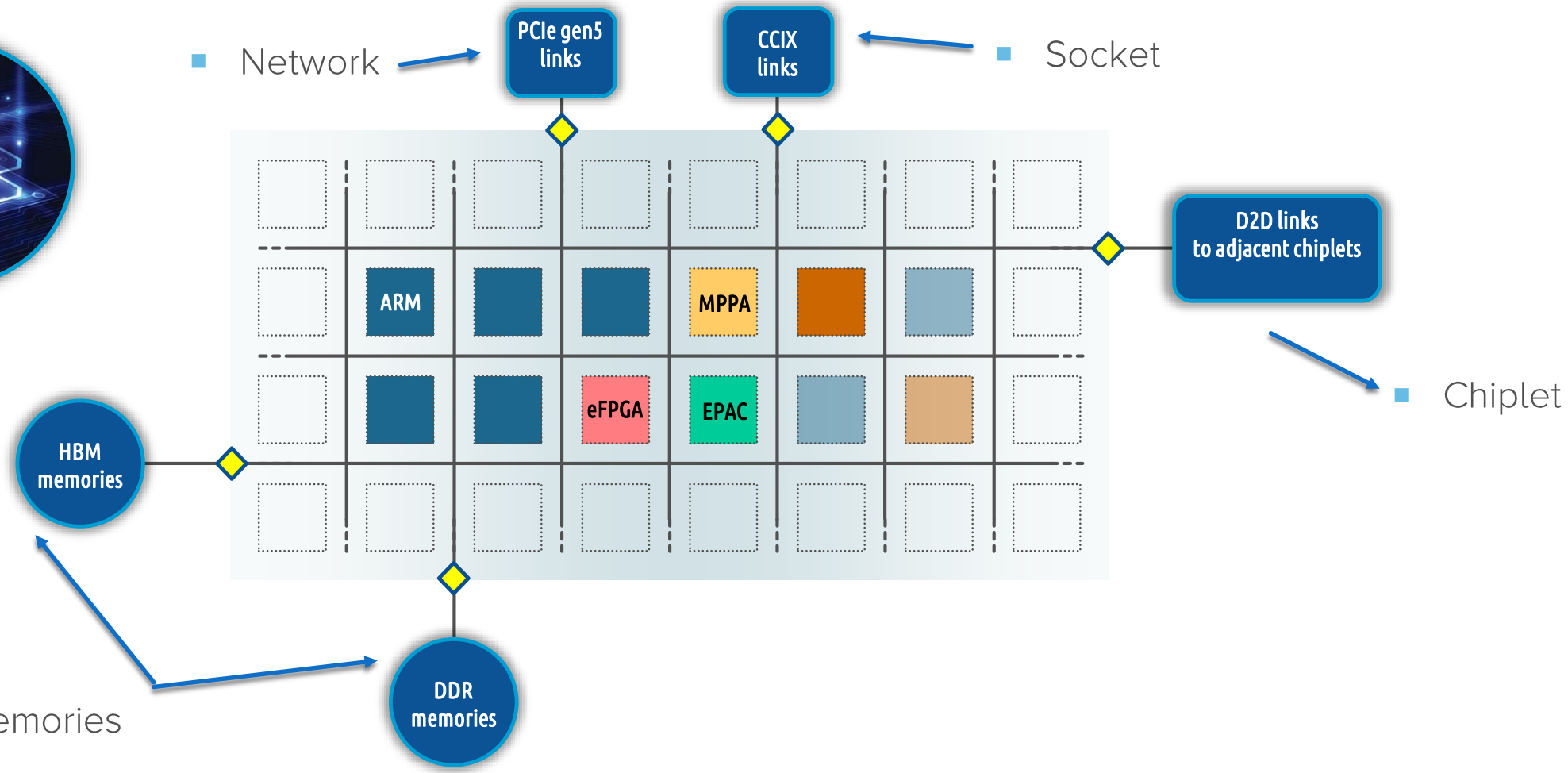
Automotive eHPC software support	**Programming tools & Libraries**
Low-level Software, Security, Power Management	
Linux Operating System	
EPI Processor and Reference Hardware	

COMPUTING UNITS

- ARM – Scalable Vector Extension
- MPPA - Multi-Purpose Processing Array
- EPAC – RISC-V based Accelerators
- eFPGA - embedded FPGA

OFF-CHIP INTEGRATION OF ACCELERATORS

- Network
- Socket
- Memories
- Chiplet



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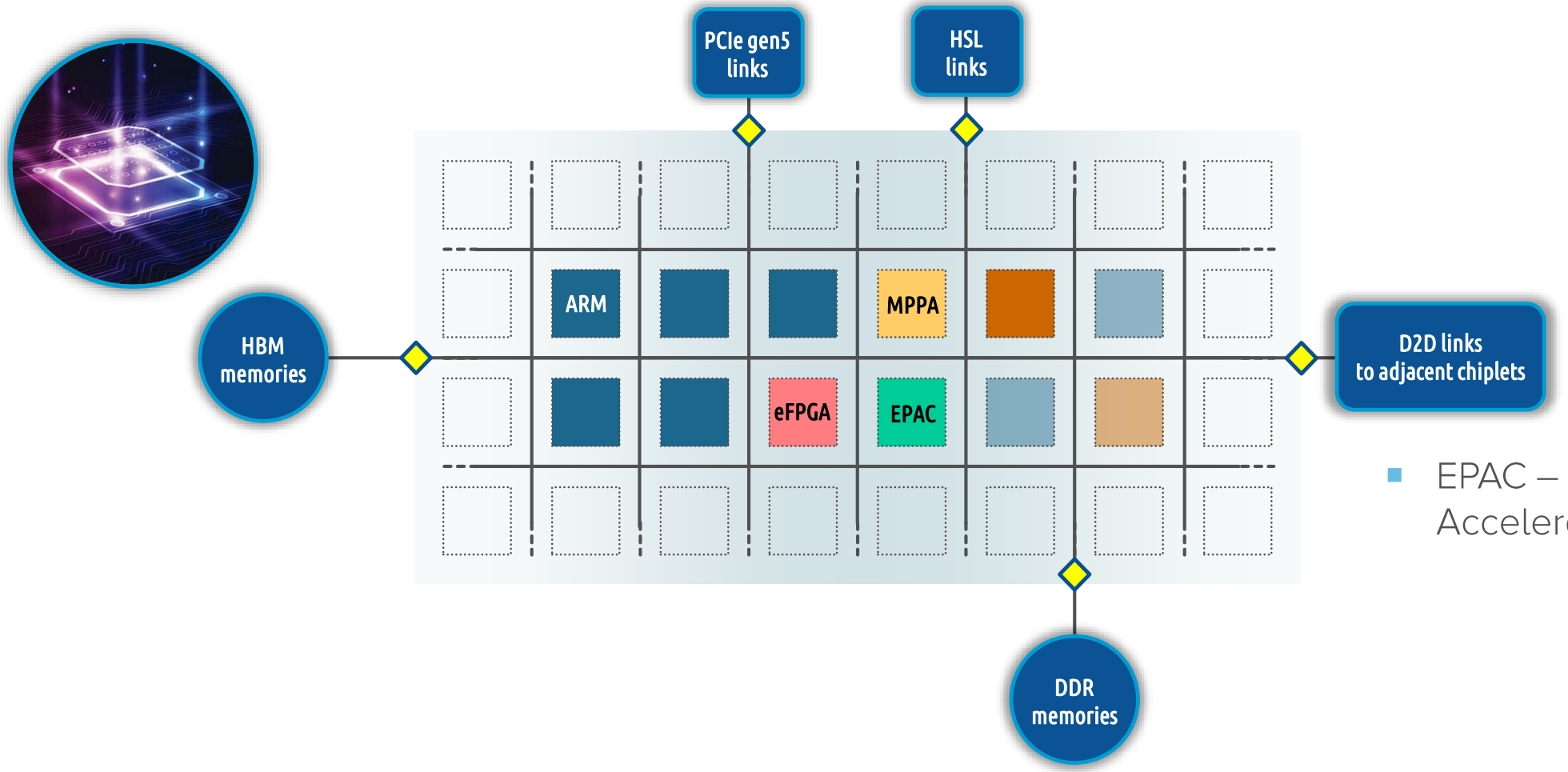
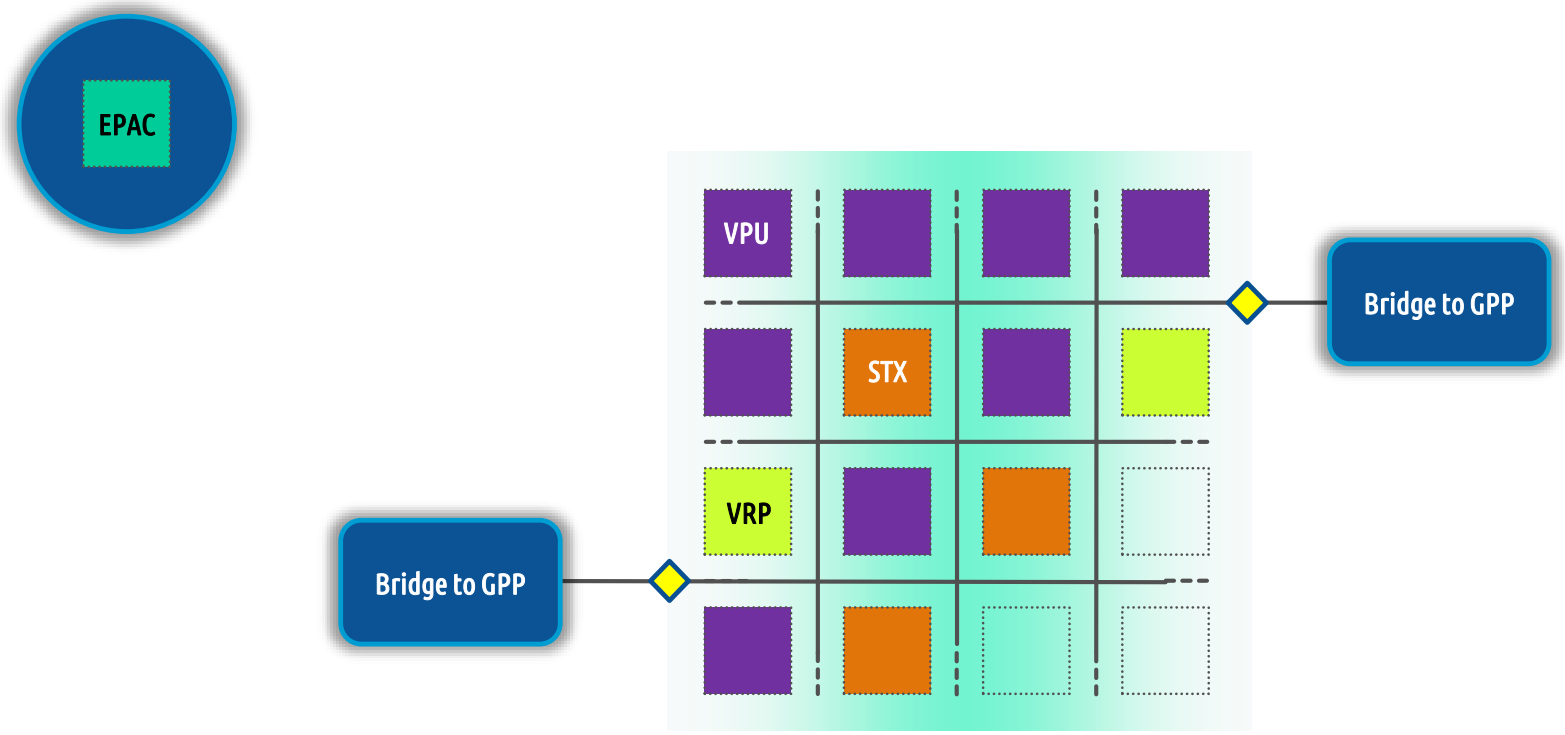
ACCELERATOR

RECALL… THE GPP AND COMMON ARCHITECTURE



- EPAC – RISC-V based Accelerators

EPAC – RISC-V ACCELERATOR



- EPAC - EPI Accelerator
  - VPU – Vector Processing Unit
  - STX – Stencil/Tensor accelerator
  - VRP - VaRiable Precision co-processor

AUTOMOTIVE

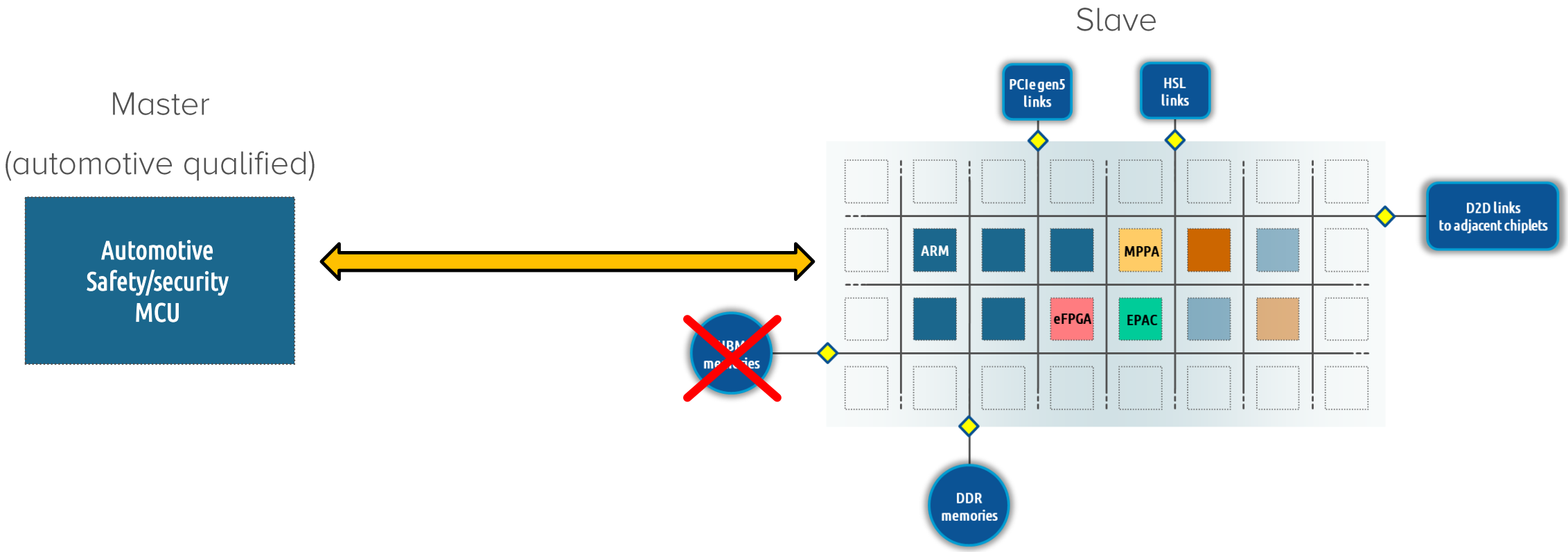
EPI AUTOMOTIVE

- Autonomous driving systems
- Connected mobility
- EPI: A powerful data fusion platform – the automotive embedded HPC platform
- EPI heterogeneous multicore architecture can provide enough performance and low power consumption in parallel

AUTOMOTIVE DOMAIN

- High-performance needed but… within specific domain requirements
  - Reliability
    - Harsh operating conditions due to Electro-Magnetic Interference (EMI), humidity, vibration, etc.
  - Safety
    - Development process subject to functional safety standards
      - Design
      - Verification and validation
  - Security
    - Connectivity
    - Updates

THE EPI APPROACH: EMBEDDED HPC ARCHITECTURE

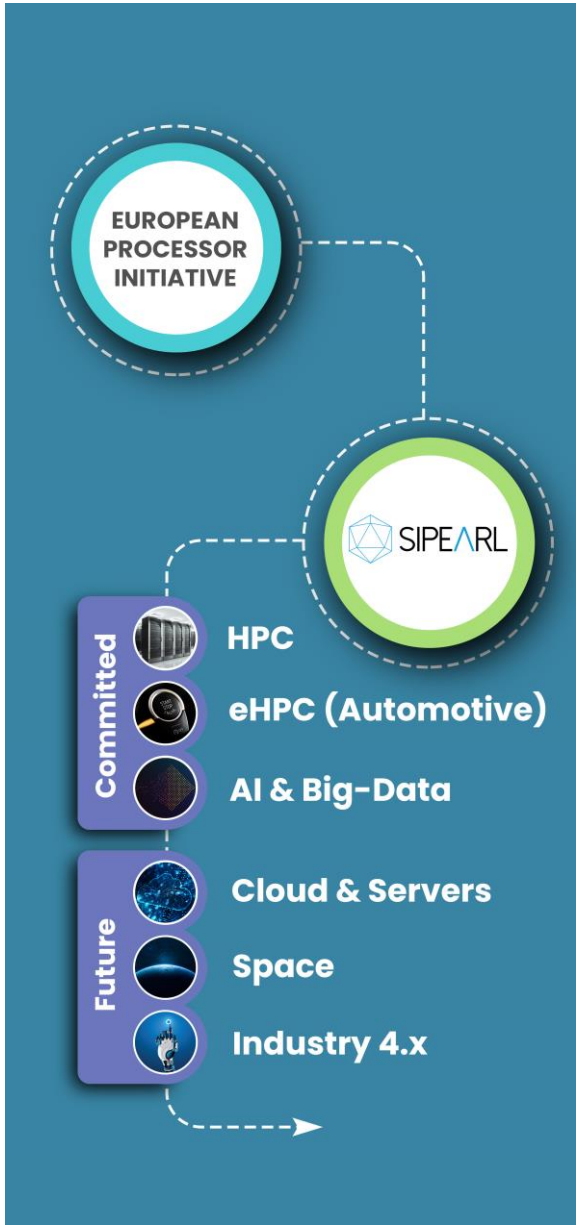


EPI FABLESS COMPANY

EPI FABLESS COMPANY: SIPEARL

- EPI's Fabless company: SIPEARL
  - licence of IPs from the partners
  - develop own IPs around it
  - licence the missing components from the market

  - generate revenue from both the HPC, IA, server and eHPC markets
  - integrate, market, support & sales the chip
  - work on the next generations



WE ACCELERATE ACCELERATORS !!!!

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CONCLUSION

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- HPC is crucial to resolve societal challenges and preserve European competitiveness
- The chip design effort must continue for the EU's sovereignty and competitiveness
- EPI should create a processor ecosystem covering HPC, autonomous connected vehicles, servers and cloud

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