Internet of Things for Automotive Industry: New Trends in Circuits and Systems

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IEEE CASS School “Circuits and Systems for IoT”, Porto Alegre, Brazil, 5-9 Aug. 2019

Outline

Part I

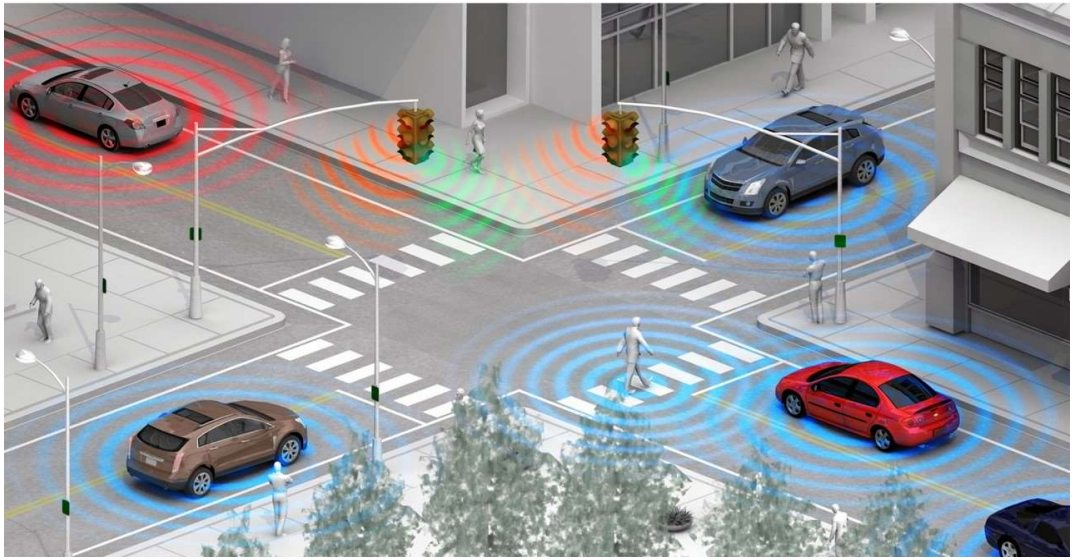
- Societal, economical and technical challenges of autonomous/connected vehicles and intelligent transport systems (ITS)
- CAS for remote sensing (Radar, Lidar) in smart vehicle & ITS
- Sensing technology & CAS for navigation
- CAS for connected cars: V2X receiver in low-cost CMOS

Part II

- CAS for connected cars: cryptographic HW accelerators
- eHPC (embedded High Performance Computing) needs of autonomous and connected cars
- New computing arithmetic (Posits) for DNN acceleration
- Mixed-signal ICs for smart vehicles
- Conclusions

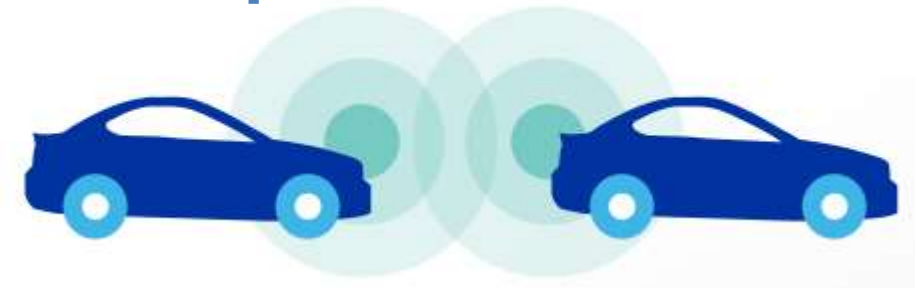
Wireless for context-aware ADAS

Wireless communications & networks (802.11.p @ 5.9 GHz, cellular-V2X)
Vehicle to Vehicle
Vehicle to Infrastructure (Internet of Vehicles)
Vehicle to Human
Vehicle to Network and Social sensors



Complementary wireless systems for ADAS

802.11p-based



- Anti-collisions
- ADAS
- Safety
- Queue warning
- …

Real-time, Critical applications, Short range, Low latency

4GLTE/5G

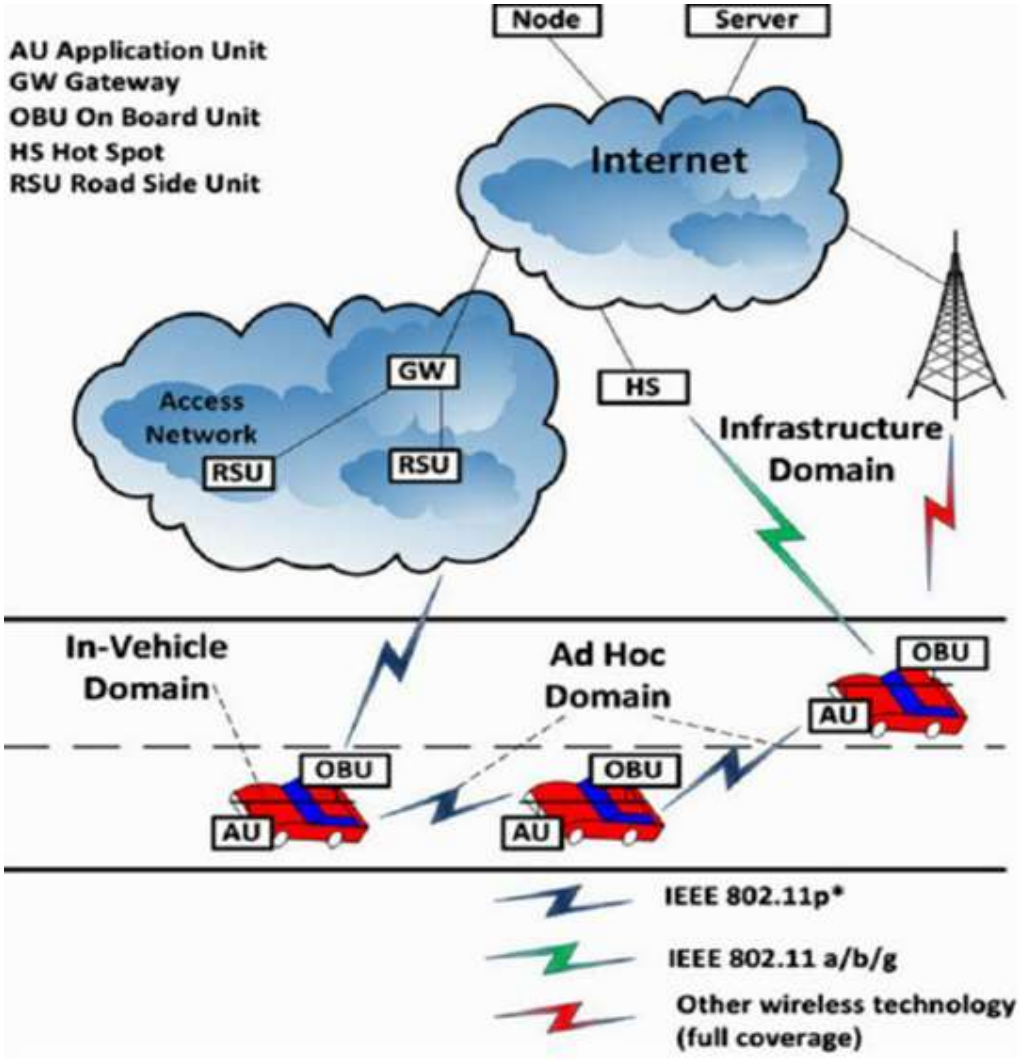
- Infotainments
- Social sensors
- Multimedia
- …

- High data speed
- Network infrastructures
- High capacity
- Long range

IEEE 802.11p overview

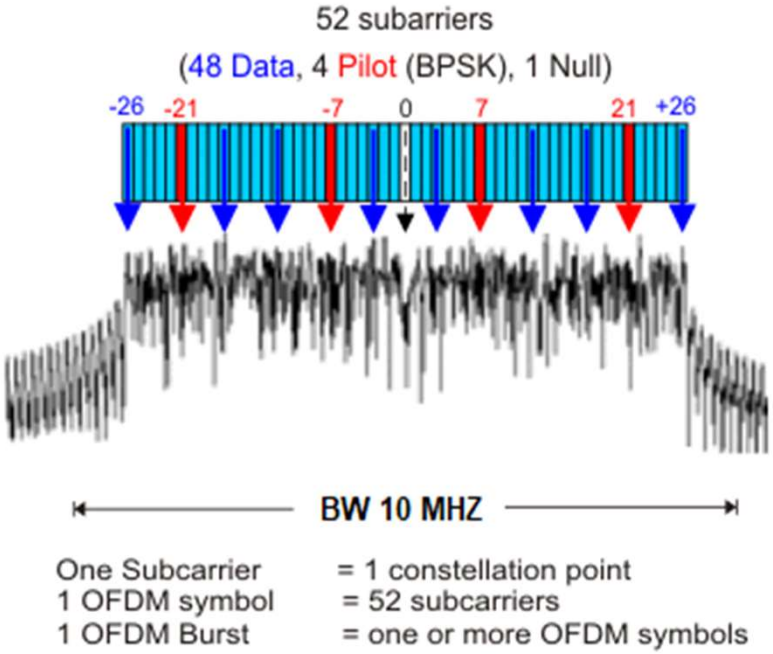
802.11p

- 5.9 GHz BW=75 MHz
- 200 mW Pout
- -90 dBm sensitivity
- 6 Mbps

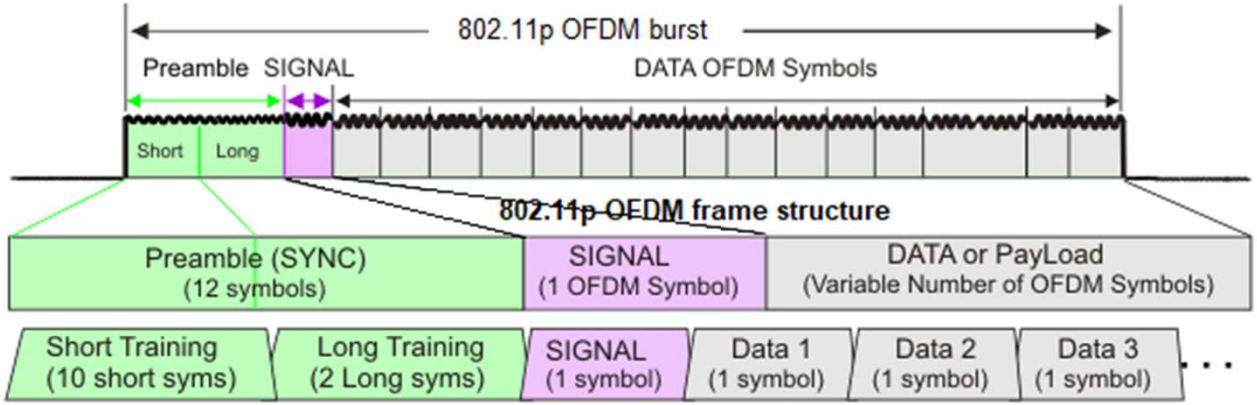


IEEE 802.11p overview

802.11p OFDM PHY Parameters	
BW	**10 MHZ**
Subcarrer Spacing	**156.25 Khz (10 MHZ/64 Pt FFT)**
Information Rate	**3, 4.5, 9, 12, 18, 24, 27 Mbit/s**
Modulation	BPSK, QPSK, 16QAM, 64QAM
Coding Rate	1/2, 2/3, 3/4
Total Subcarriers	52 (Freq Index -26 to +26)
Data Subcarriers	48
Pilot Subcarriers*	4 (-21, -7, +7, +21) *Always BPSK
DC Subcarrier	Null (0 subcarrier)



One Subcarrier = 1 constellation point
1 OFDM symbol = 52 subcarriers
1 OFDM Burst = one or more OFDM symbols



Short Training Seq.
16 us length
12 subcarriers -
every 4th subcarrier
equal Magnitude
signal detect
AGC Diversity Sel
timing sync
coarse freq offset est.

Long Training Seq.
16 us duration
all 52 subcarriers
equal mag/phase
channel estimation
chan equalization
fine freq offset est

SIGNAL symbol
8 us duration
always BPSK
Rate info
Length info

Data symbols
8 us duration
1 IFFT per symbol
52 subcarriers per symbol
48 data, 4 pilots & zero Null sub.
data: same mod fmt per burst
(BPSK,QPSK,16QAM,64QAM)
pilots: BPSK only

IEEE 802.11p overview

Received Signal Power:

$$P_R = P_T \frac{G_R G_T}{L_P L_R} \ (W)$$

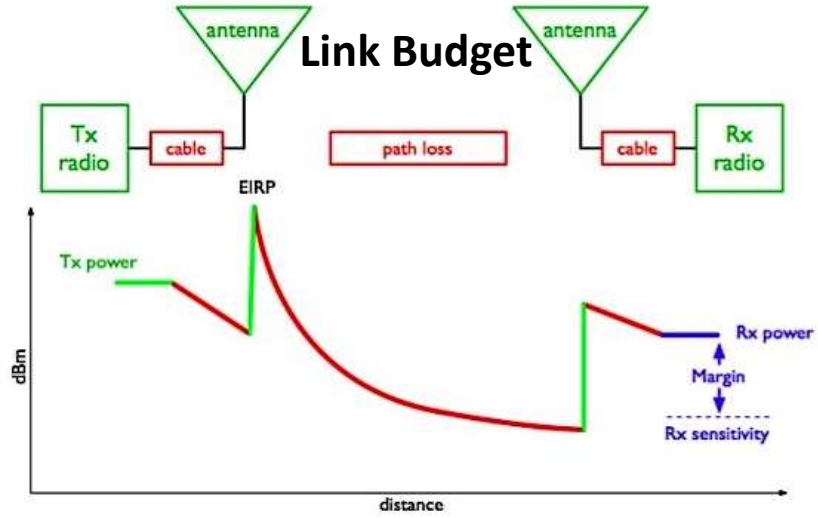
Thermal (Noise) Power:

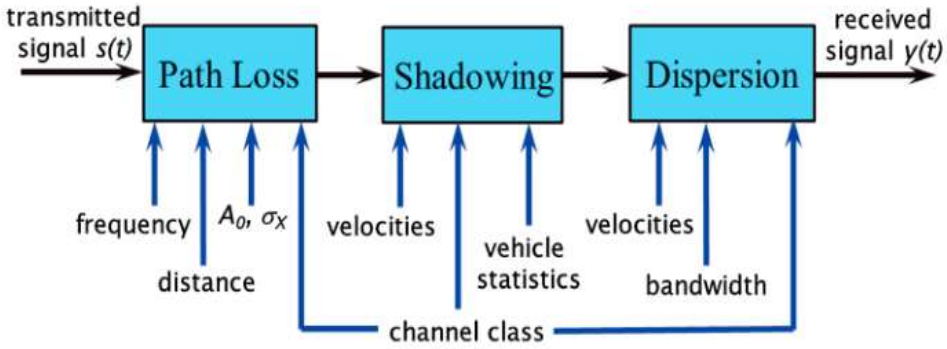
$$P_N = kT_0 \cdot B_w \cdot F$$

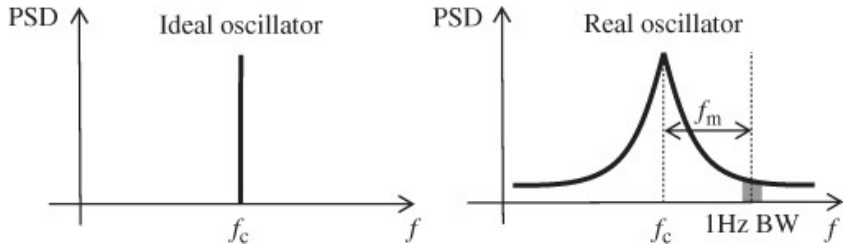
Signal to Noise Ratio:

$$\frac{S}{N} = \frac{P_T \ G_R \ G_T}{k \ T_0 \ B_w \ F \ L_P \ L_R}$$

$$\frac{S}{N} = \left(\frac{E_b}{N_0}\right) \cdot \left(\frac{R_b}{B_w}\right)$$



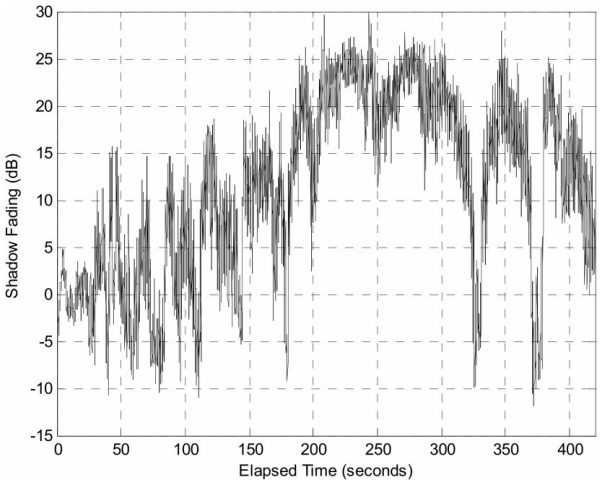


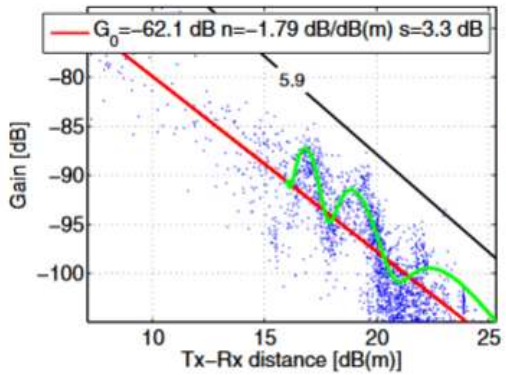


Transceiver and channel model

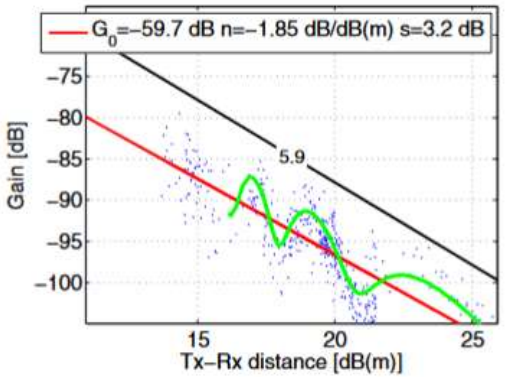
$$PL\,(dB) = PL\,(d_0) + 10\,n\,log_{10}\left(\frac{d}{d_0}\right) + X_\sigma$$

Environment	Power law		
	$PL\,(d_0)\ (dB)$	n	$\sigma(dB)$
Rural	-61.1	-1.79	3.3
Highway	-59.7	-1.85	3.2
Urban	-68.5	-1.61	3.4
Suburban	-65.0	-1.57	4.2

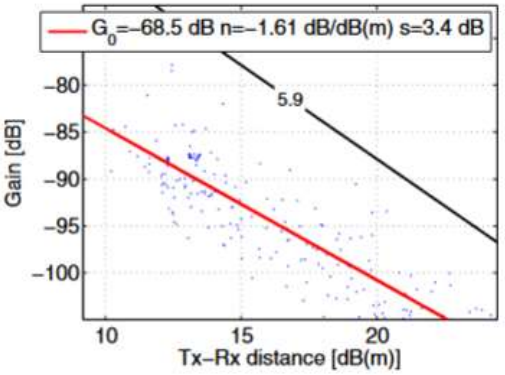




(a) Rural

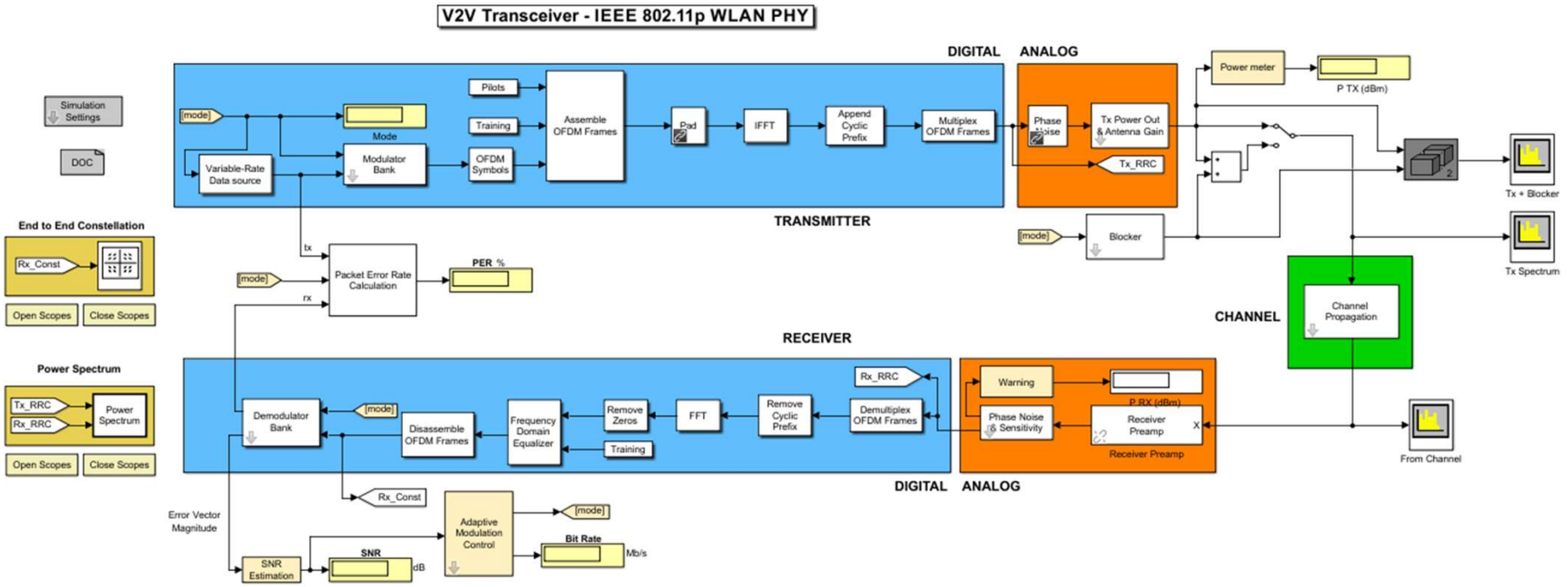


(b) Highway



(c) Urban

Transceiver and channel model



COLOR LEGEND:

Blue: Digital system blocks

Orange: Analog system/signals

Light Orange: Control system/signals

Yellow: Display and graphics

Green: Radio Channel and documentation

Grey: Settings

Transceiver and channel model

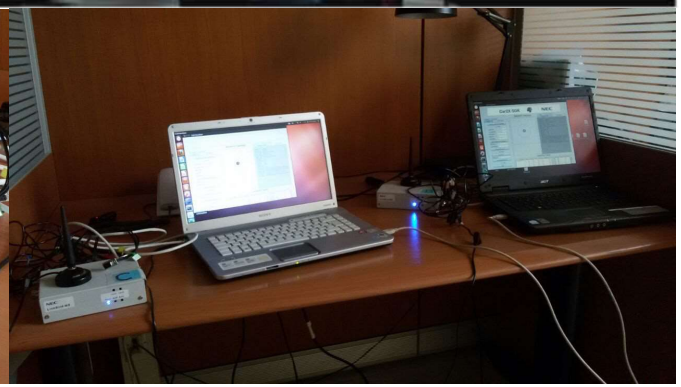
Experimental measurements:

- **scenarios**: highway, suburban and urban canyon
- **Line of sight condition**: LOS, NLOS

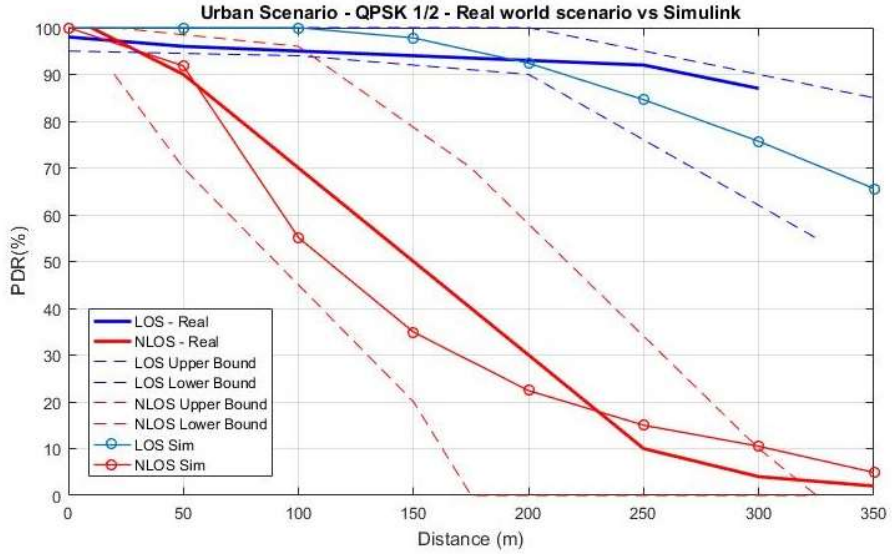
Results:

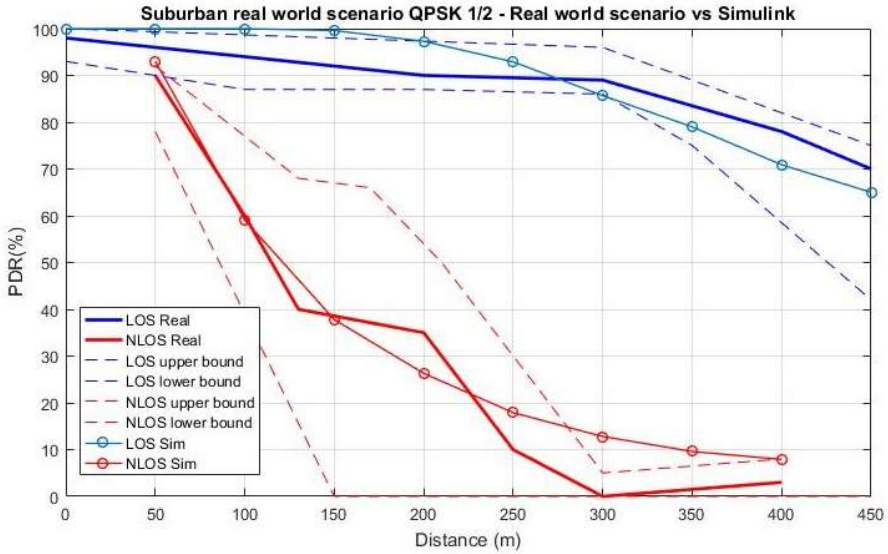
- **PDR(%) vs distance**

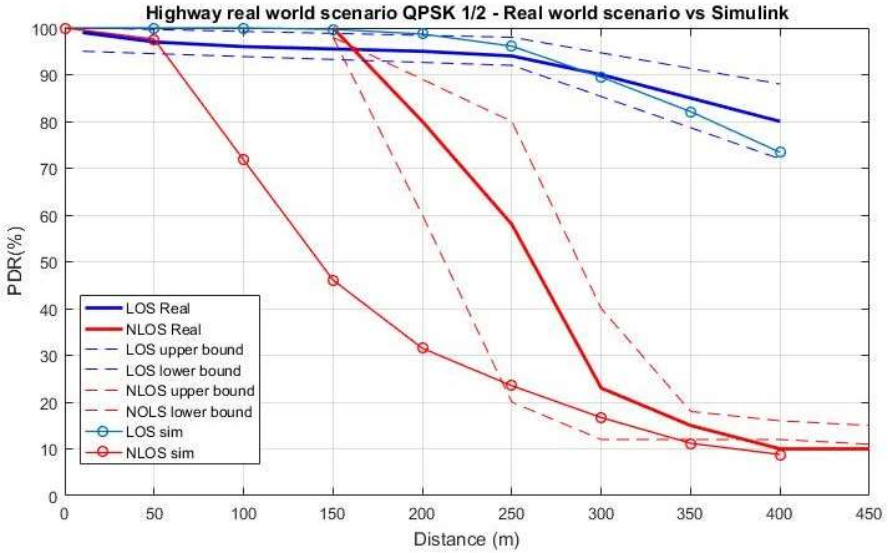
Parameter	802.11p
Channel	180
Center frequency (MHz)	5900
Bandwidth (MHz)	10
Data rate (Mbps)	6
Tx power (setting, dBm)	18
Tx power (measured, dBm)	10
Antenna gain (dBi)	5
Beacon frequency (Hz)	10
Beacon size (Byte)	36

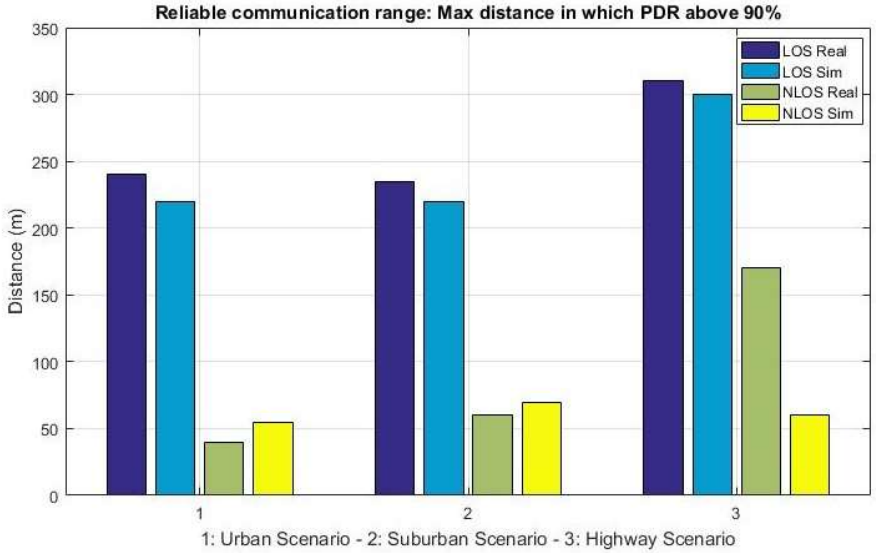


Model vs. real world comparison

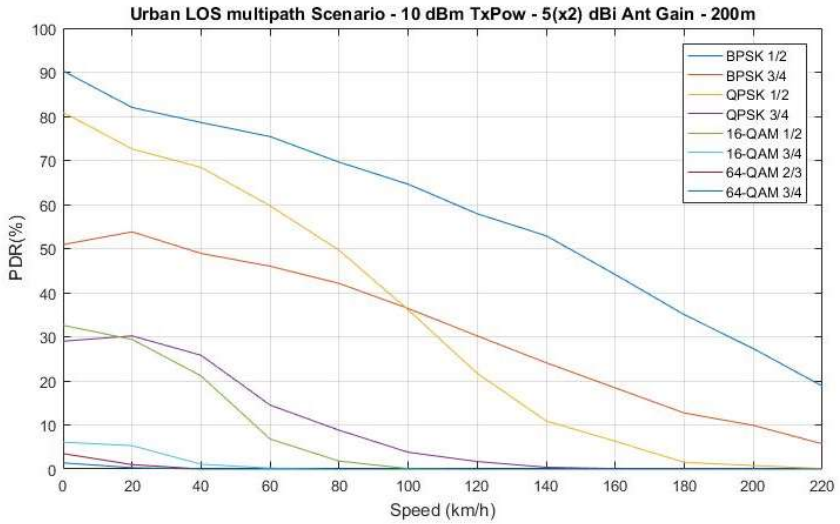


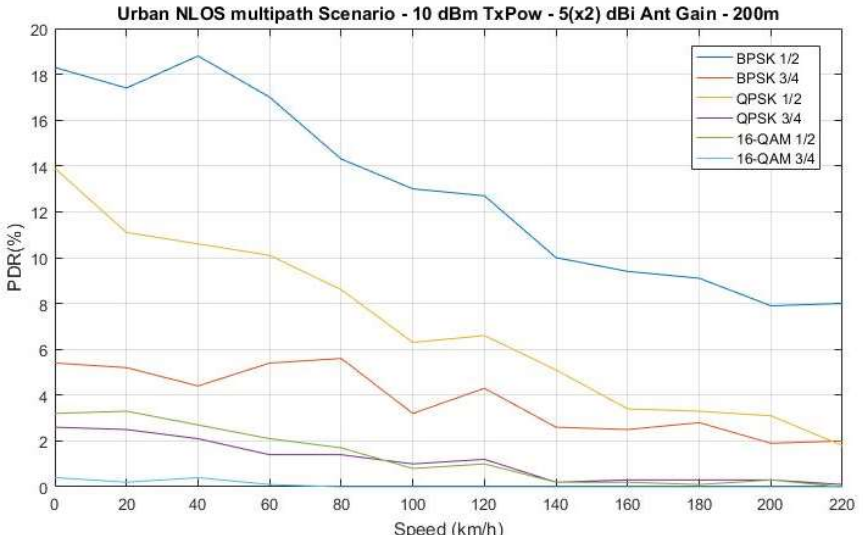


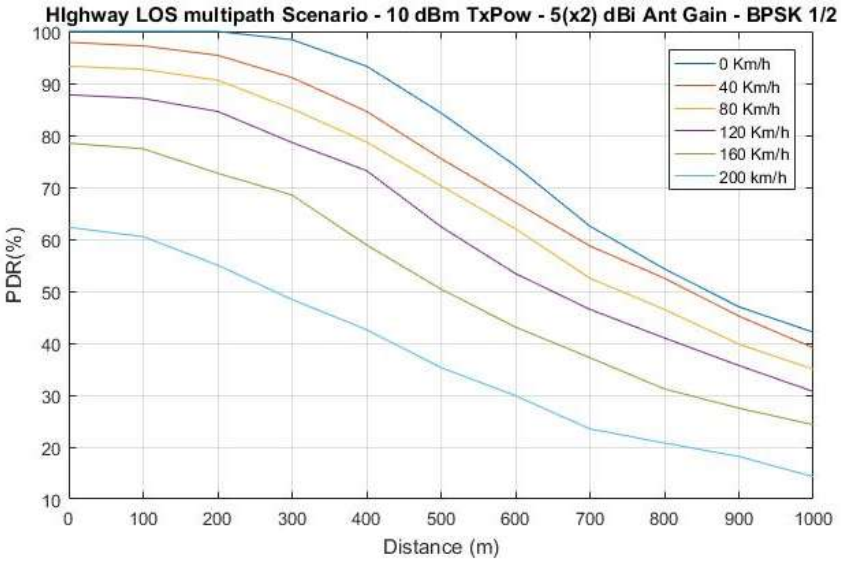


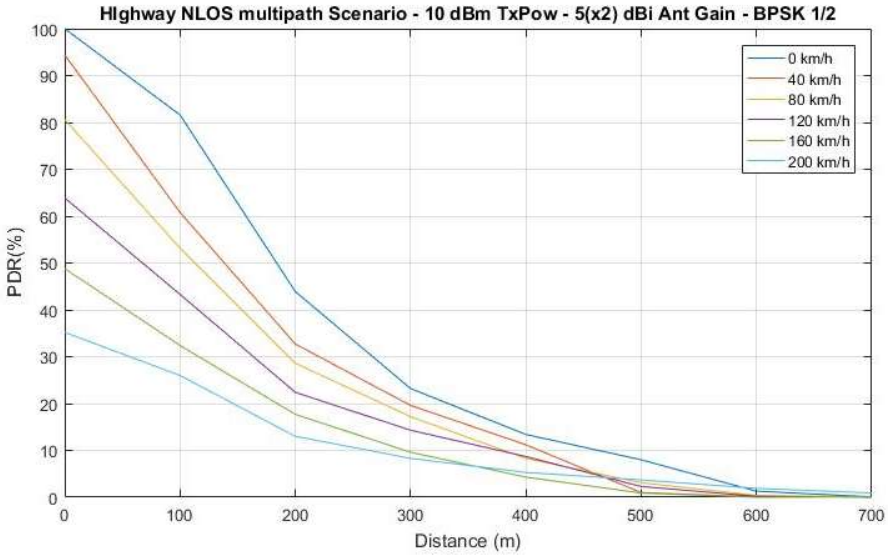


Impact of distance and speed



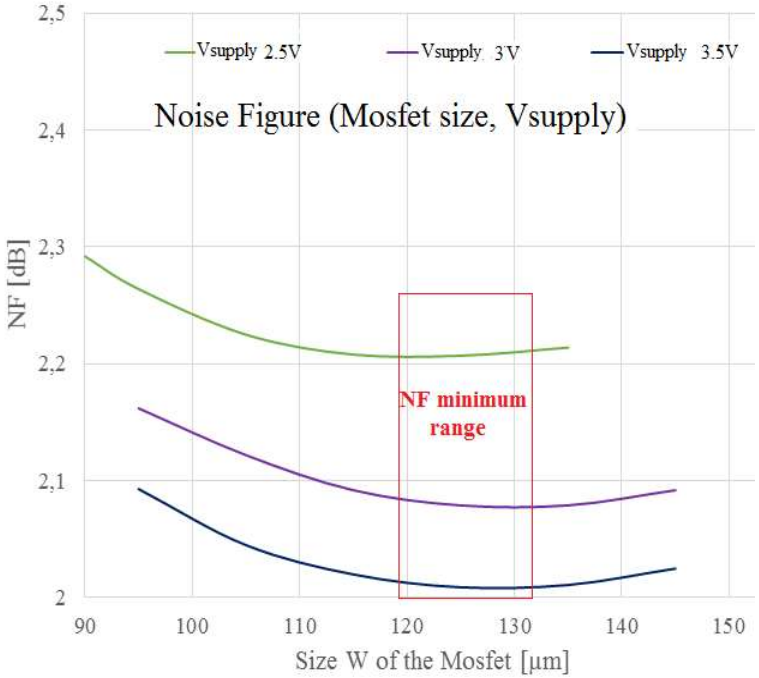


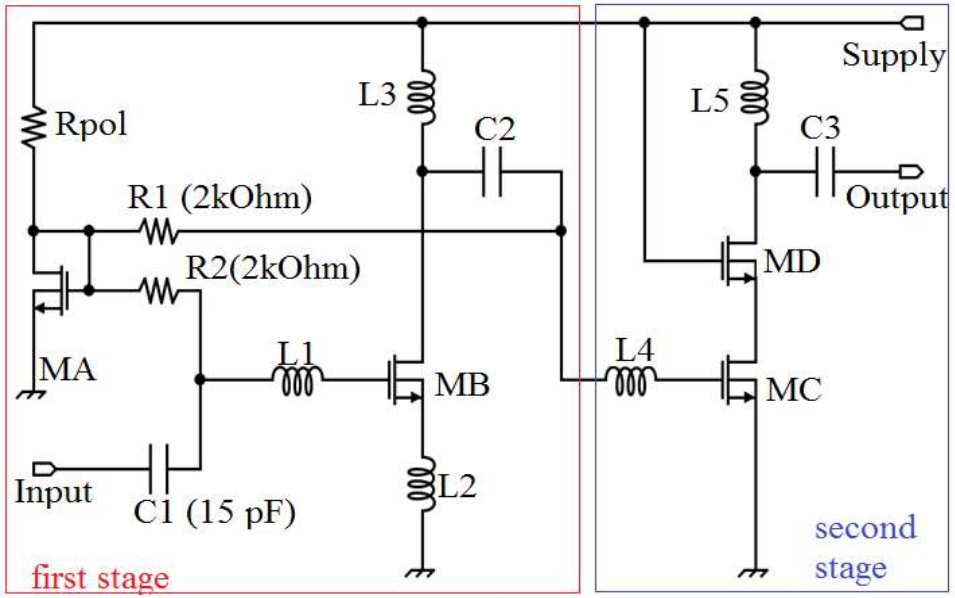




IEEE 802.11p receiver in low-cost CMOS

NF 2.43 dB, 30 mW, G_T 32 dB, 1dBOP 0.8 dBm

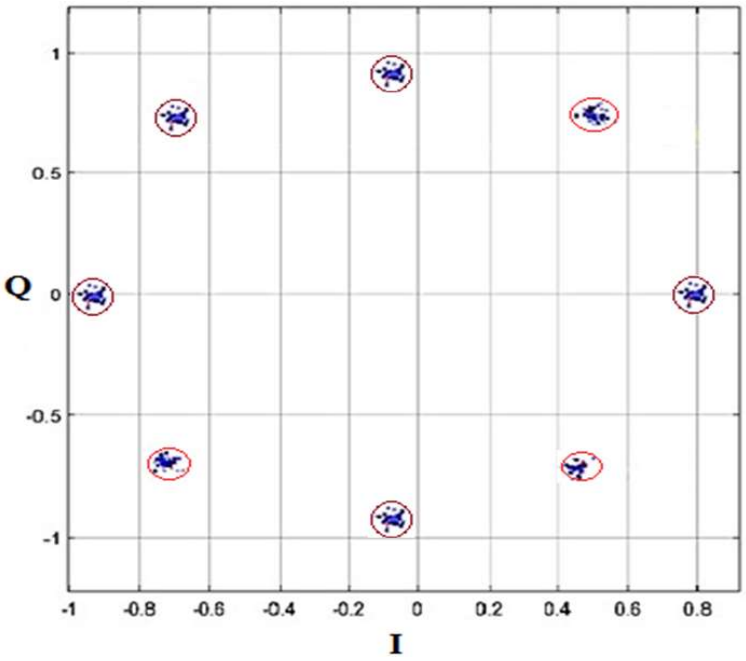


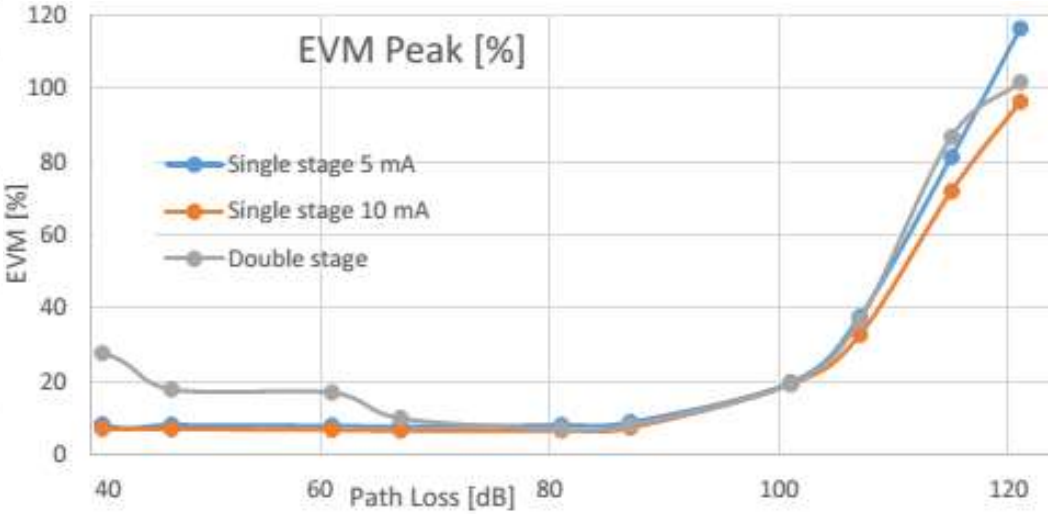


Technology	Price (€) / mm²
0.35µ CMOS	800
0.35µ SiGe-BiCMOS	880
0.18µ CMOS aC18	1100
SGB25V 0.25µ SiGe	2500
SG25H3 0.25µ SiGe	3800
130nm SiGe BiCMOS9MW	3100
55nm SiGe BiCMOS055	7900

IEEE 802.11p receiver in CMOS

Path Loss: 40 dB@ 0.5m, 100 dB@ 500 m, 120 dB@5 km





8-PSK received constellation and Error Vector Magnitude @ 300 meters (200 mW Pout)

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Automotive cybersecurity: a real challenge

Exposure to cyber attacks:

- Vehicle hack
- Data tampering
- Denial of Service

SW computing of crypto functions

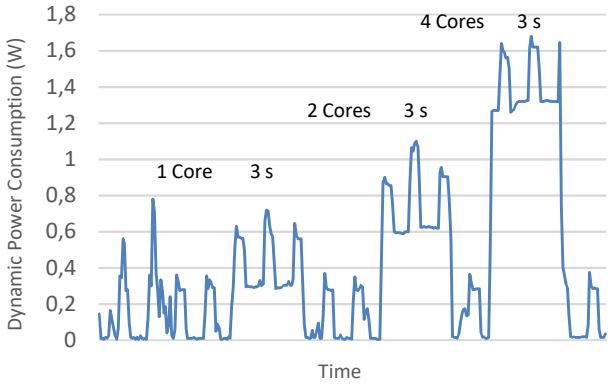
Too slow, too power consumption

Performances data for AES-ECB-256, SHA-2 256 and ECDSA SW implementation (Open SSL library on 4-core 64b Cortex-A53 Broadcom MPSoC)

Number of core	Exec. time (s)	D (Mb)	TH (Mbps)	P (mW)	E (mJ/Mb)
1	3	917.4	305.80	300	0.98
2	3	1812.8	604.27	600	0.99
4	3	3628	1209.33	1300	1.07

Number of core	Exec. time (s)	D (Mb)	TH (Mbps)	P (mW)	E (mJ/Mb)
1	3	337.9	113,01	310	2.74
2	3	664.9	221,63	650	2.93
4	3	1213.9	404,63	1380	3.14

Number of core	Exec. time (s)	D (Op)	TH (Op/s)	P (mW)	E (mJ/Op)
1	10	282.4	28.24	310	10.98
2	10	560	56	620	11.07
4	10	1085	108.5	1330	12.26



2 orders of magnitude in speed and 1 order of magnitude in power improvement with HW acceleration

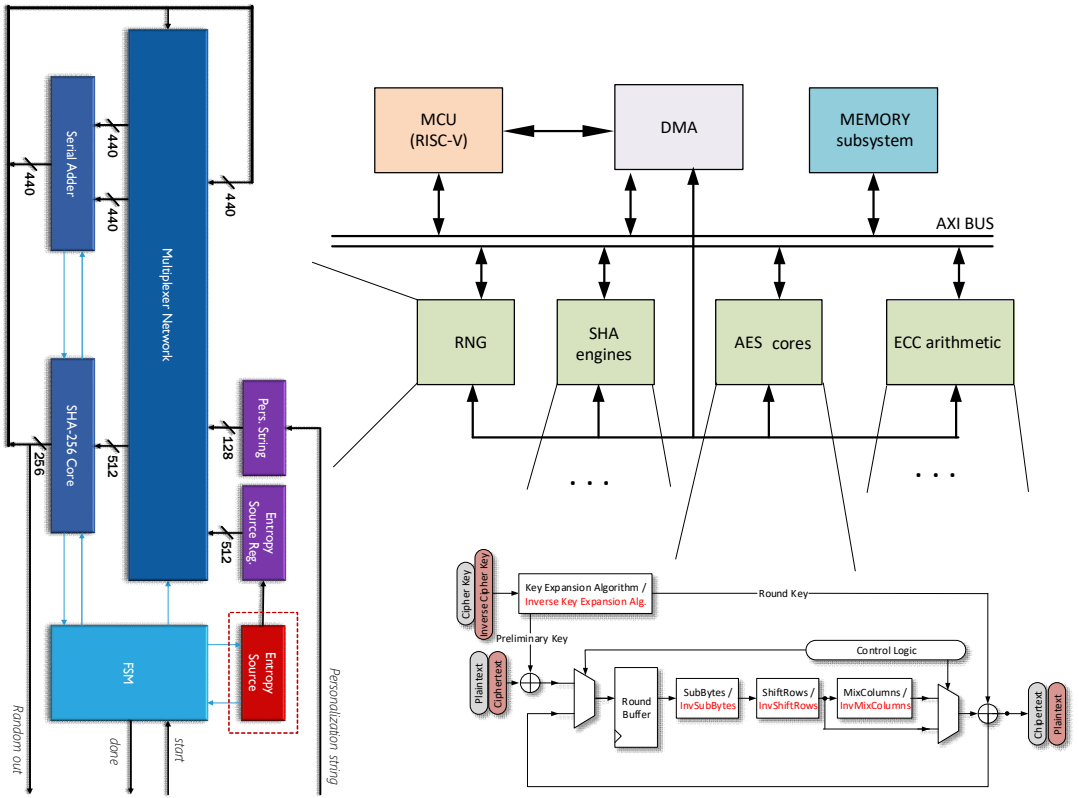
HW acceleration for cryptography

- Main idea: accelerate the intensive operations of cryptographic standards in order to meet the high-performance requirements of the automotive world in terms of latency
- Standards can be easily implemented in SW but this could not be enough in terms of performance for the automotive world
- HW solutions may lack flexibility: a cryptographic co-processor is the best trade off between performance, flexibility and reusability when compared to ISE and dedicated crypto processors
- General purpose code running on the GPP while sensitive operations are accelerated in HW
- Post- quantum security needs long key/hash e.g. AES256, SHA512
- ECC-based crypto not suited for post-quantum crypto

HW-based Root of trust

Examples from the H2020 European Processor Initiative:

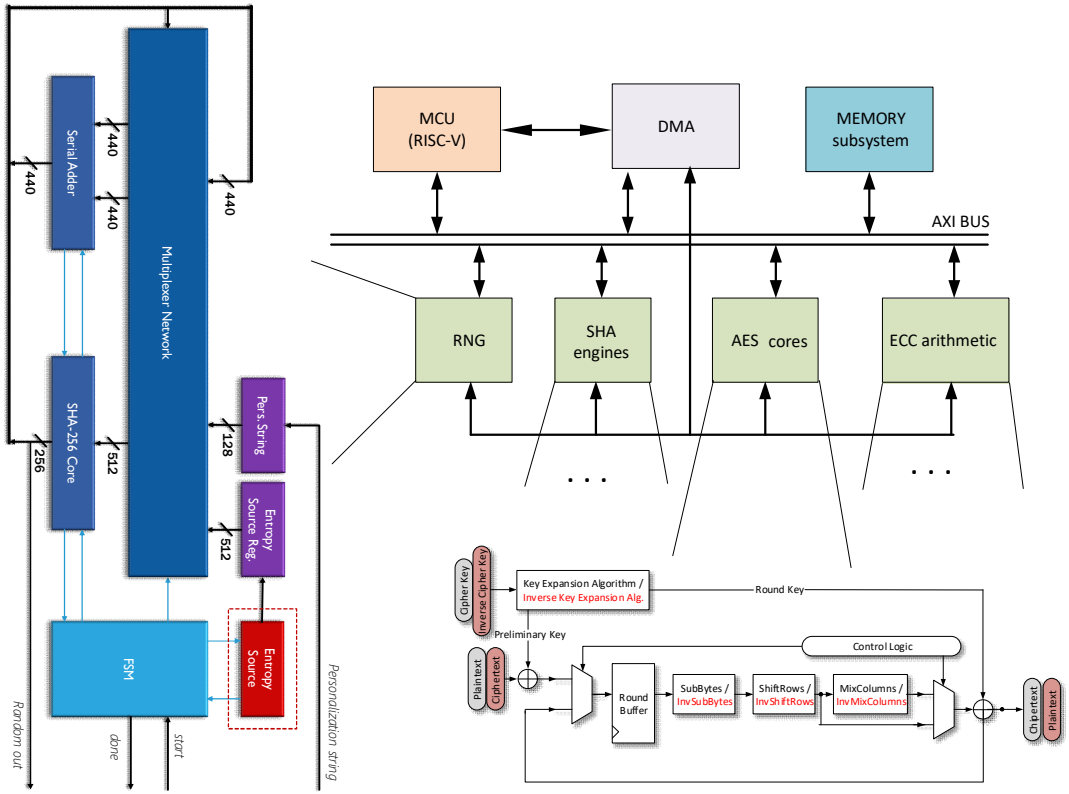
- Definition of the HW and SW architecture of the Secure Element (SE) that will be the root of a trusted chain to avoid that malicious SW runs on EPI multi-cores
- The multi-core on-chip system divided in secure zones (quadrants) each with a secure MCU
- Focus on a secure boot sequence and on the relation between secure elements and power manager



HW-based Root of trust

Examples from the H2020 European Processor Initiative:

- SE trustiness by proper HW/SW partitioning including:
  - OTP/e-fuse integration,
  - RNG for seed generation,
  - acceleration for advanced and complex crypto functions
  - programmability (e.g. RISC-V core plus DMA capability)



Configurable HW crypto IPs

- Open SSL SW benchmark results (encryption throughput) on 4-core Arm64 V8.0 (e.g. that of S32NXP):
  <1 Gbps (AES ECB 256), 400 Mbps (SHA2-256), 100 signature/verification per second with ECDSA NIST-P521 for a power cost in the order of Watt
- Orders of magnitude improvement in speed (x10) and power-efficiency (x100) with EPI HW crypto acc
- Up to 300 Gbps AES XTS encryption/decryption in 7 nm
- Design of accelerator IPs for embedded cybersecurity
  - AES 128/256 with configurable modes (ECB, CBC, CTR, OFB, CFB, CCM, CMAC, GCM, XTS) compliant with NIST SP800-38A/38B/38C/38D/38E
  - SHA2 and SHA3, 256 and 512 bits compliant with FIPS-180/FIPS-202
  - Configurable ECC-based public key accelerator modes (ECDSA, ECIES, ECDH,..) and curves (NIST-P 256, 521) compliant with FIPS 186-3,…
  - TRNG and CSPRNG verified vs NIST SP800-90B, SP800-22

More than just an HW IP core

Secure management policy of keys/certificates embedded in HW enabling advanced SW services

- Enforce good practice in sensitive data management at HW level
- Provide mechanisms at HW level to enforce usage of cryptographic algorithm and associated keys (Specification of a key management interface and internal secure storage
- Provide necessary robustness to detect and limit impact of SW bugs and attacks by enforcing strict usage rules of the crypto processor interface
  - need to know, data separation per usage, and state machine approaches
- Help to architecture the SW for high security and safety, with the concept of SW islands: simple and restricted functionality, by isolating the different operations when manipulating sensitive data; limiting access to associated sensitive data to each part
- Ease the certification of the HW/SW by using concept of independent island when dealing with the configuration of the crypto processor (locking mechanism, CPU privilege restrictions, …)
- Crypto-processor configuration and operation management

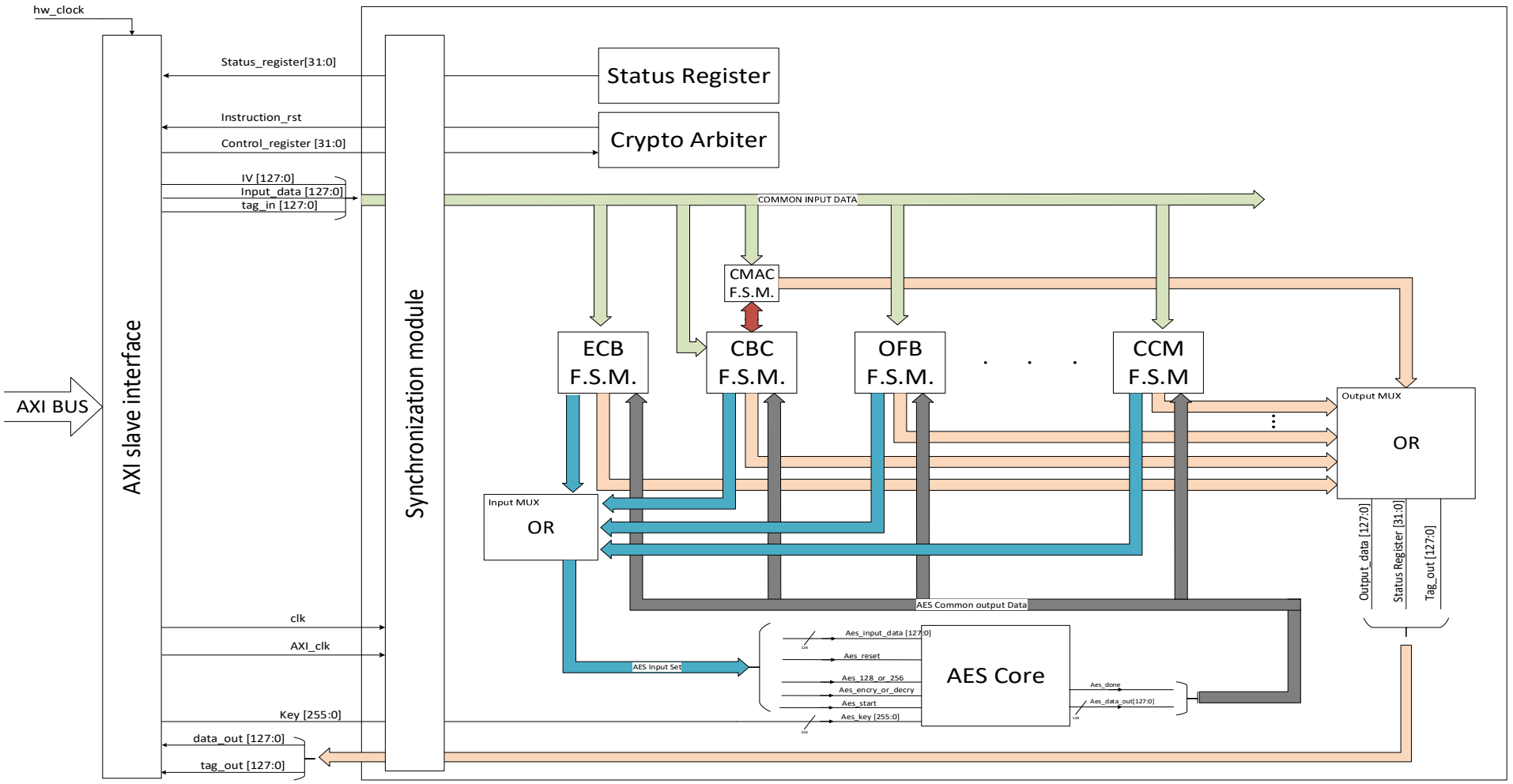
Configurable coprocessor for HW car security

- Easy-to-integrate solution for automotive SoCs, where fast and context-aware security approaches are required
- Flexible and adaptable interface to a GPP
- AES (Advanced Encryption Standard) based Block cipher Modes to guarantee confidentiality, integrity… with 128/256-bit key sizes
- Compliant with US NIST standards: ECB (ElectronicCodeBook), CBC (Chiper Block Chaining), CFB (ChiperFeedback), OFB (Output Feedback), CTR (Counter mode encryption), CMAC (Chiper-based Message Authentication Code), CCM (Chiper block Chaining Message authentication code), GCM (Galois Counter Mode)
- High-Flexibility: Conditional instance of HW modes to minimize area
- Support core security functions needed for diffused security standard such as SHE, MACSec or WAVE

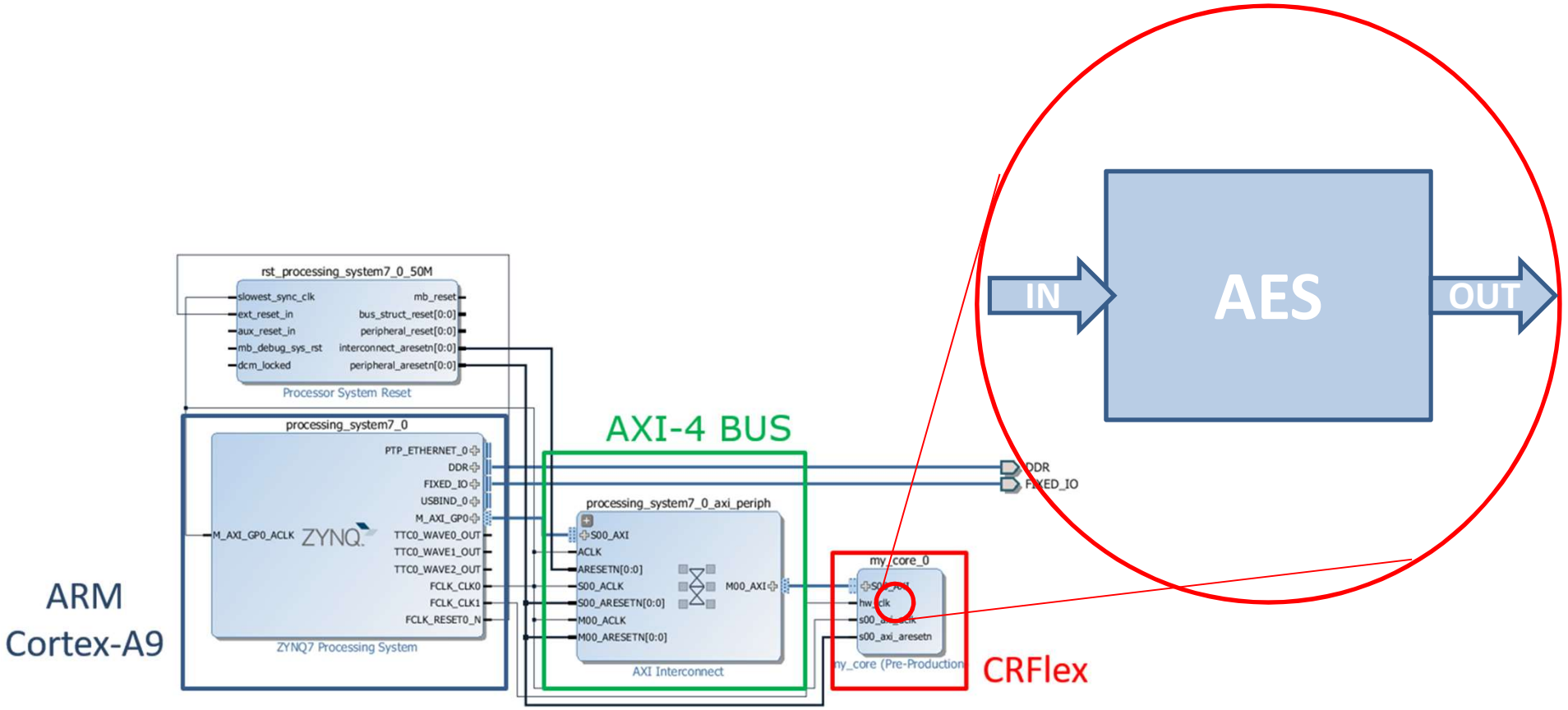
Why multiple modes?

Cipher Mode	Confidentiality	Integrity	Authenticity
ECB	✓	✗	✗
CBC	✓	✗	✗
OFB	✓	✗	✗
CFB	✓	✗	✗
CTR	✓	✗	✗
CMAC	✗	✓	✗
GCM	✓	✓	✓
CCM	✓	✓	✓
…			

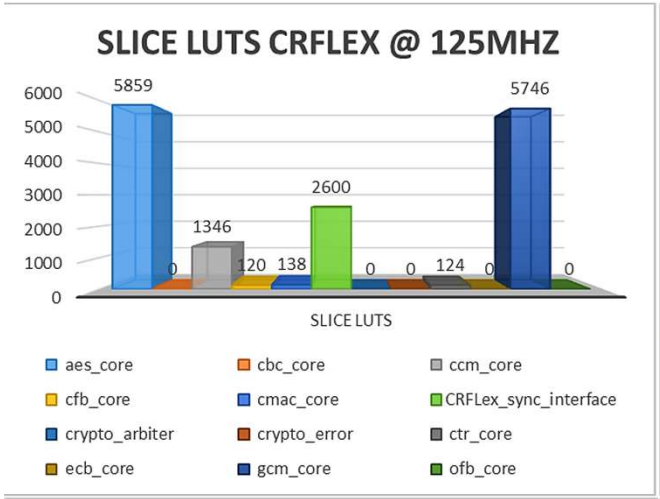
Cybersecurity IP core architecture

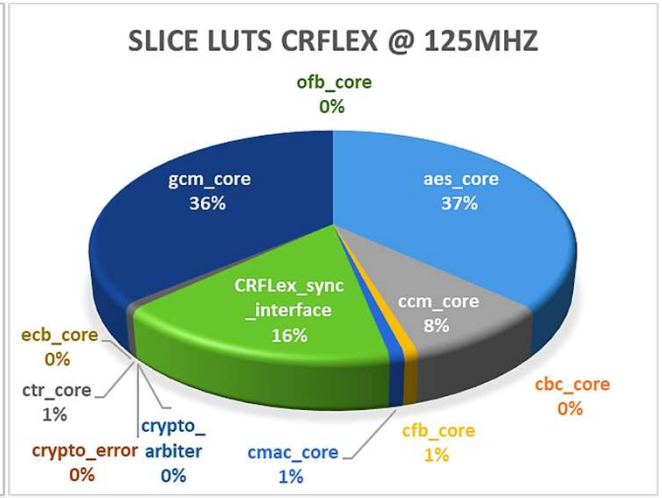


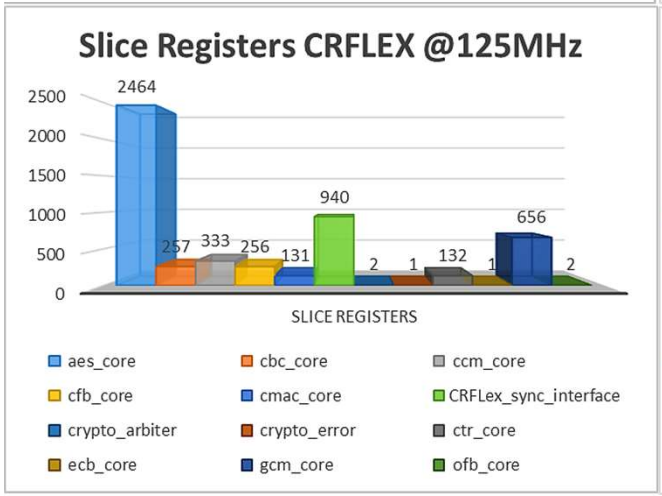
Cybersecurity HW/SW architecture

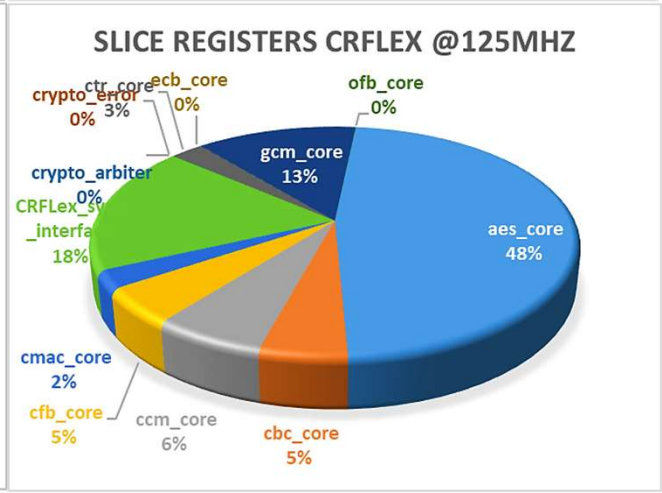


Complexity Results (ZynQ 7000 FPGA resources)









AES core is the most complex module

GCM mode combinational logic count is the highest due to the heavy finite field multiplier

CCM is smaller but potentially slower than GCM, due to a double encryption needed

Synchronization logic is considerable due to the number of CDC in the HW/SW interface

Outline

Part I

- Societal, economical and technical challenges of autonomous/connected vehicles and intelligent transport systems (ITS)
- CAS for remote sensing (Radar, Lidar) in smart vehicle & ITS
- Sensing technology & CAS for navigation
- CAS for connected cars: V2X receiver in low-cost CMOS

Part II

- CAS for connected cars: cryptographic HW accelerators
- eHPC (embedded High Performance Computing) needs of autonomous and connected cars
- New computing arithmetic (Posits) for DNN acceleration
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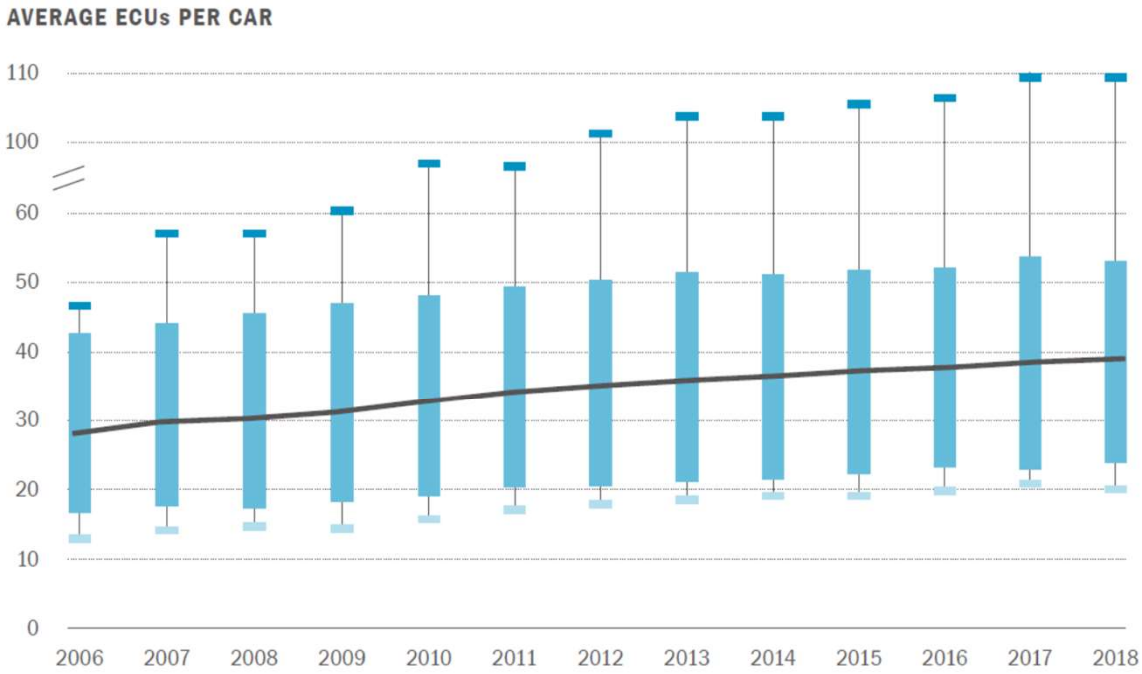
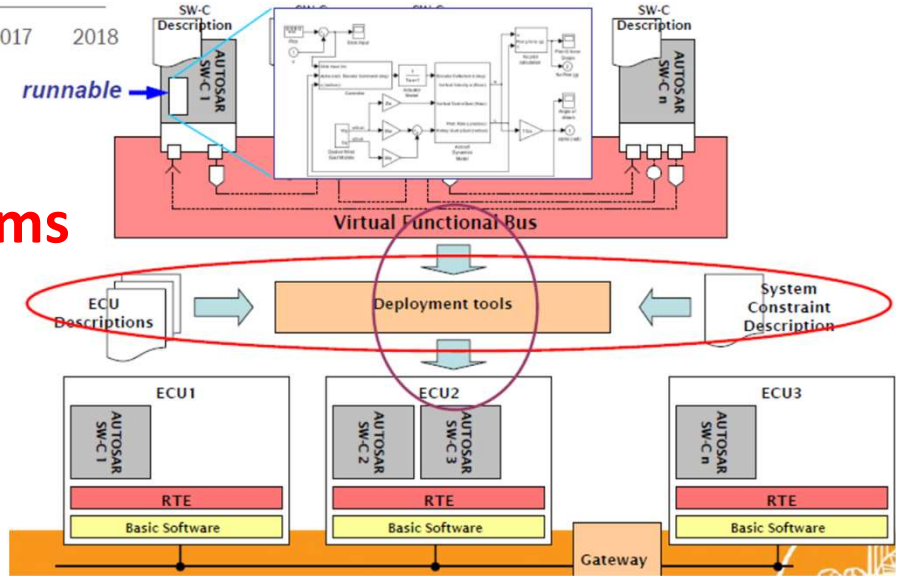
- Conclusions

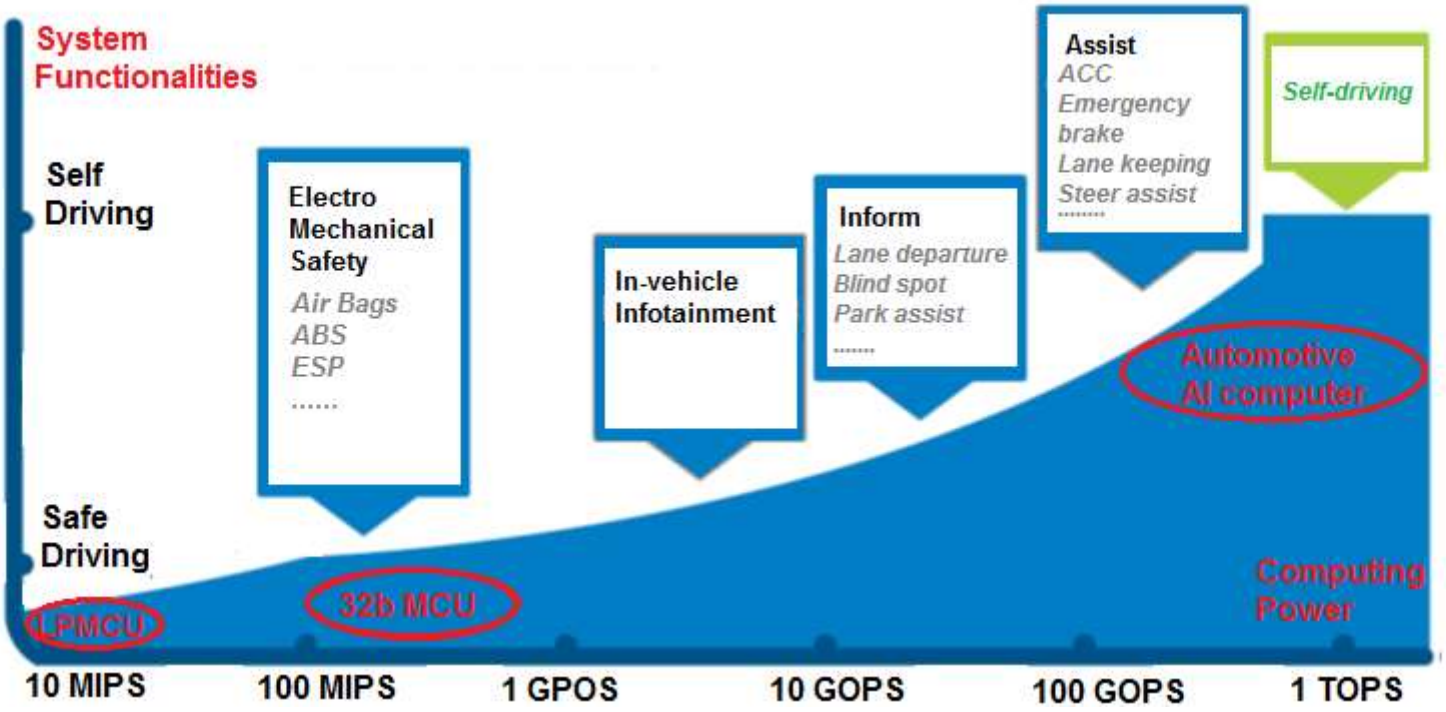
ECU and sensor DSP computing



HW-SW co-design & embedded systems for computing intensive applications

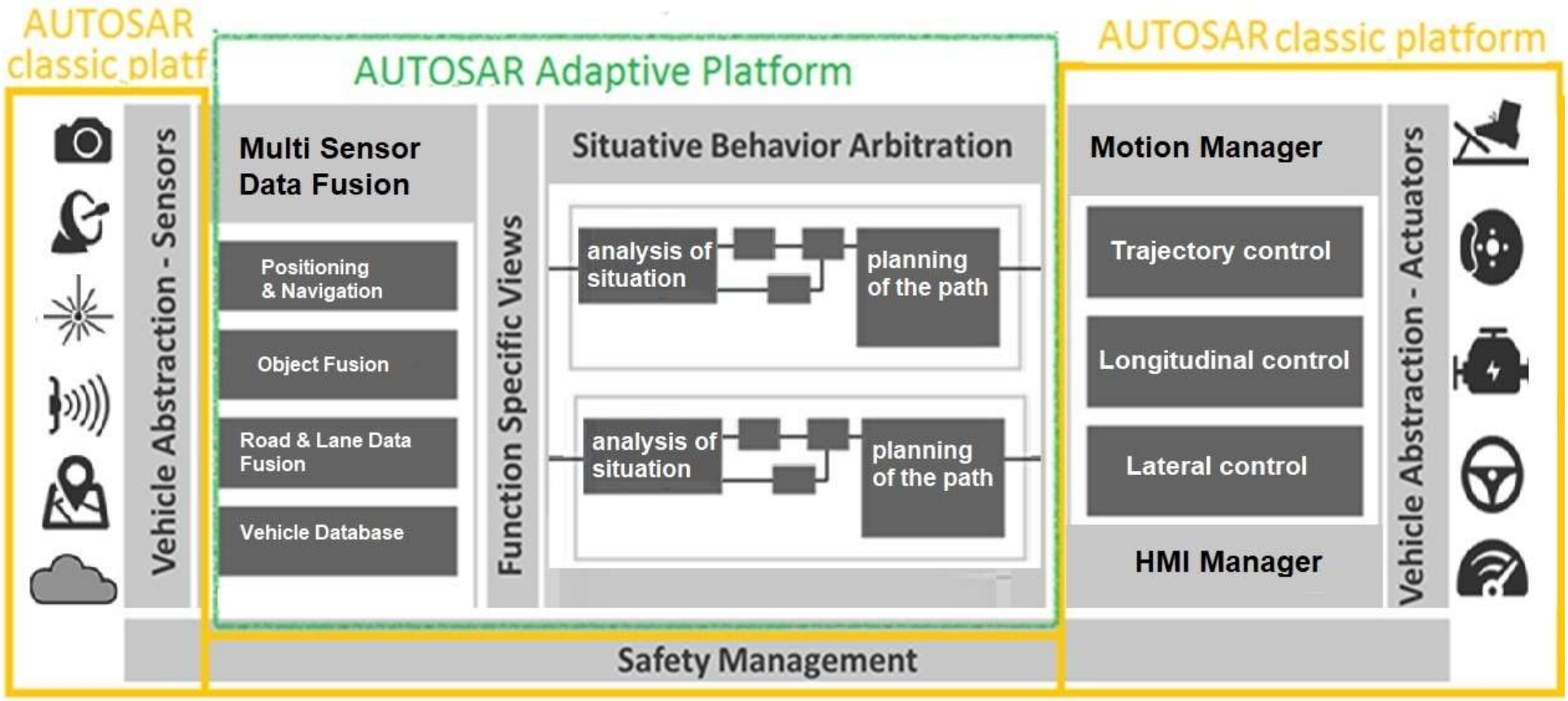


ECU and sensor DSP computing



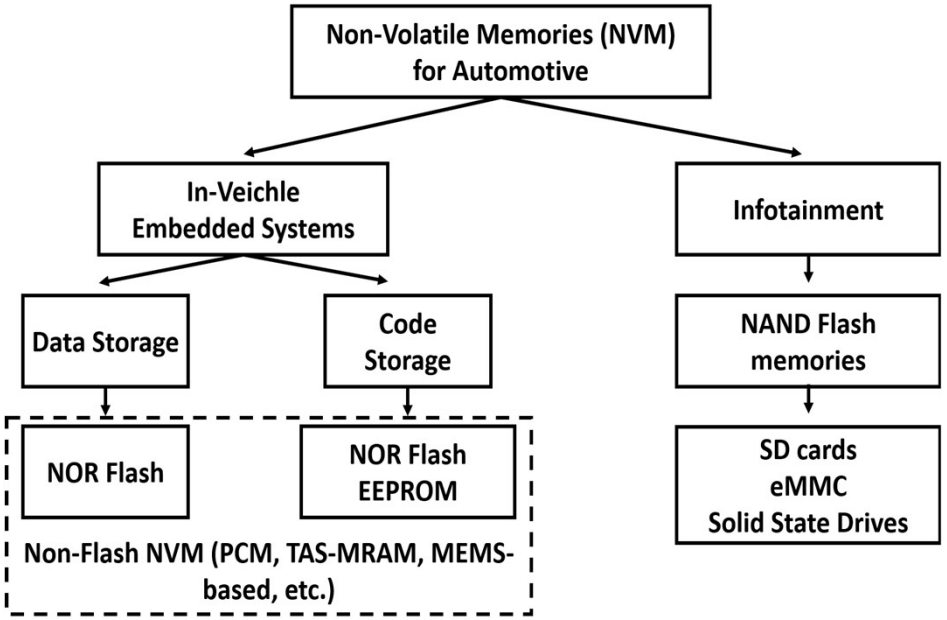
State-of-art is 32b MCU with high-SIL Increase in system but functionalities towards autonomous driving will require multi-core platforms with up to TOPS capability

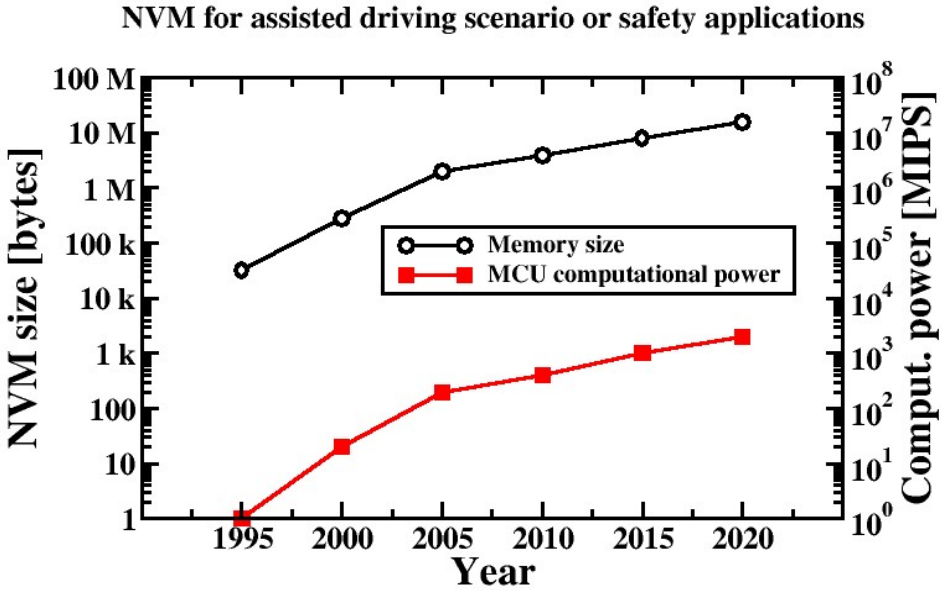
ECU and AUTOSAR



State-of-art is 32b MCU with high-SIL Increase in system but functionalities towards autonomous driving will require multi-core platforms with up to TOPS capability

Memory needs and trends for assisted driving



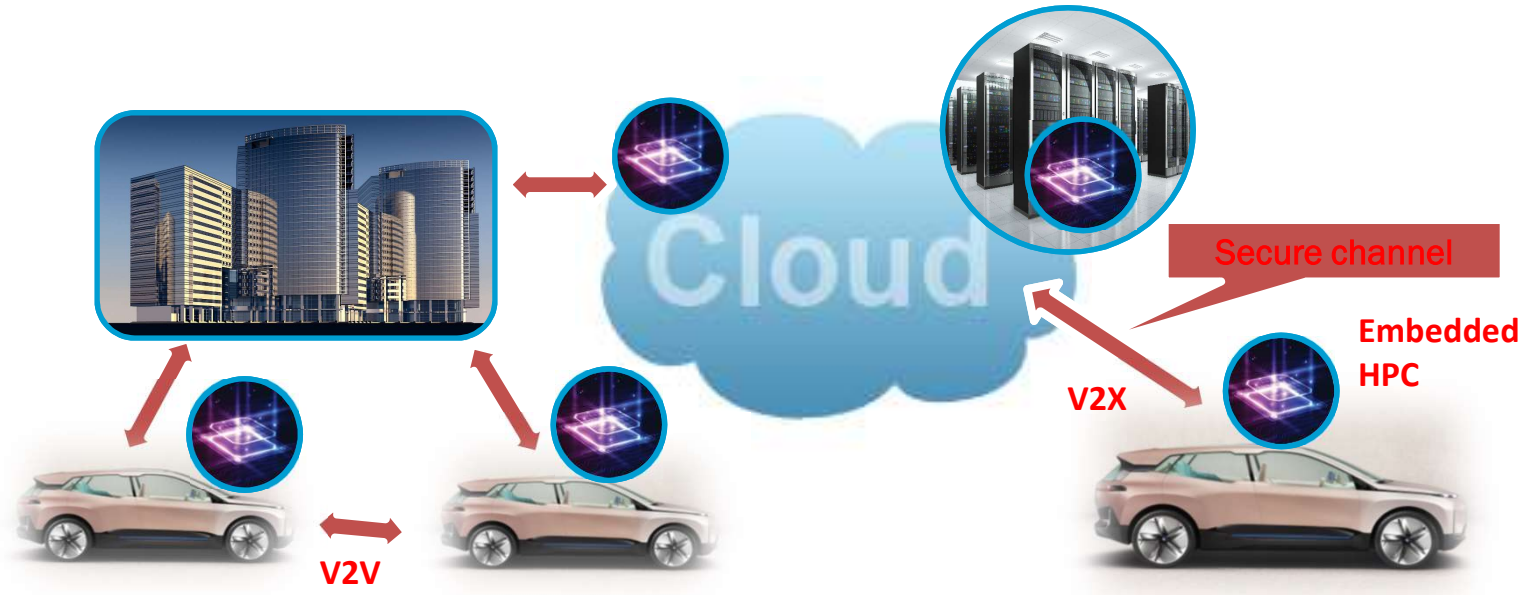


Parameter	EEPROM	NOR Flash Code Storage	NOR Flash Data Storage	PCM	MEMS-based	RRAM CBRAM	TAS-MRAM
Endurance	500k	10k – 100k	500k – 1M	>1M	>1M	100k	>1M
Data Retention	>10 yrs/125 °C	10 yrs/125 °C	>10 yrs/125 °C	10 yrs/85 °C	>10 yrs/125°C	10 yrs/85 °C	>10 yrs/125 °C
Power consumption	Low	Low	Low	High (Write)	Low	Low	High
Read Latency	20 – 50 ns	< 20 ns	< 20 ns	> 20 ns	> 100 ns	> 20 ns	50 – 100 ns
Cost per bit	Medium/High	Medium	Medium	Low	High	Low	High

Memory needs for autonomous cars

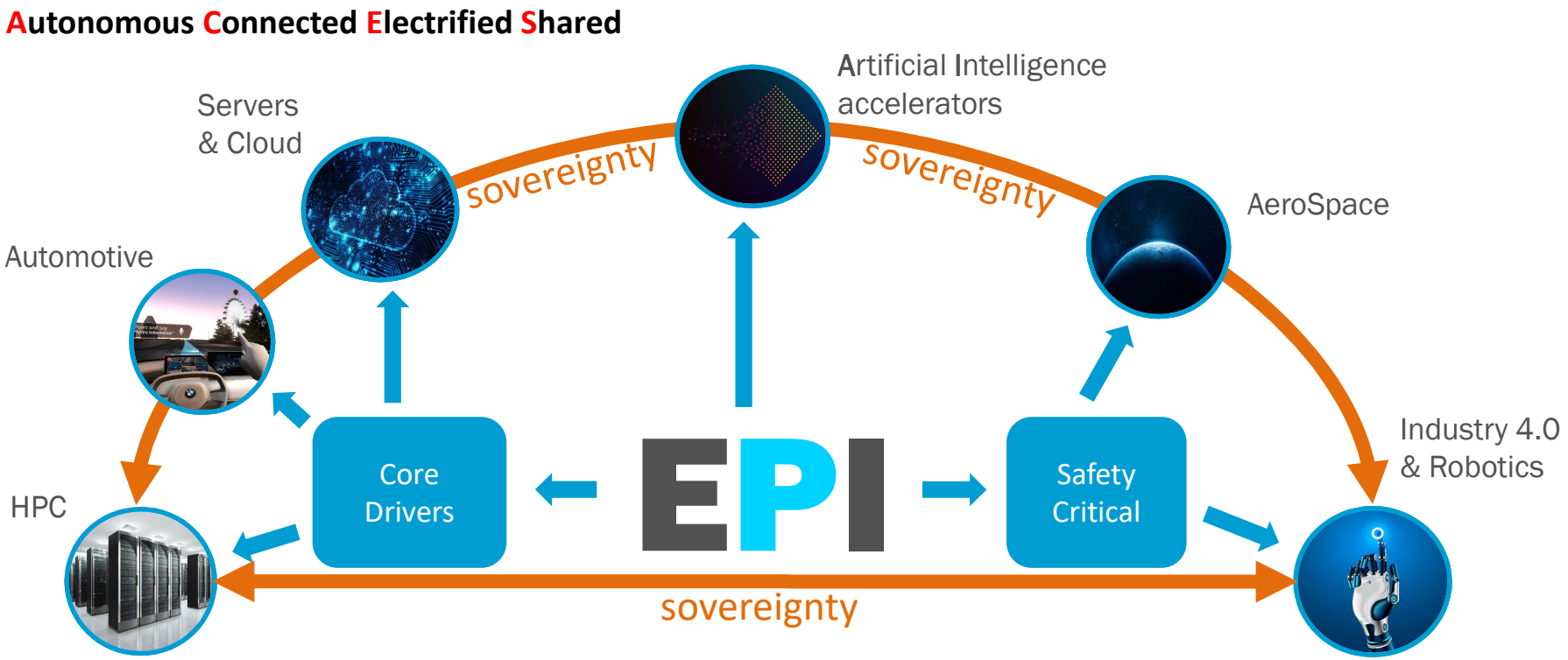
European Processor Initiative

Enabling **TE**chnologies for sm**A**rt vehicles and **M**obility (EPI 120 M€ project in 5 years)

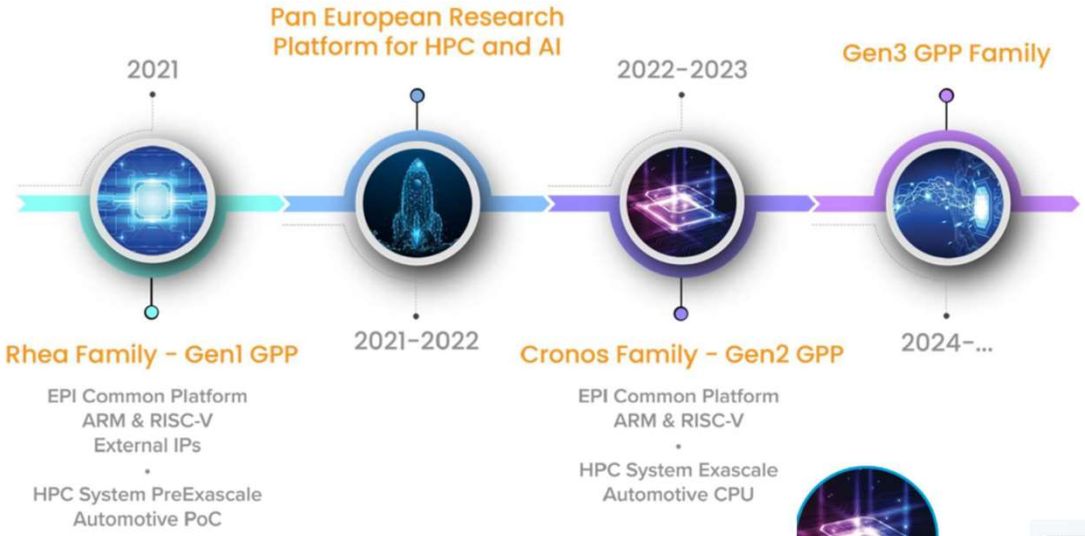


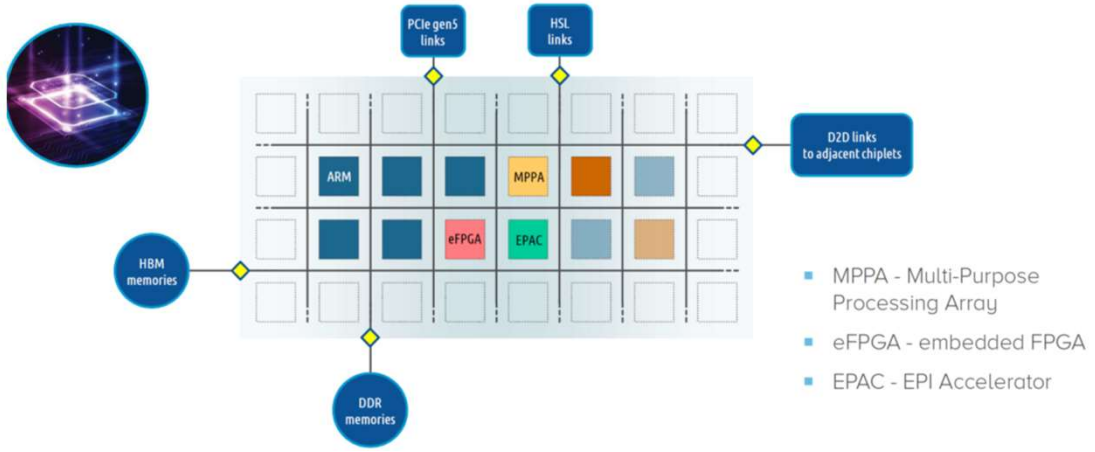
EPI PARTNERS

ACES Vehicles & Mobility



Roadmap & ArchitEcture





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Motivations

- In Automotive Applications, Machine Learning (ML) and Deep Neural Networks (DNNs) must run in vehicle, without relying on internet connection and remote services
- Thus we need both a high computing power onboard the vehichle, and/ore more efficient representation of the information
- The representation chosen for real numbers has a high impact on the synthetized hardware (cores, SoC acceletarors, etc.)
- In this work we will review the state-of-the-art of representation for real numbers
- Then we will present the novel **posit** format
- Then a posit library developed in Pisa: the cppPosit library
- Then its performance on a ML application (K-NN) and on DNN-based image classification
- Finally we will discuss possible extensions of the posit library and its high level synthesis

Alternative Representation For Real Numbers

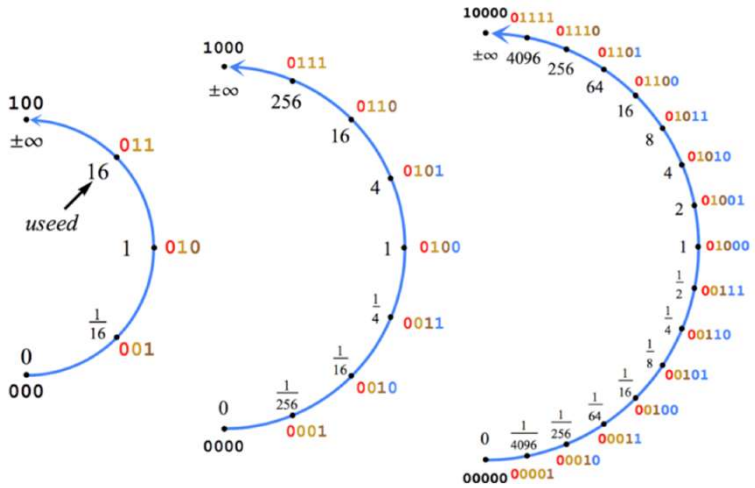
- The floating-point representation (IEEE standard n. 754 of 1985, updated in 2008) has some limitations:
  - The support to unnormalized numbers is tricky (requires more hardware)
  - To many representations wasted for Not-A-Number (again, requires more hardware)
  - Uses the same number of bits for the mantissa, both for small and large numbers (and this is inefficient)

Computing Industry Is Looking for Alternatives Too

- Intel/Google BFLOAT16 (equivalent to a standard single-precision floating-point value with a truncated mantissa field). Basically, they are less precise than fp16, but with a range similar to fp32. Supported in Google cloud TPU and TensorFlow and Intel AI processors
- Intel flexpoint (16bits size aiming at equivalent fp32 accuracy)
- NVIDIA (e.g. concurrent execution of Floating Point and Integer Instructions in the new Turing SM; from Fp32/Fp16and INT32 to INT8 and INT4 precision modes for inferencing workloads that can tolerate quantization)
- Tesla FSD chip (Neural processing units use 8-bit by 8-bit integer multiply and a 32-bit integer addition)
- Transprecision computing proposed in state of art (e.g. Greenwaves, IBM,..)

The Novel Posit Format

- Proposed by John Gustafson in 2017
- It can be viewed as a compressed floating-point format, which deserves more mantissa bits for low number and less for large numbers (within a fixed-length format)
- No-need to use un-normalized floats (so, no extra-hardware wasted to handle this exception)
- Only one representation wasted for Not-A-Real (NAR)
- Posit numbers use an interesting encoding which allows, to compare two posits, to reuse the same circuit used to compare two integers in 2's complement already present in the ALU



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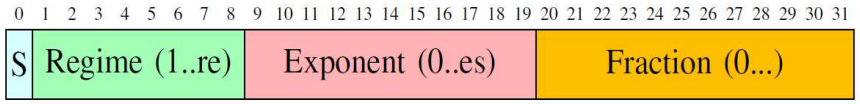


Fig. 1. An example of Posit data type.

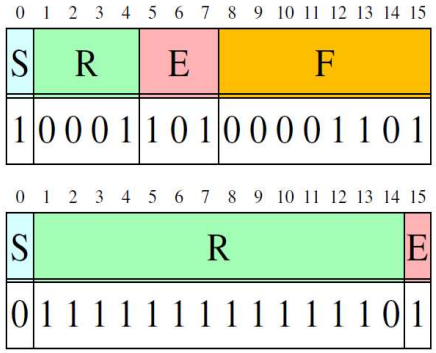


Fig. 2. Two examples of 16-bit Posit with 3 bits for exponent (es=3). In the upper the numerical value is: $-256^{-3} \cdot 2^{5} \cdot (1 + 13/256)$ (13/256 is the value of the fraction, 1 + 13/256 is the value of the mantissa). The final value is therefore $-1.907348 \times 10^{-6} \cdot (1+13/256) \cong -2.0042 \times 10^{-6}$. In the lower the numerical value is: $+256^{+12} \cdot 2^{4} \cdot (1 + 0)$ (since the fractional part of the mantissa is missing, we set it to zero). The final value is therefore $2^{16} \cdot 2^{4} \cong 1.2676506 \times 10^{30}$. The second example allows to clarify that: i) the fractional part can be missing, ii) the exponent field can be shorter than its maximum size (in that case the missing bits are assumed zero: the exponent 4 comes from the reconstructed exponent field 100).

The cpp-Posit Library developed in Pisa

- State-Of-The-Art Posit library, developed in Pisa
- Very efficient (written in C++, fully exploiting templates and several features of the C++14 standard)
- Emulates a Posit Processing Unit (PPU) using, either
  - The FPU and the ALU, or
  - The ALU alone (the FPU is emulated using softfloat)
- Supports **TABULATED POSITS** (using look-up-tables, for posit having total length <= 14 bit): this speedup the library, a mandatory feature to train DNNs
- Next goals (ongoing activities):
  - Exact Dot Product (see next slides): **main goal 1**
  - High Level Synthesis in FPGA/ SoC Accelerator: **main goal 2**

Are Posits Really Better Than Floats?

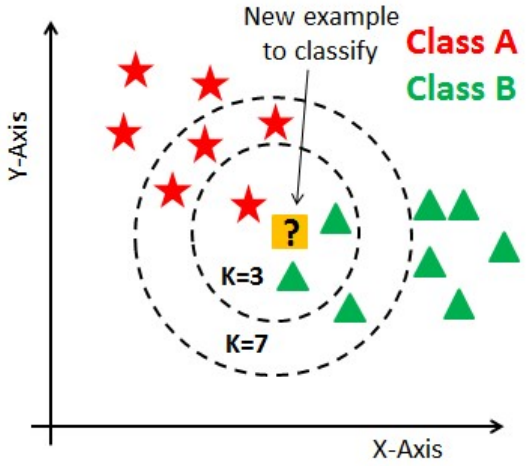
- Yes!
- UNIPI has performed comparisons on both Machine Learning (K-NN) and Deep Neural Networks for Image Classification (we extended the tiny-DNN C++ library)
- We have found that, on a K-NN application (see next slide):
  - a 16-bit posit is as accurate as a 32-bit float (*single precision*)
  - an 8-bit posit is much better than a 16-bit float (*half precision*).
- On an DNN used for image classification:
  - a 10-bit posit is as accurate as a 32-bit float (>98.5% of correct classification)
  - a 8-bit posit is able to provide a very high accuracy (>97%)
- Both cppPosit-based K-NN and tiny-DNN libraries have been selected as WP1 benchmark applications (they support both floats and posits)

The Cpp-Posit based K-NN Library

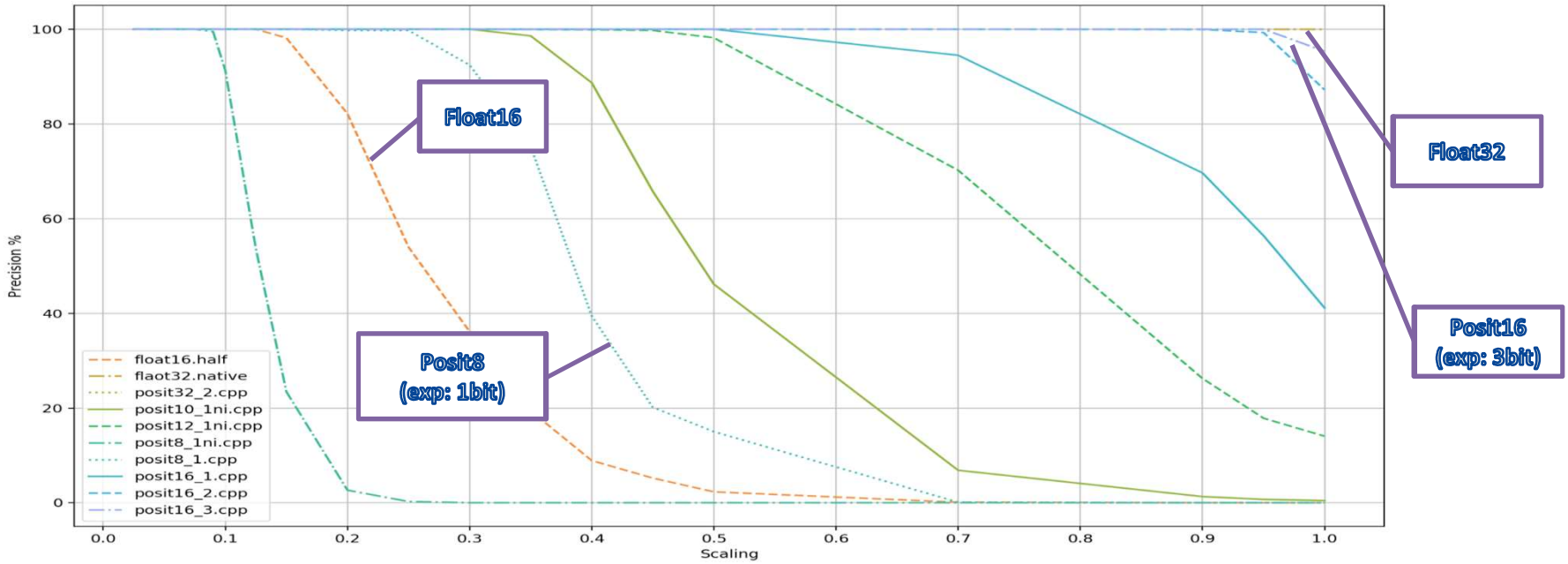
- The K-NN algorithm searches for the K points in a dataset that are the closest to a given query point.
- It can be computed in an exact or approxima
- We implemented the approximated NI and poits
- We have compared the two formats or benchmarks:
  - Fashion Mnist 784 Euclidean

    http://ann-benchmarks.com/fashion-mnist euclidean_10_euclidean.html
  - SIFT-128-Euclidean

    http://ann-benchmarks.com/sift-128-euclidean_10_euclidean.html



Comparing Posits and Floats on K-NN



The scaling factor is used to re-scale the dynamic range
of the original dataset, without affecting the relative dynamic.

Scale 1.0: original dataset. For a given scaling factor, the higher the precision, the better

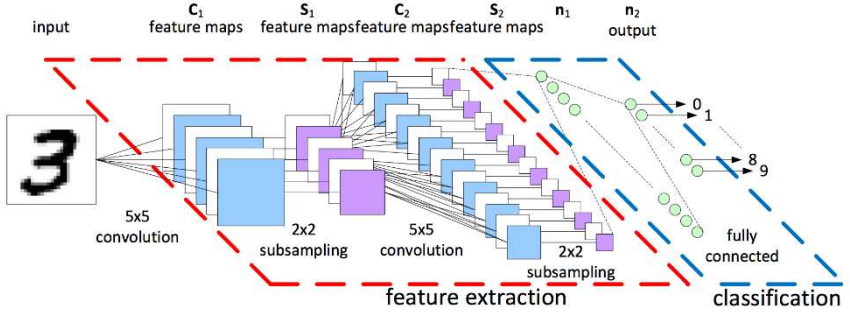
Experiments with Deep-Neural Networks

- We started from the open source C++ DNN library tiny-DNN
- We integrated the cppPosit library with tiny-DNN
- We have been able to show that a posit12 DNN reaches the same accuracy of the float32 counterpart
- To speedup the learning phase, we tabulated the posits (LUT, Look-Up Table approach)
- Acceptable performance can even be attained using an 8-bit

DNNs for DIGIT Recognition within the UniPI Extended Tiny-DNN Library

- **MNIST** dataset: 10 classes, 10,000 samples
- Convolutional Neural Network

Data Type (tot_bits, exp_bits)	Accuracy on 10,000 images
Float32	98,88%
Posit16,2	98,88%
Posit14,2	98,85%
Posit12,2	98,66%
Posit10,0	**98,69%**
Posit8,0	**97,24%**



- Similar results obtained on **CIFAR10**.
- Currently investigating the **ImageNet** dataset, using the AlexNet pre-trained network

Experiments with Deep-Neural Networks

- We started from the open source C++ DNN library tiny-DNN
- We integrated the cppPosit library with tiny-DNN
- We have been able to show that a posit10 DNN reaches the same accuracy of the float32 counterpart
- Currently cppPosit library **emulates** posits using
  - either the FPU and ALU, or
  - the ALU only
- What is needed is a Posit Processing Unit (PPU) implemented in hardware (main goal 1)
- At the moment we have been able to speed-up the neural network learning phase by using **tabulated posits** (look-up table approach). This is suitable only for Posit up to 14 bits. Posit16 and Posit32 must be provided in hardware: PPU16 and PPU32

Advantages of Posits vs Floats

- Lower memory footprint (on RAM, on disk)
- Higher bandwidth
- Lower power consuption
- More cache-friendly (due to the use of shorter data)
- More suited for vectorization (again, shorter data means more data on registers at the same time – see ARM SVE)

Final Goal: High Level Synthesis of the PPU

Final Goal is the High Level Synthesis of the PPU in FPGA/SoC Accelerator, starting from our cppPosit Library.

A Posit Processing Unit (PPU) can automatically synthesised e.g. using the Vivado toolkit.

The cppPosit library allows the automatic VHDL code generation starting from C++ source code.

An alternative is a LUT-based tabulated implementation of a PPU, particulalry for posits with max 8 or 10 bits

Memory need to store the single LUT as a function of X (total number of bits of the Posit)

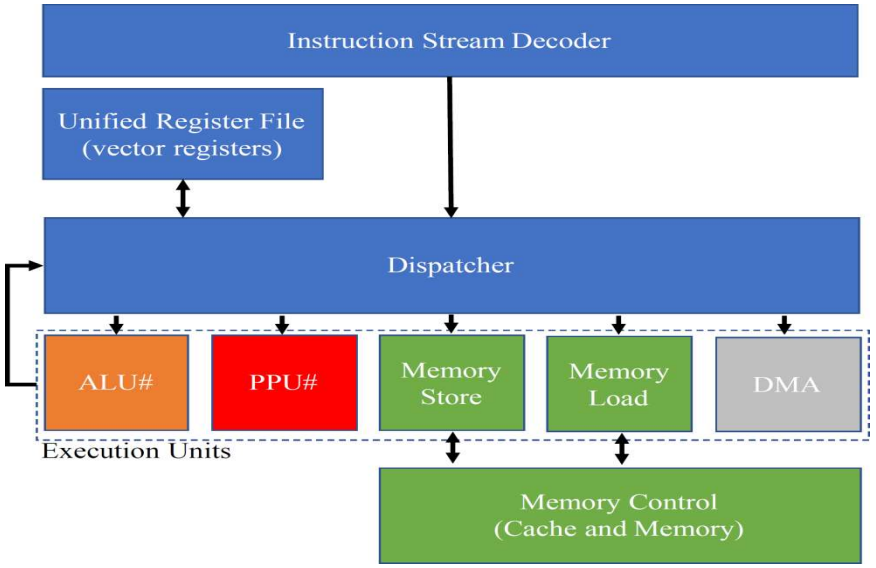
Total bits (X)	Storage type bits (b)	Per-table occupation
8	8	64KB
10	16	2MB
12	16	32MB
14	16	512MB
16	16	8GB

Challenges in Dimensioning a PPU

- The total number of bit must be carefully decided. It is, of course, application dependent.
- The maximum number of bits for the exponent must be decided too.
- Probably, we should implement in hardware the16bit PPU (to cover from float12 to float 32) and the 32 bit PPU (to cover floats > 32bit). We expect that a 32bit PPU is equivalent to a 64 bit float.
- The 8bit, 10 bit and 12 bit PPU dont' need to be implemented in hardware, since the use of LUT is enough in most of the applications

Possible HW Architecture TO Integrate and Better Exploiting Posit Properties

- To compare two posits, we can reuse the same circuitry used to compare two integers, i.e., the ALU
- This requires that the registers of the processor are content agnostic: they can contain, naturals, integers, posits, addresses, at different times.



Exact Dot Product (EDP)

- DNNs heavily use the dot product between two vectors (the matrix-matrix multiplication, for instance, is a series of dot products): $c = \sum_i a_i b_i$
- Traditionally, the FPU does not compute the exact dot product, since it rounds the intermidiate product $a_i b_i$ before accumulating
- Exact dot product techniques, also called «fused dot product», aims at performing the rounding operation only at the end, before storing the result of the output variable c.
- The use of the EDP in DNN can further reduce the number of neeeded bit (a posit8 can reach the same accuracy of a posit12, for instance).
- Implementing in hardware a PPU supporting fused operations between floats (in particular, the exact dot product) is challenging
- It requires a lot of additional circuitery
- A trade-off must be accurately chosen: we are still investigating this issue

Conclusions

- Posits have the potential to overcome most of the float issues in Machine Learning and DNN computing
- They allow to reduce the bandwidth bottleneck problem during read/write from/to RAM
- Have beneficial effects on vectorizable applications, since data are generally shorter
- They are more cache friendly, every time a posit8 can replace a float16, a posit16 a float32 and a posit32 a float64 (i.e., in most of the applications)
- A posit library developed at UniPI (cppPosit)
- Tested on K-NN and DNN benchmarks
- Activity ongoing:
  - Test on additional datasets/applications
  - Recompile on ARM-64 SVE simulator
  - Software implementation of the Exact Dot Product
  - Hardware PPU by high level synthesis

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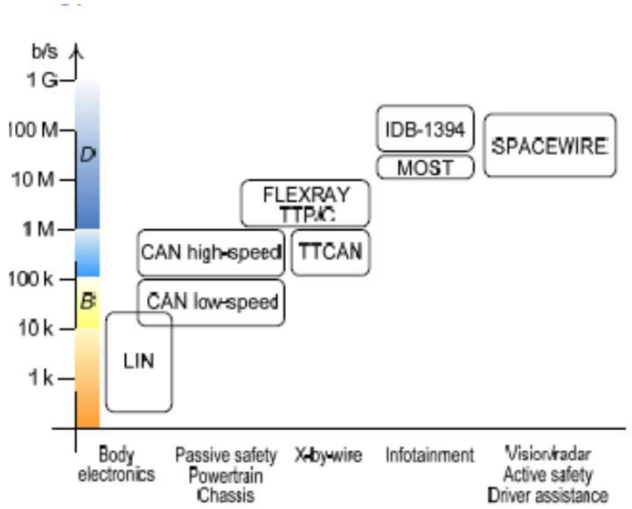
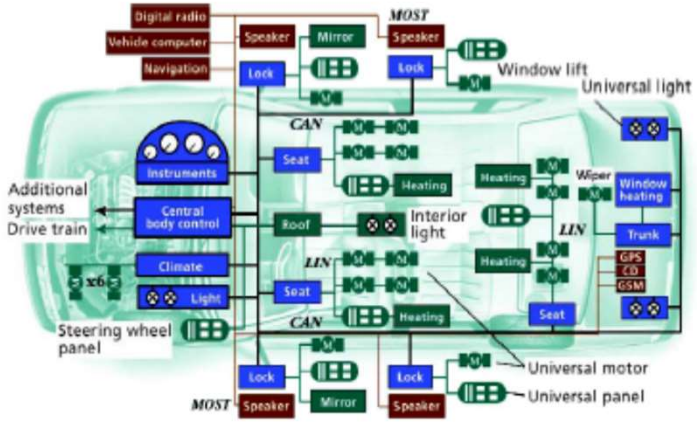
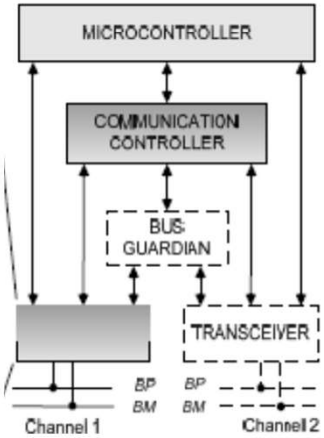
On-board vehicle networking

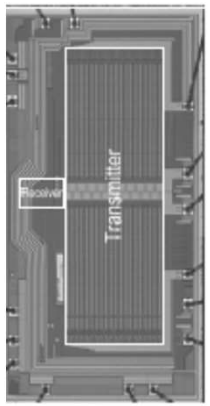




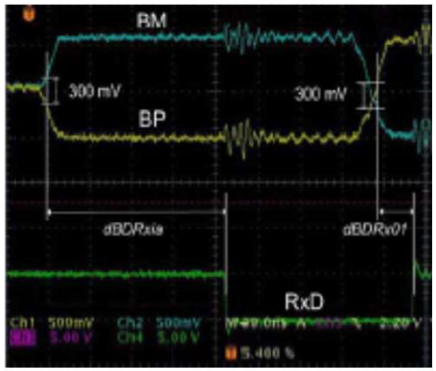
- **FlexRay** nuovo standard event/time-triggered a **10 Mb/s** per **X-by-wire** (su BMW X6)
- **CAN**
- **ISB-1394/MOST per infortainment**
- **LIN per interconnesioni locali a basso bitrate (pochi Kbps)**

On-board diagnostic/control measurements & networking





	min	max
Battery	-0.3 V	+58 V
Bus DC Voltage	-58 V	+58 V
Junction Temp. (TJ)	-40°C	+150°C
ESD (HBM)	-4 kV	+4 kV
Latchup immunity	-100 mA	100 mA



Intelligent Generic Sensor Interface (I-GSI)

Sensors needs signal conditioning in both analog and digital domains for continuous compensation (bias, temperature, …)

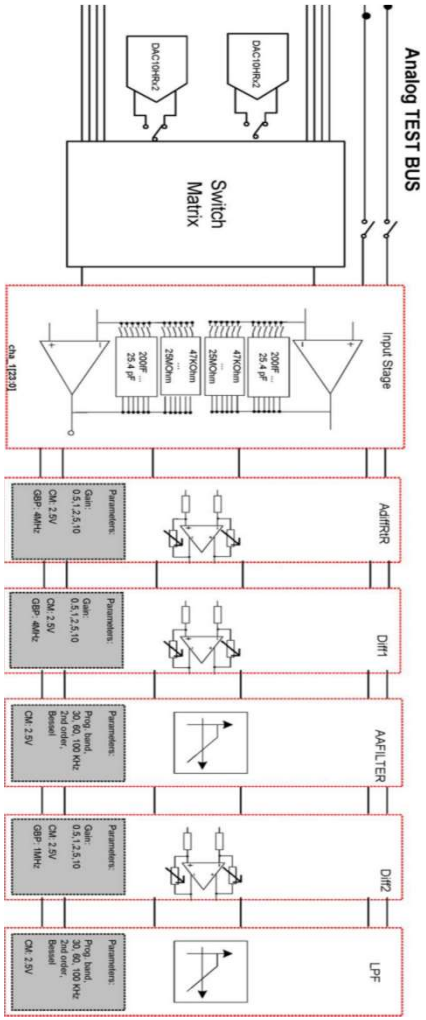
Smart vehicles need lots of different sensors (accelerometers, gyroscopes, temperature., speed, gas leaks, pressure,…)

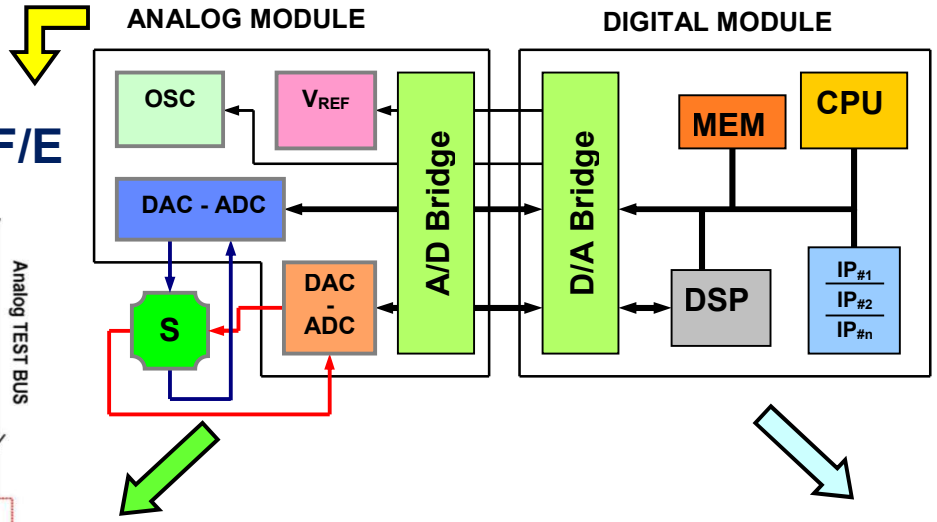
Automotive industry needs low-cost but configurable solutions

Intelligent Generic Sensor Interface

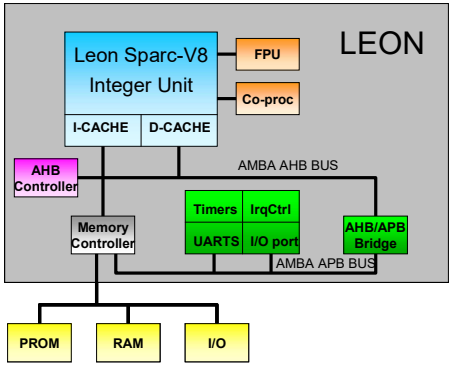
Intelligent Generic Sensor Interface (I-GSI)

Multi-channel config. analog F/E





Processor



Generic Sensor

temperature

speed

pressure

acceleration

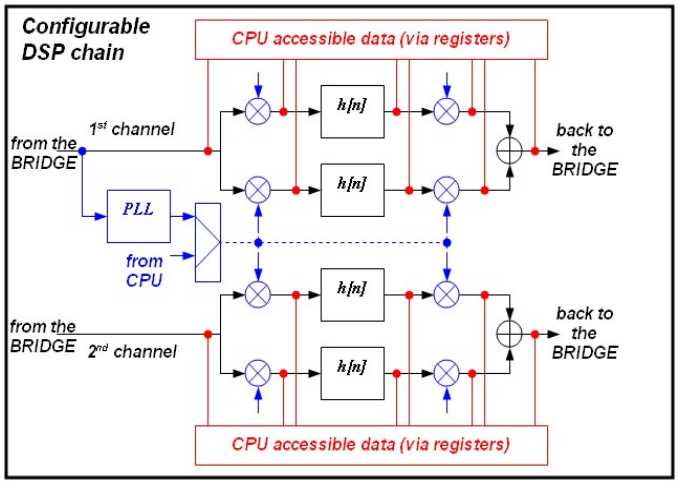
angular speed

gas ……

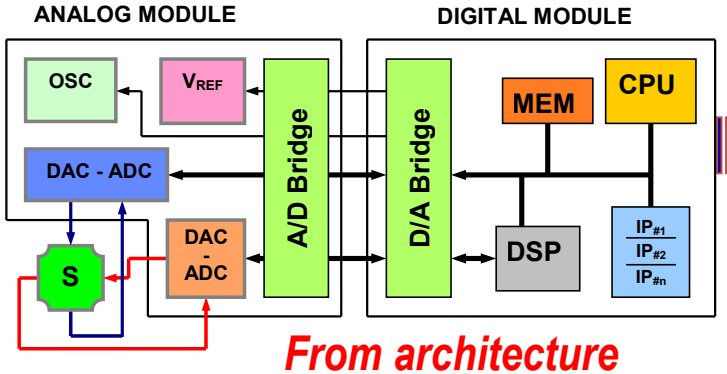
Automotive, Space, Industrial

2 IEEE TIM in 2011, IEEE TIM16

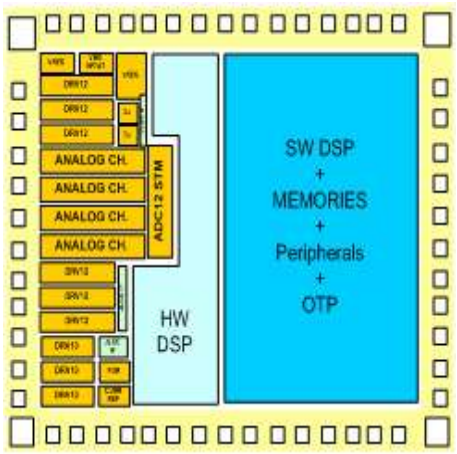
Digital Signal Processing



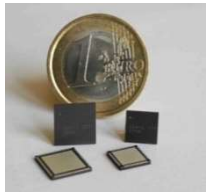
I-GSI platform & specific ICs spin-off



From architecture



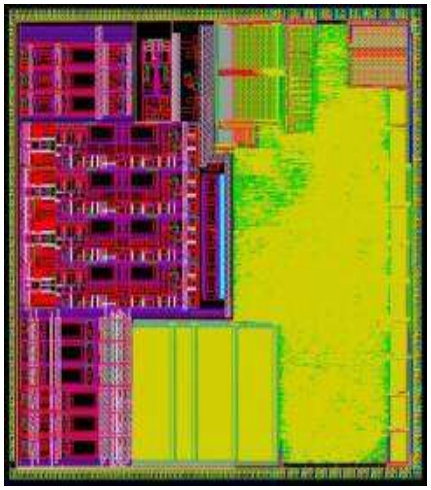
Proven in real-products (SD41x)



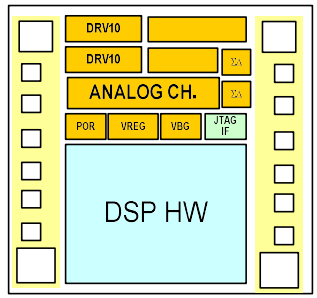
sensordynamics

..to configurable GSI

..to testing



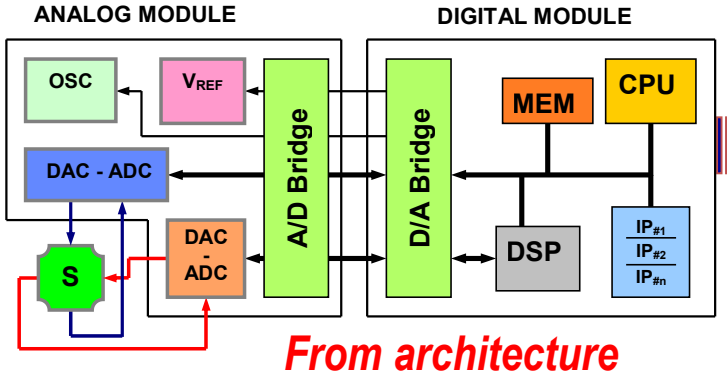
..to silicon (tens of mm2, in 0.25/0.35 μm)



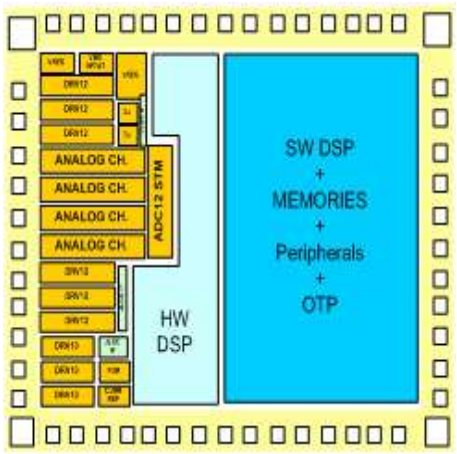
..spin-off of sensor specific ICs low design effort (few mm2)

esa

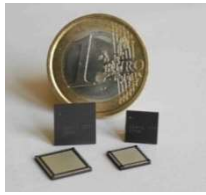
I-GSI platform & specific ICs spin-off



From architecture



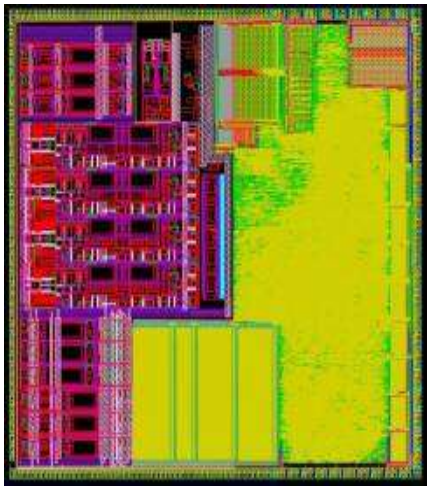
Proven in real-products (SD41x)



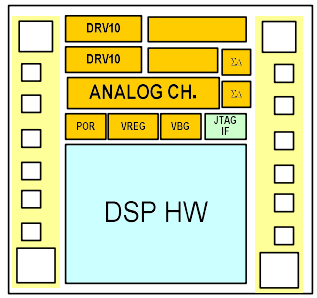
sensordynamics

..to configurable GSI

..to testing



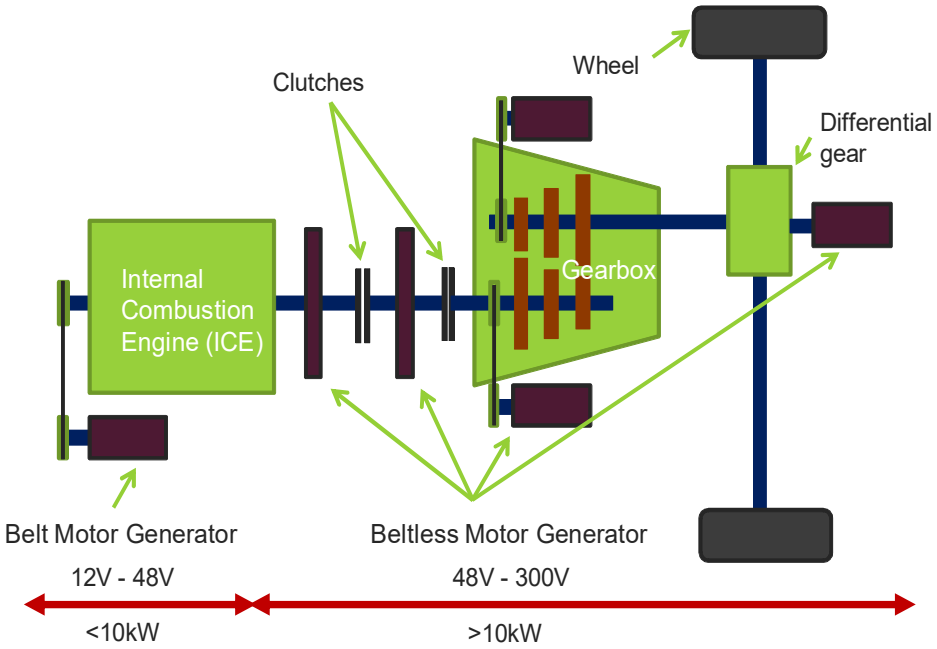
..to silicon (tens of mm2, in 0.25/0.35 μm)



..spin-off of sensor specific ICs low design effort (few mm2)

esa

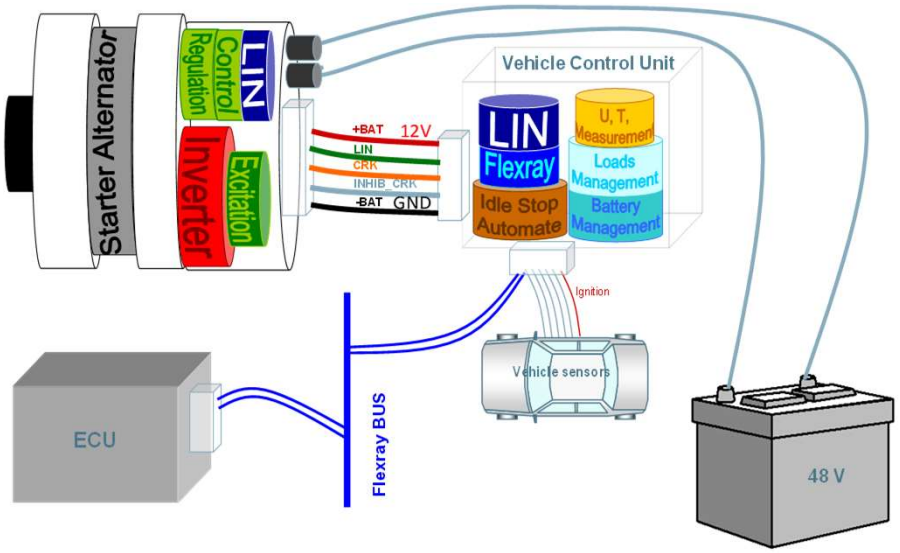
Integrated Power Converters for 48 V micro/mild-hybrid vehicles

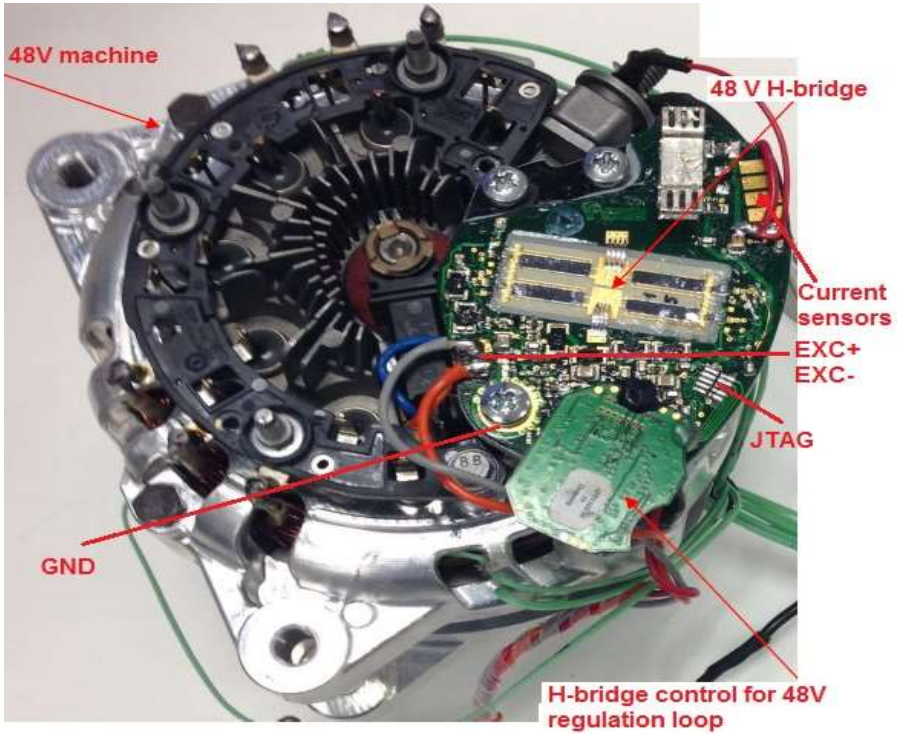


In 48 V micro/mild-hybrid vehicles a integrated starter/generator up to 10 kW, provides starting torque & low-speed torque assistance to the downsized ICE & regenerative braking

Below 70 V schock protection is NOT needed

Integrated Power Converters for 48 V micro/mild-hybrid vehicles

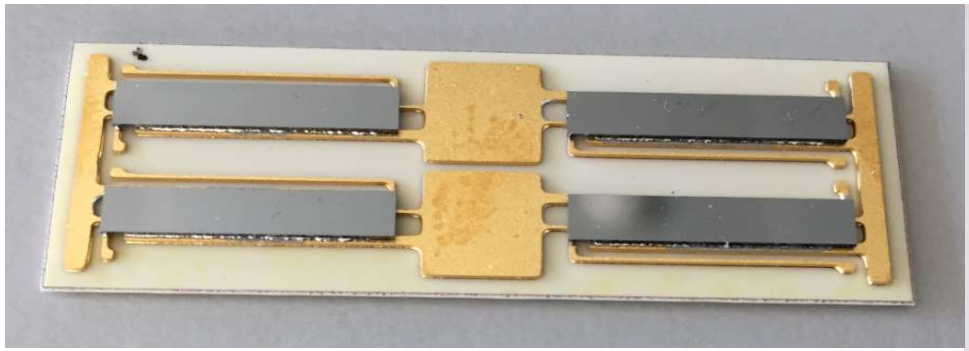


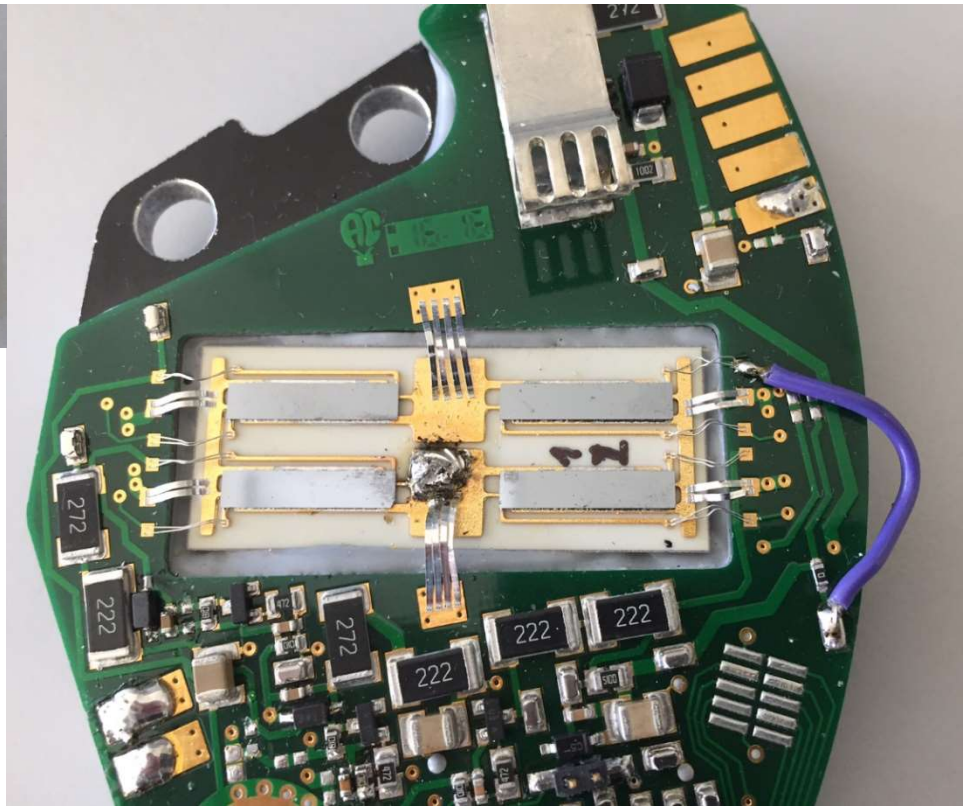


48 V power bridge provides AC excitation to the electrical machine

Collaboration with
Valeo, FP7 Athenis3D

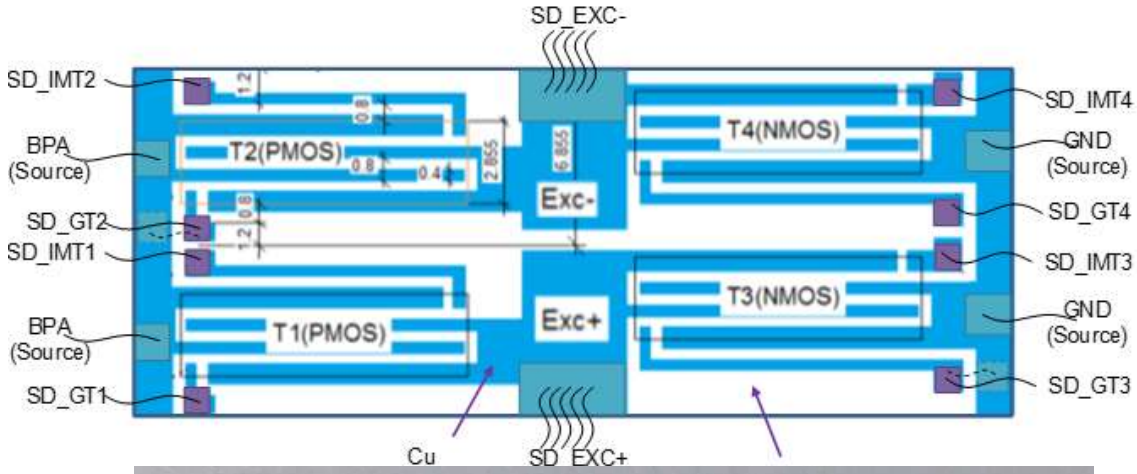
48 V power bridge in 0.18 um HVMOS

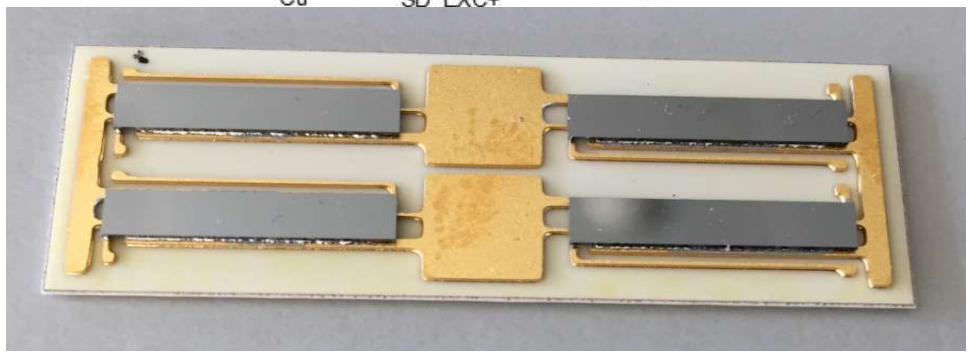


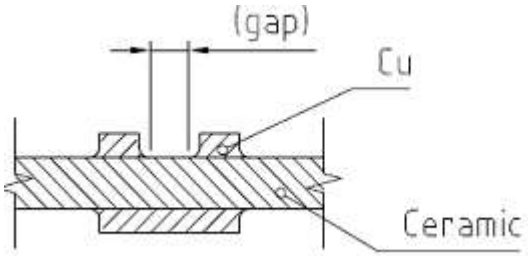


48 V Power bridge embedded within the electrical machine (Ron limited at about 10 mOhm)

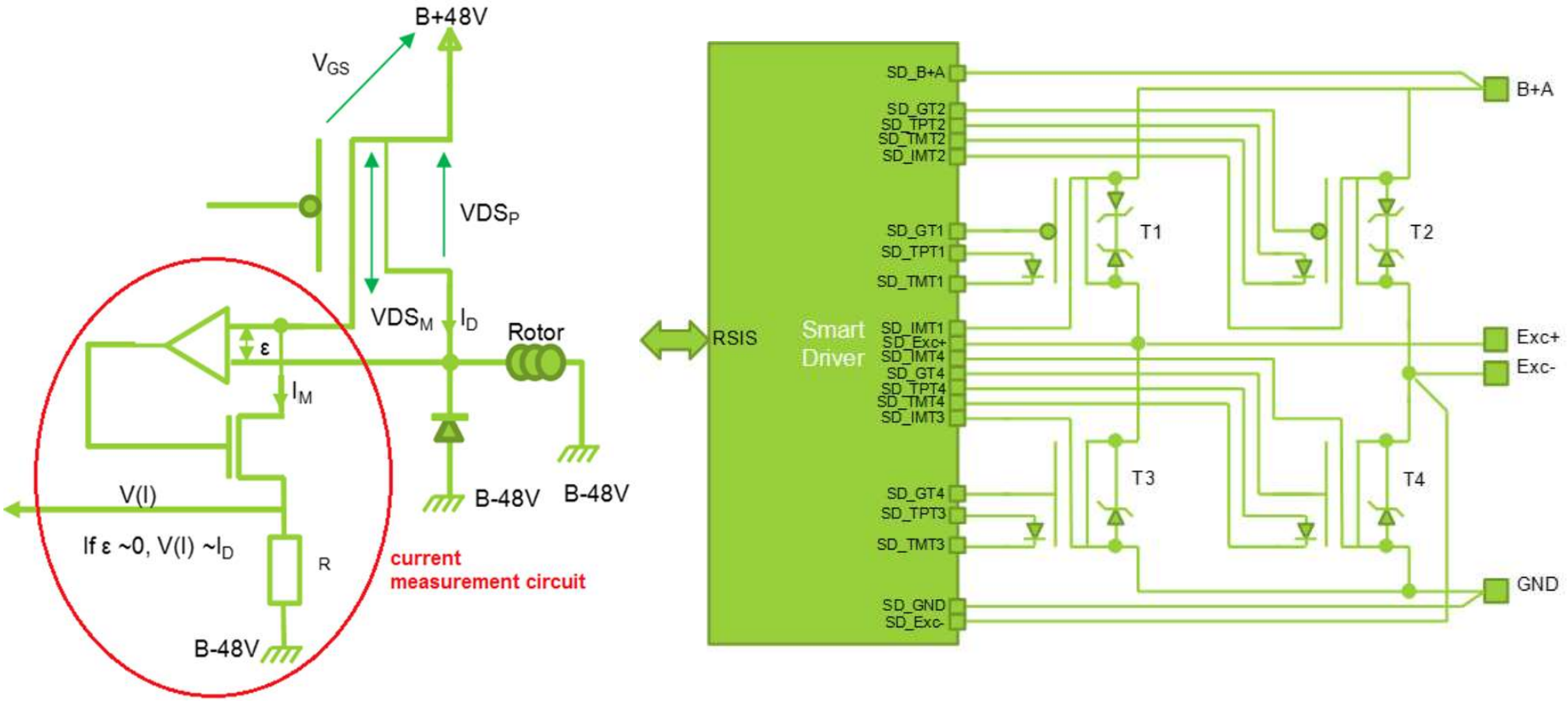
Direct bonded copper to reduce on-resistance



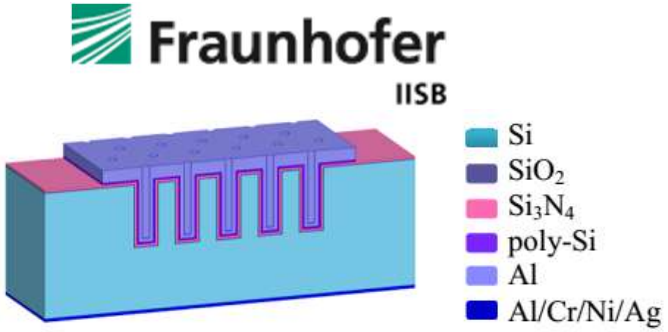


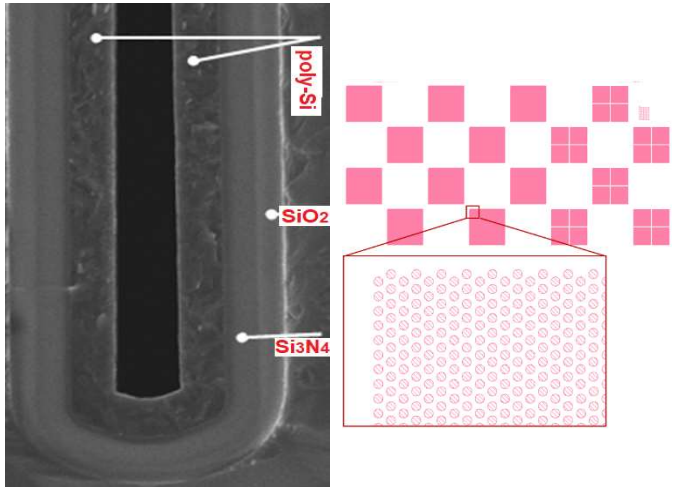


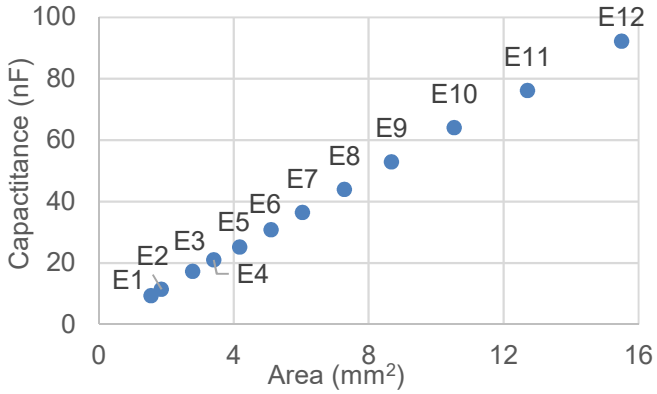
Integrated current measurement

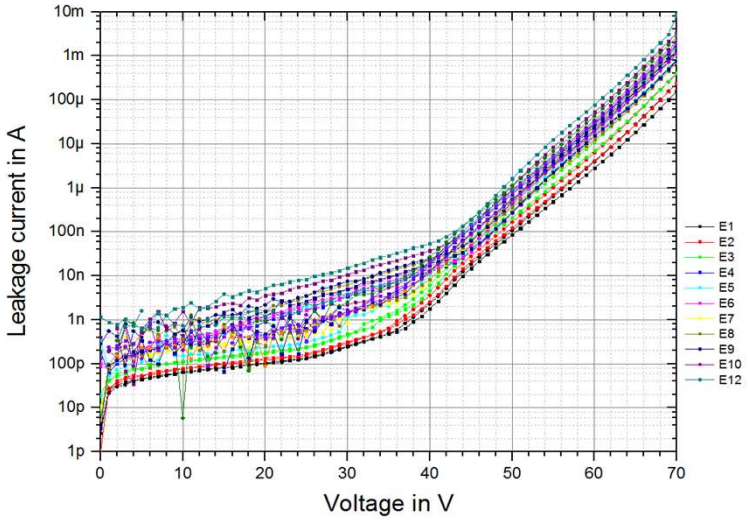


Integrated silicon-TSV HV capacitors







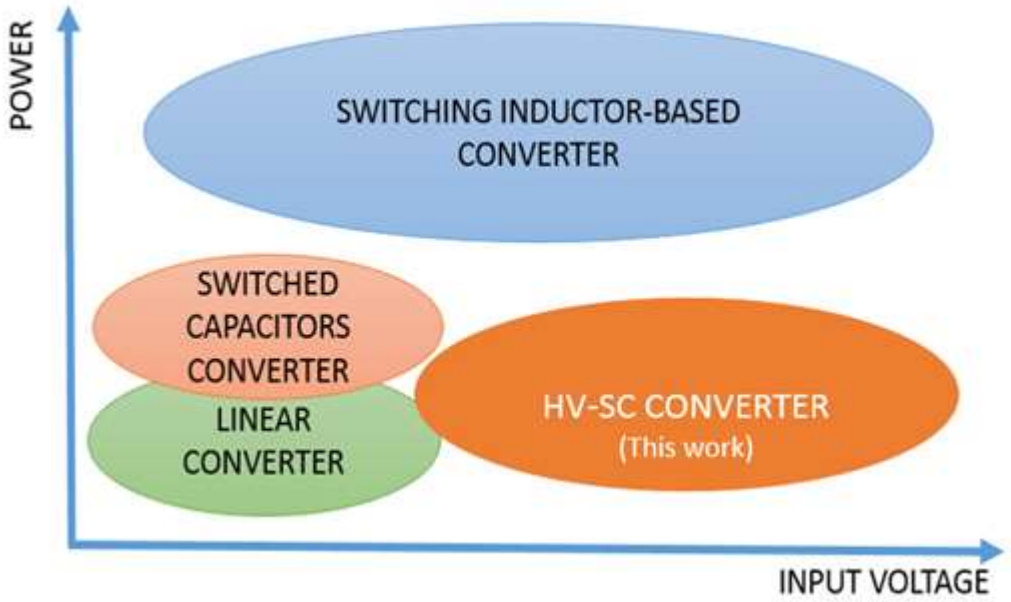


Integrated MOS-compliant power capacitors up to 70 V

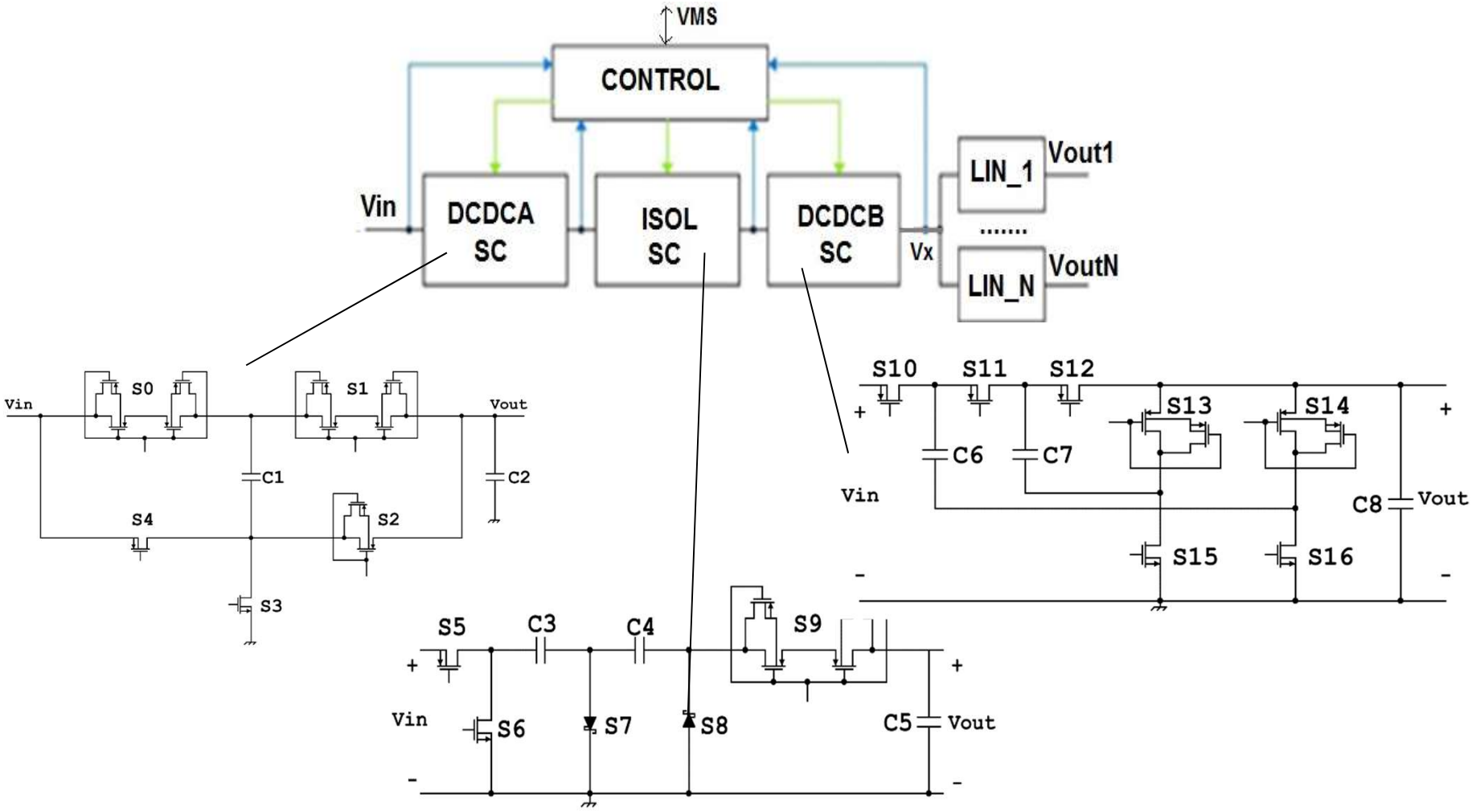
48 V DC/DC converter

In 48 V vehicle systems a DC/DC converter is needed for direct supply of low-voltage loads (processors, sensor, memories)

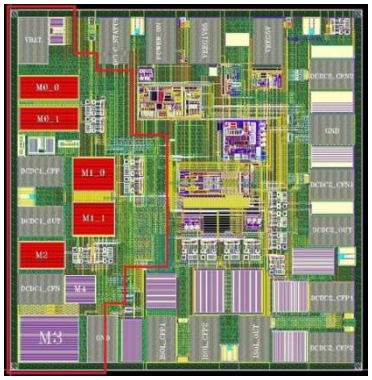
The proposed DC/DC converter covers a gap in state of art (switched cap inductorless converter for high voltage input and low power loads)



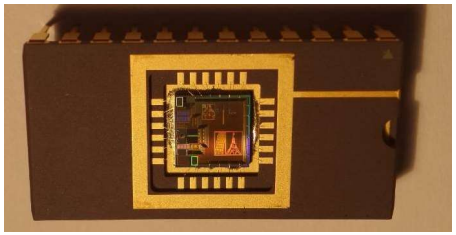
48 V Switched-Cap (SC) architecture

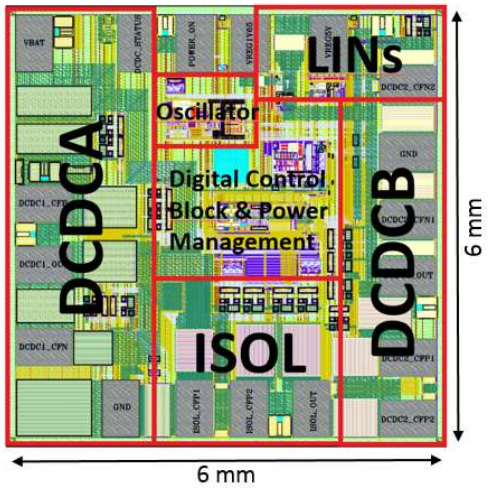


48 V chip layout and test PCB

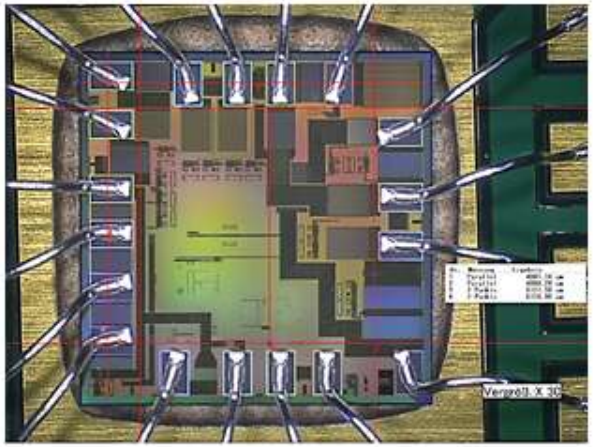


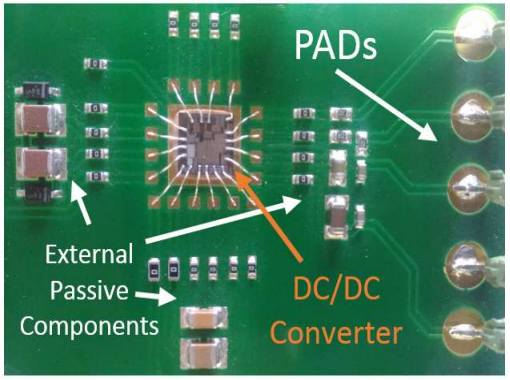
V1



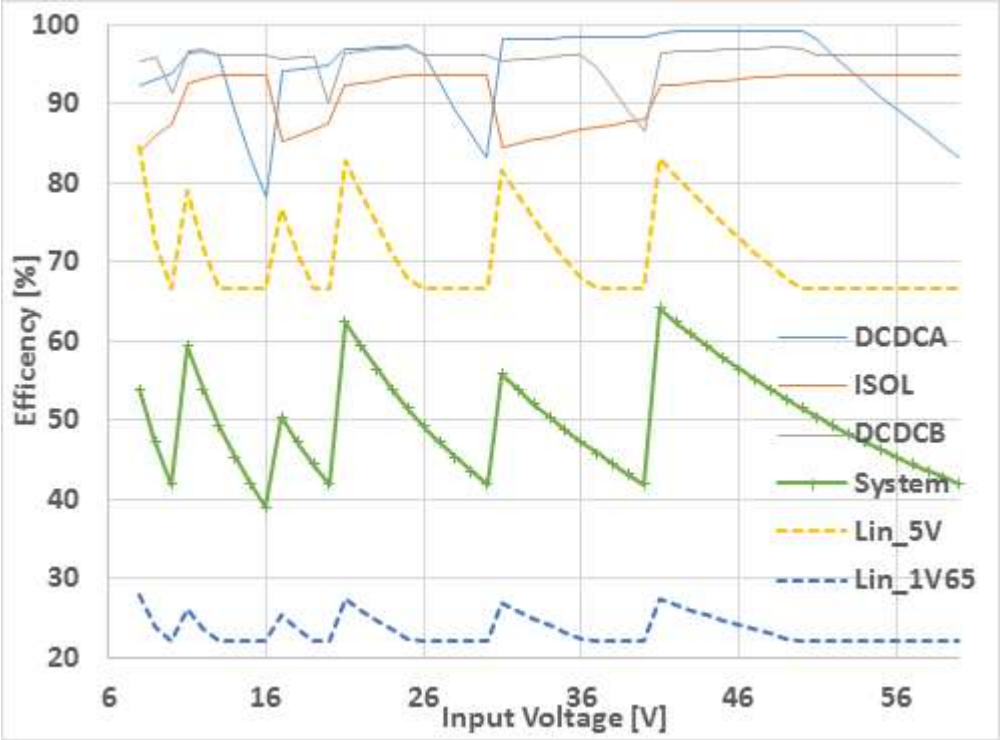


V2

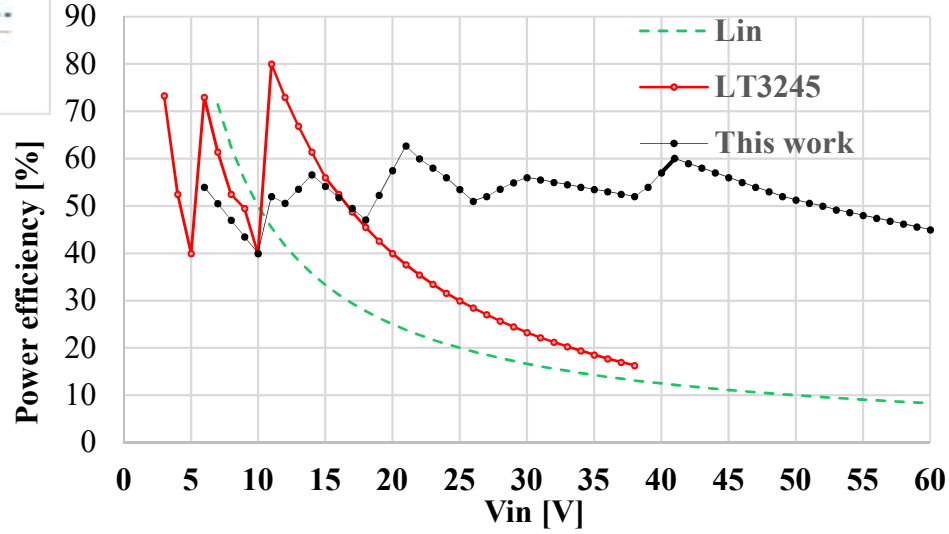




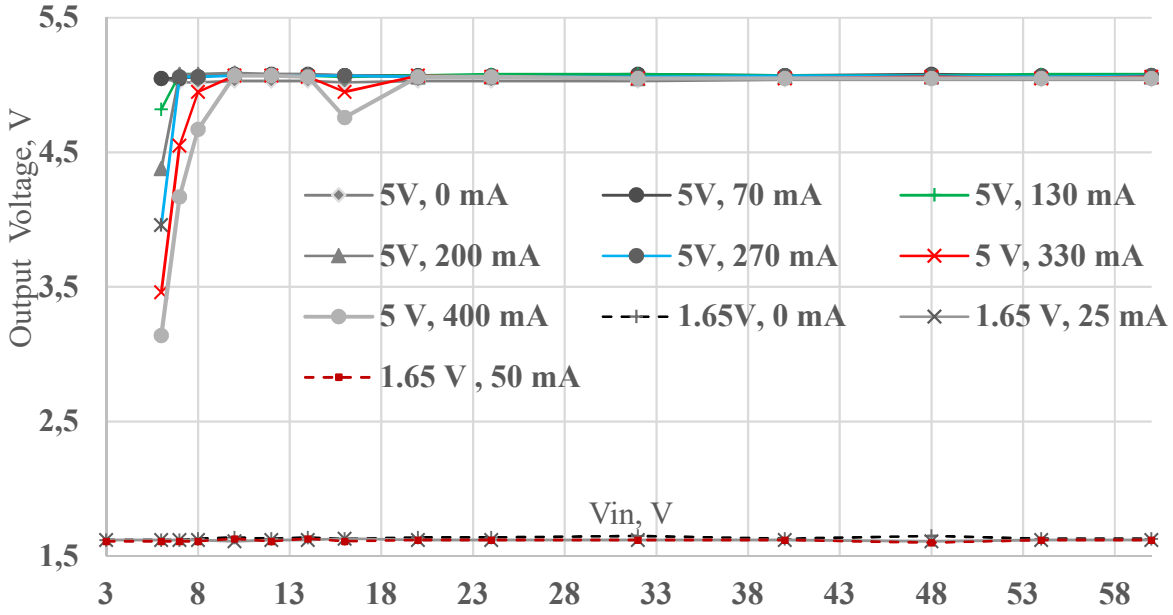
V2 efficiency measurements

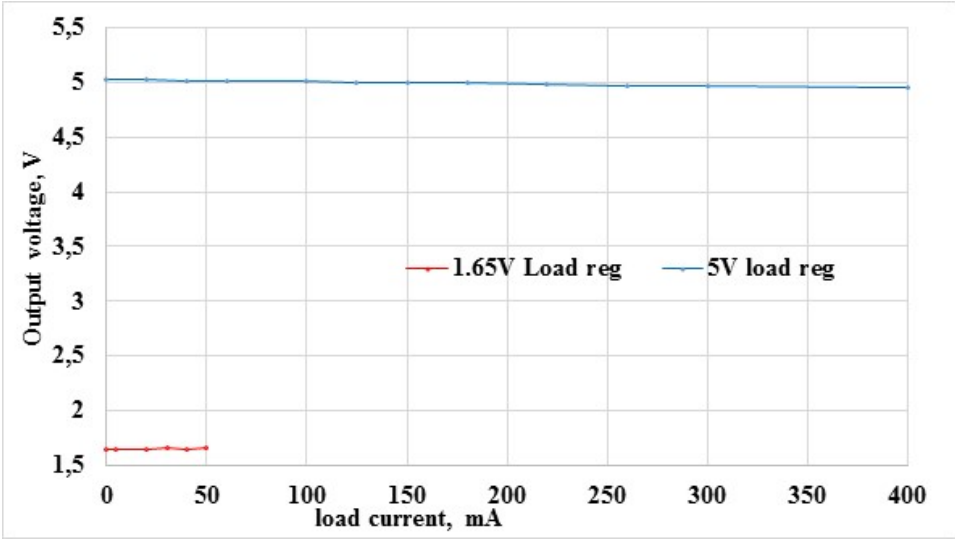


Efficiency of 50-60% much better than linear regulators and than competing ICs in a wider input range (suited for low power loads)



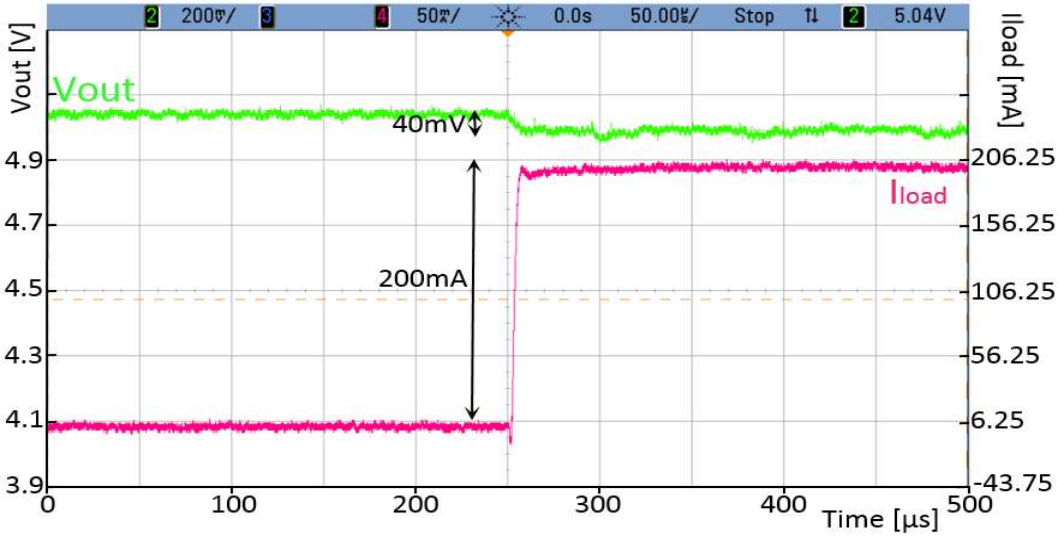
V2 line and load regulation



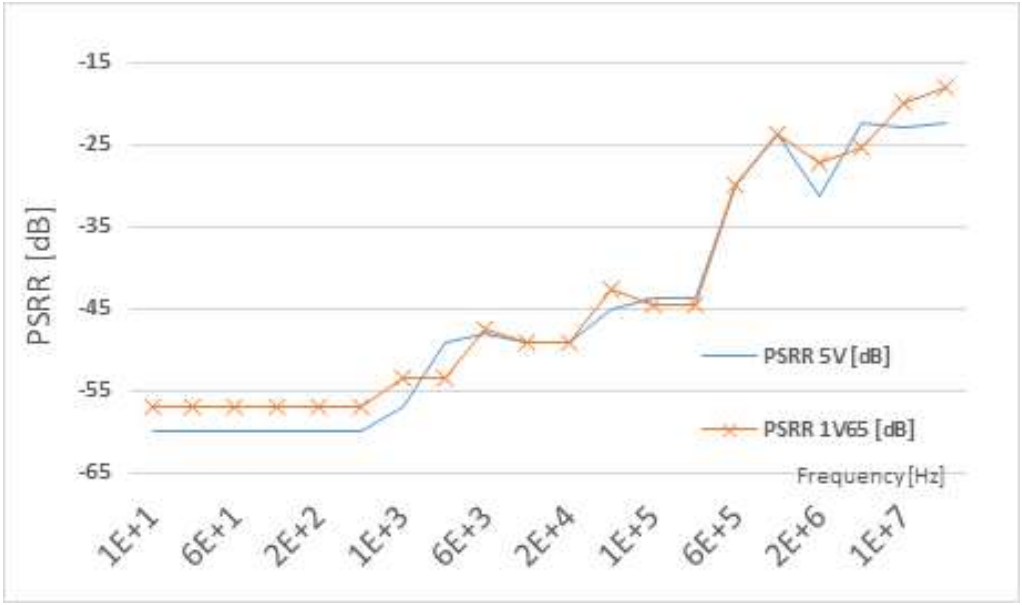


Good line and load regulation performance

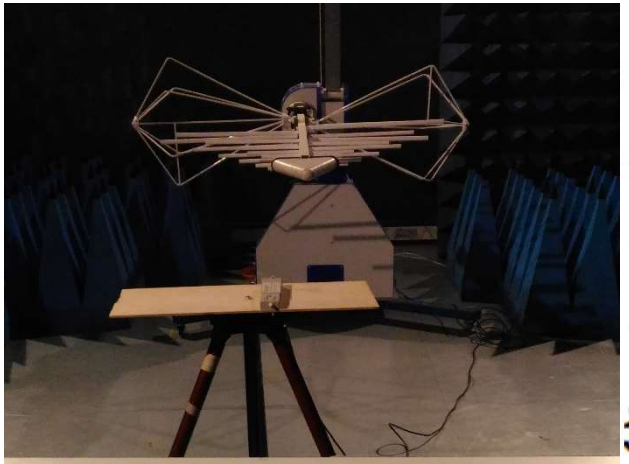
V2 transient response and PSRR

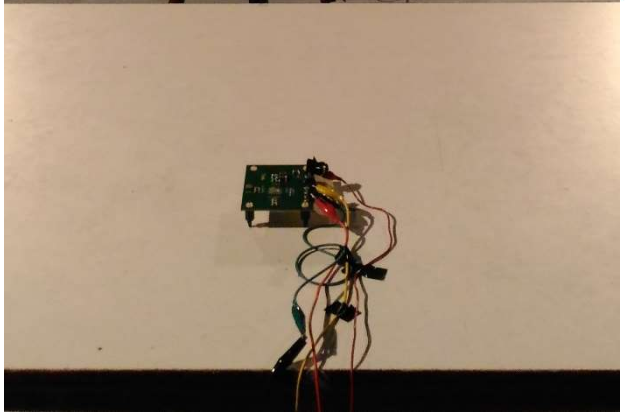


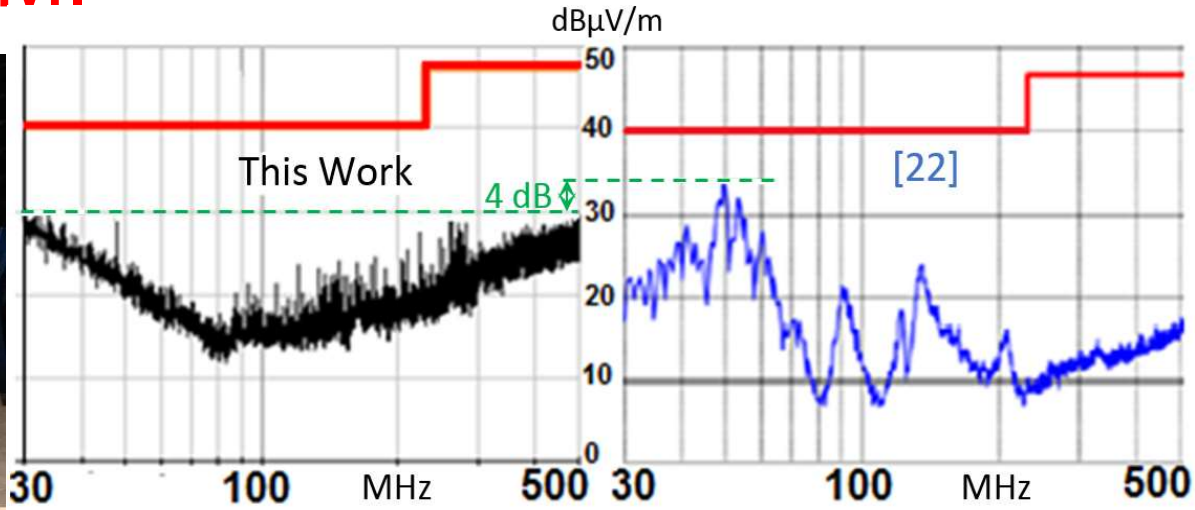
Good transient and PSRR performance

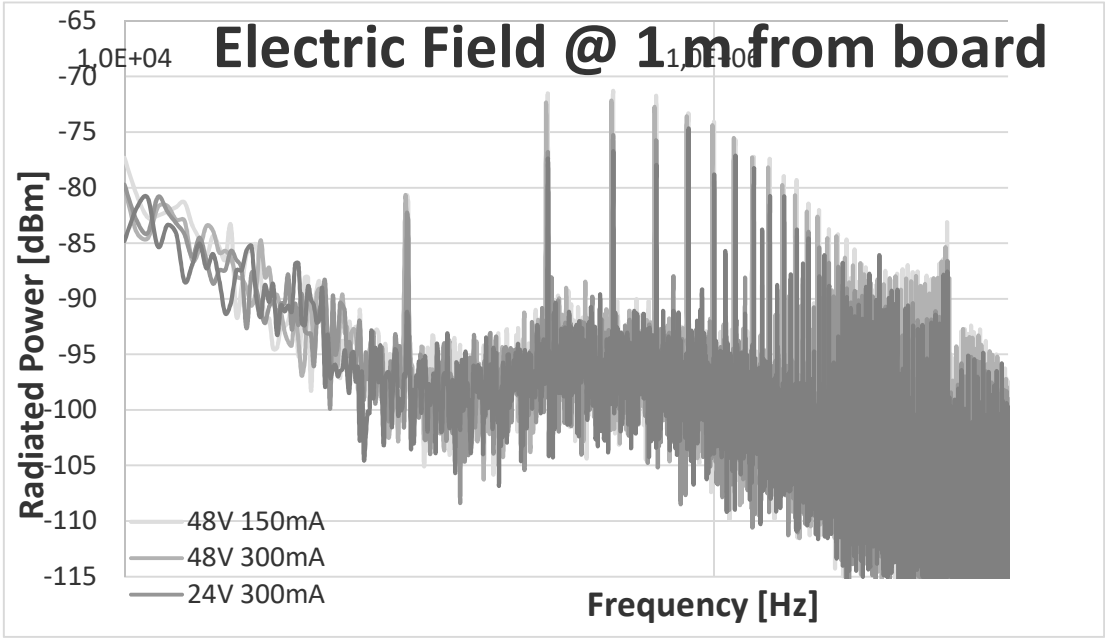


V2 radiated EMI



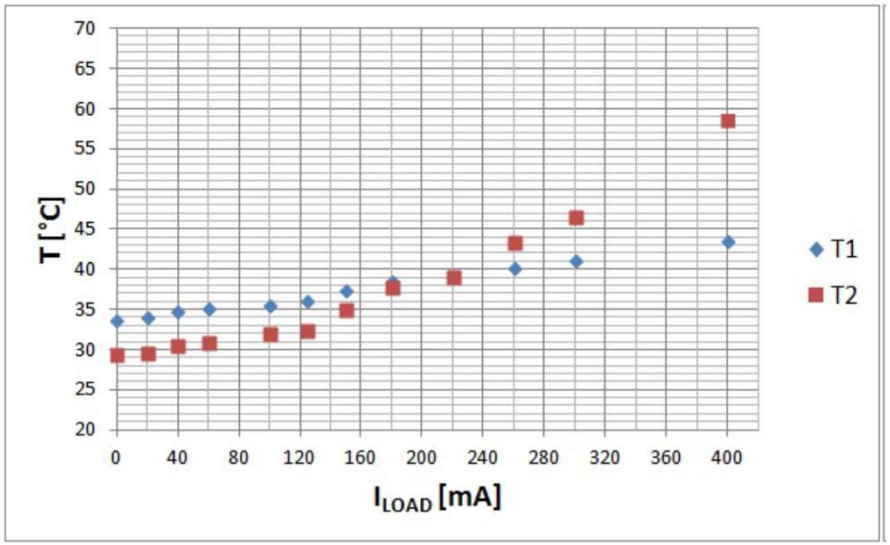






Low radiated EMI

Temperature tests and state-of-art review

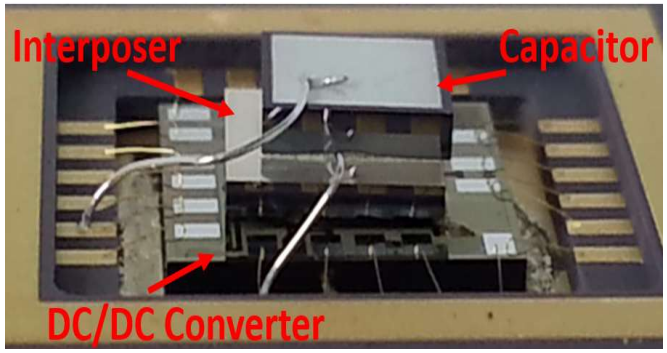


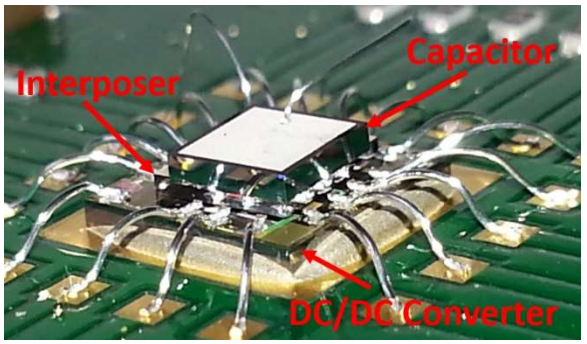
Low over-temperature (can work also without cooling system)

Integrated LDO, I/O insulation and wide input range vs. state-of-art

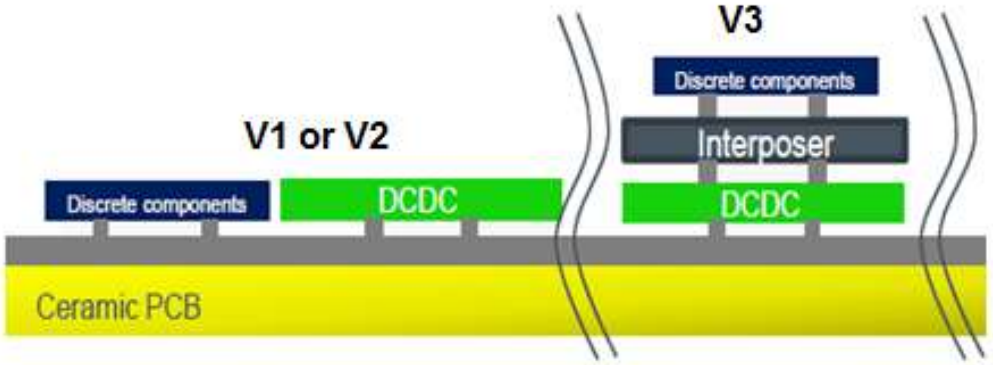
	This Work	PT4660	LT3245	LM5170
Type	SC+linear	Inductive	SC	Inductive
In-Out insulation	Yes	Yes	No	No
Input range [V]	57*	39	35	79
PSRR [dB]	-60	Off-chip LDO needed		
Output voltage [V]	1.65 / 5	3.3 / 5	5	12 / 48
Max load current [A]	0.4	30	0.25	5
Efficiency peak [%]	63	86	81	N/A
Stand-by current [µA]	5	5000	4	10

V3 with capacitors stacked on top





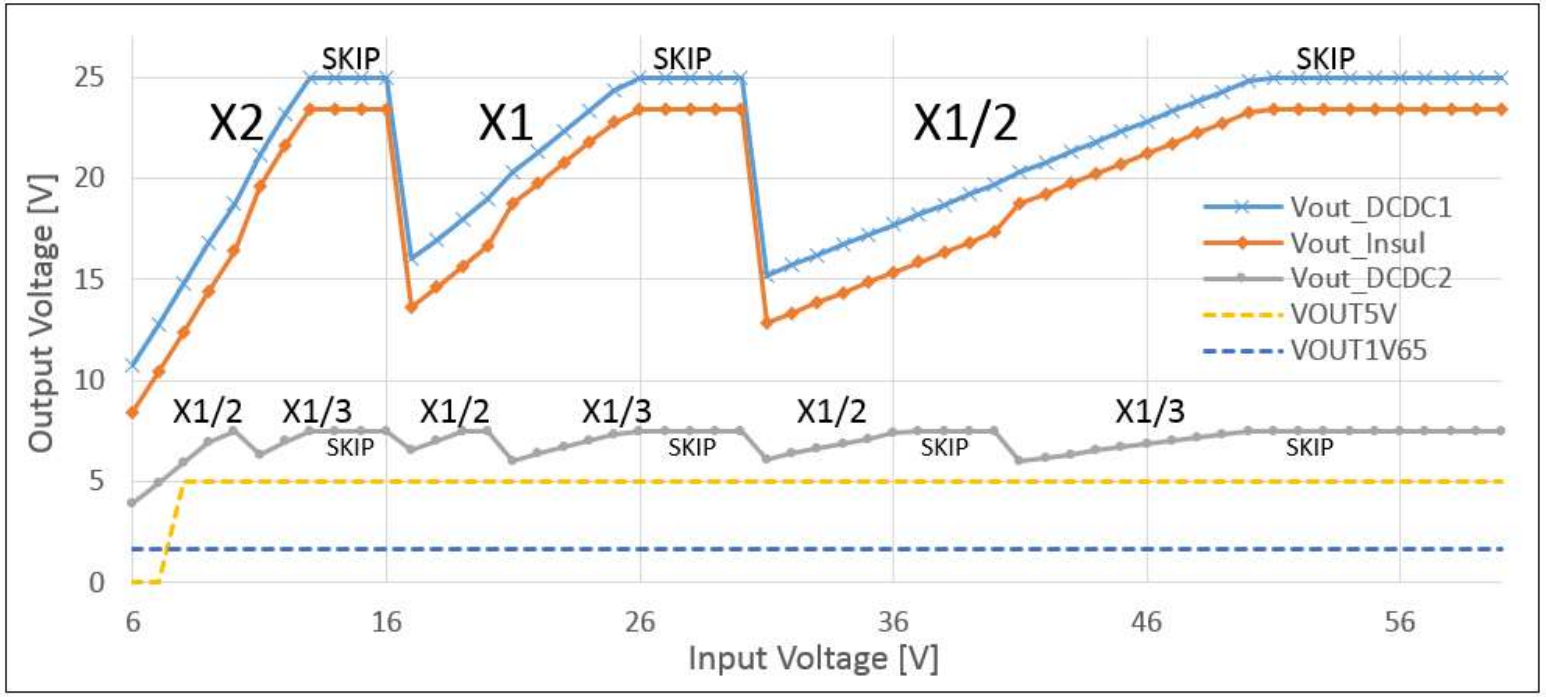
Unaltered performance of V3 vs. V2 but much lower area



Advanced control techniques: Topology reconfiguration

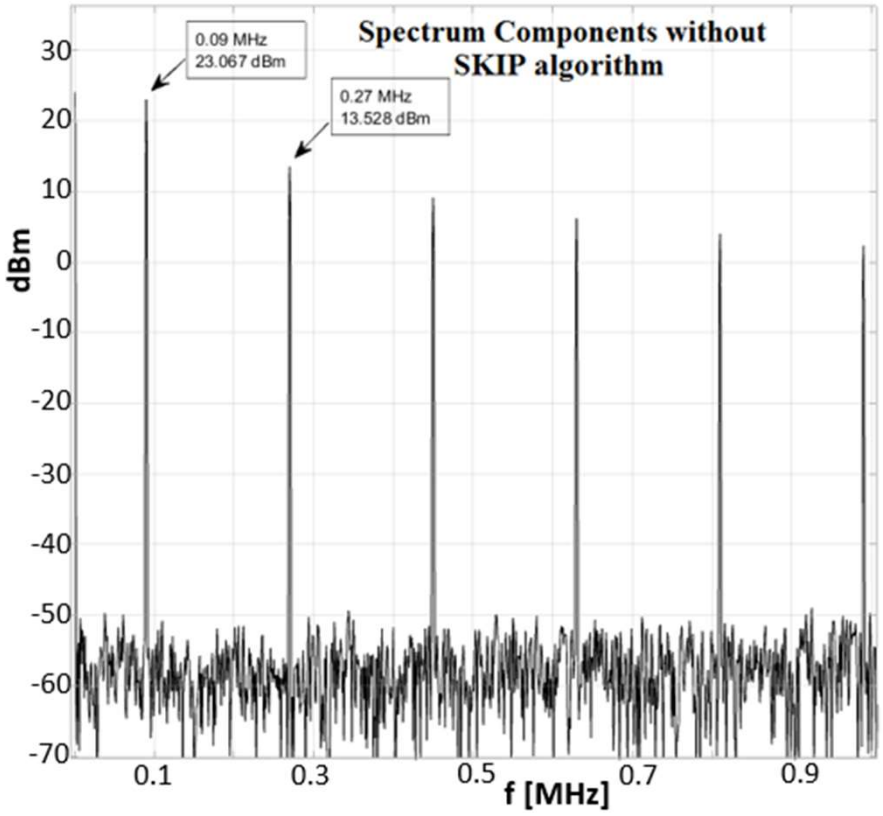
Stage	Input Voltage [V]	VCR	Output Voltage [V]
DCDCA	6 < Vin < 15	2	12 < Vout < 30
	15 < Vin < 29	1	15 < Vout < 29
	29 < Vin < 60	1/2	14.5 < Vout < 30
ISOL	12 < Vin < 30	1	12 < Vout < 30
DCDCB	12 < Vin < 18	1/2	6 < Vout < 9
	18 < Vin < 30	1/3	6 < Vout < 10
LIN_1	V_X > 6	-	5
LIN_2	V_X > 3	-	1.65

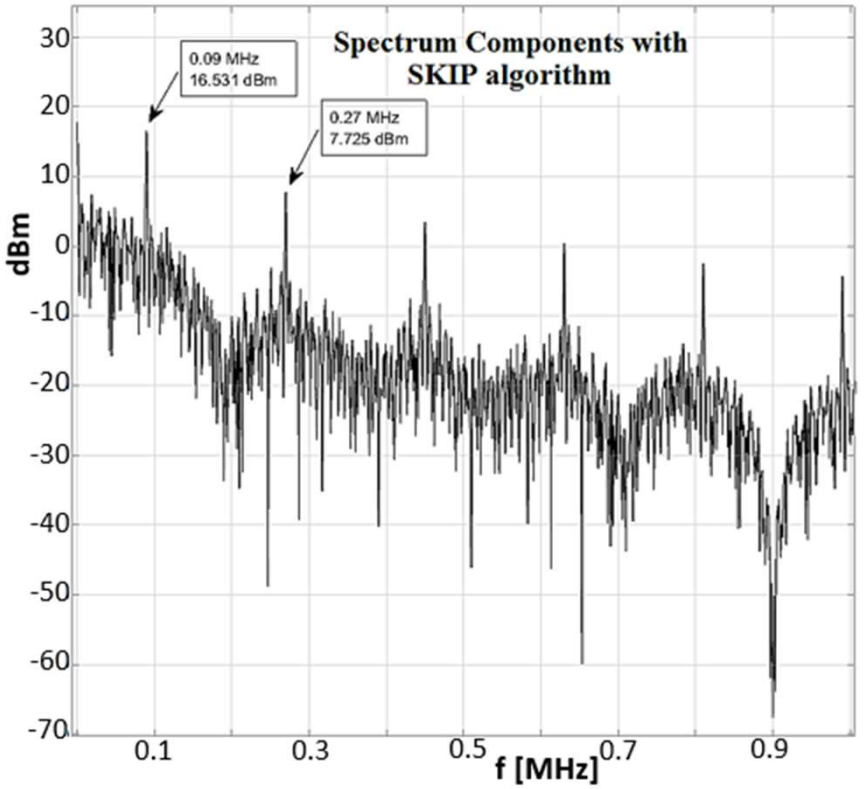
Effects of the control techniques (topology reconfiguration and SKIP-mode on the voltage regulation in the multi-stage DC/DC architecture)



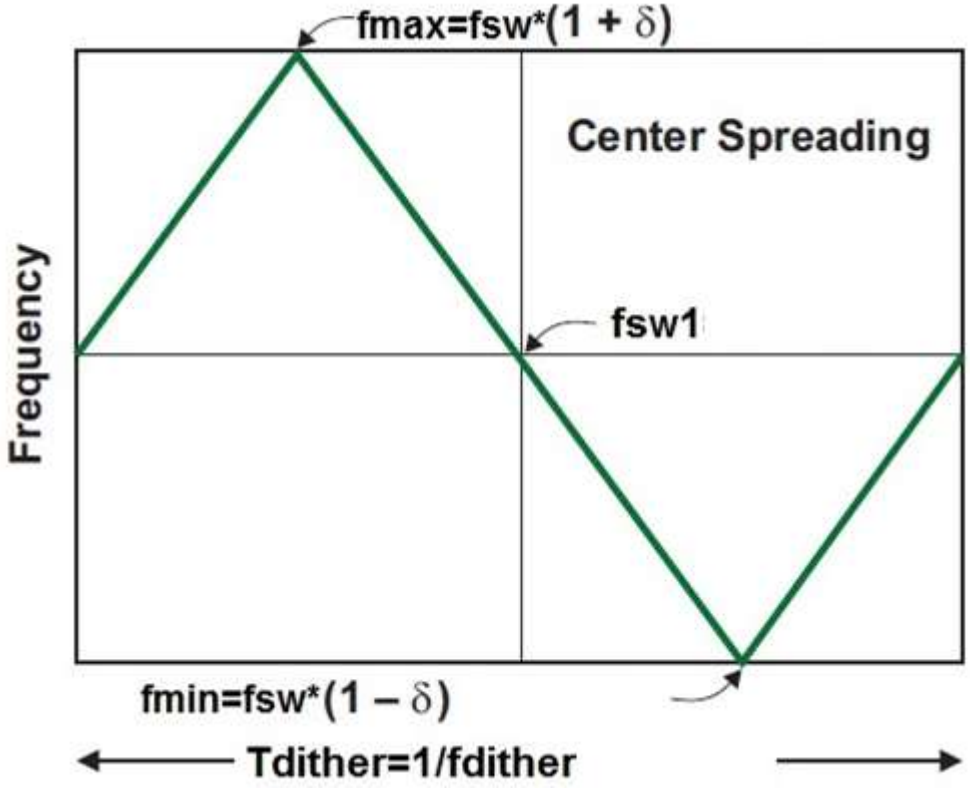
Advanced control techniques: Skip Mode

More than 6 dB reduction of the EM Interference power emission thanks to SKIP-mode. Fixed frequency, like a PWM with duty-cycle hopping between 0.5 and 0



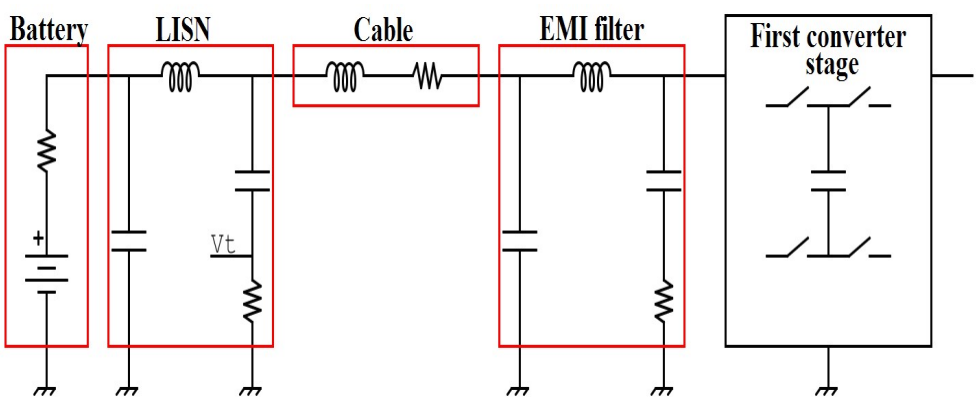


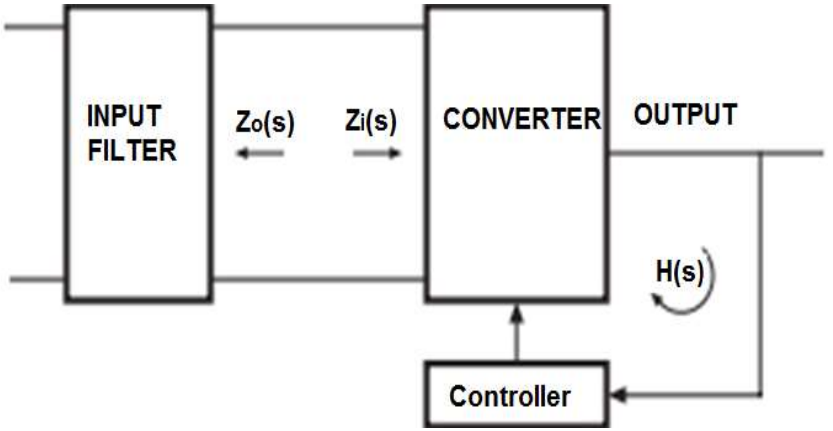
Advanced control techniques: Switching frequency spreading



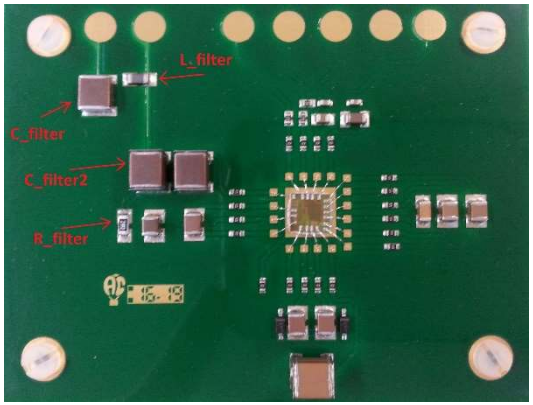
$$Extra\ spectral\ attenuation\ (dB) = 10 * \log[(f_{SW} * \delta)/(f_{DITHER}/n)]$$

Advanced control techniques: Anti-EMI filter





The design of anti-EMI filter aware of input converter impedance allows reducing x 3 the size of the filter components and avoids instability

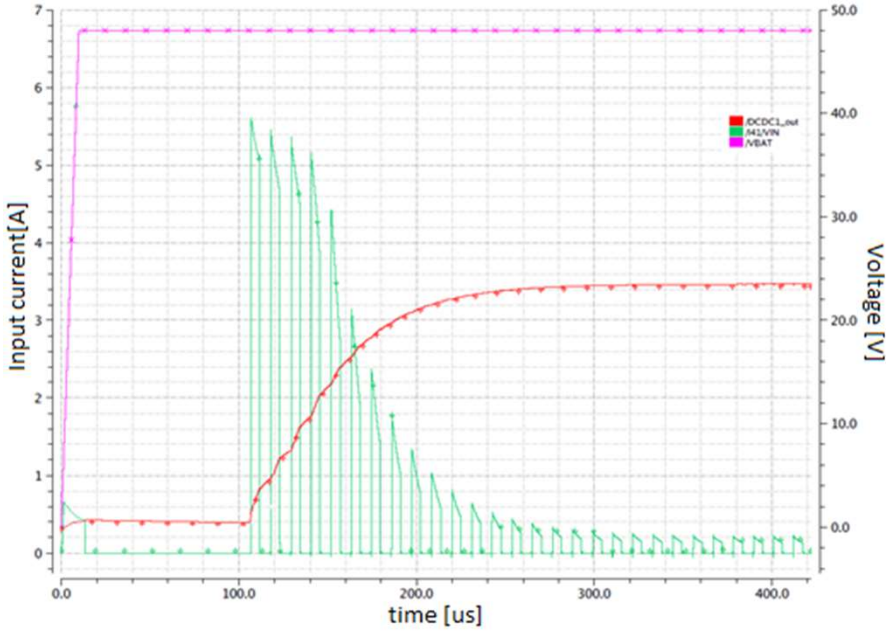


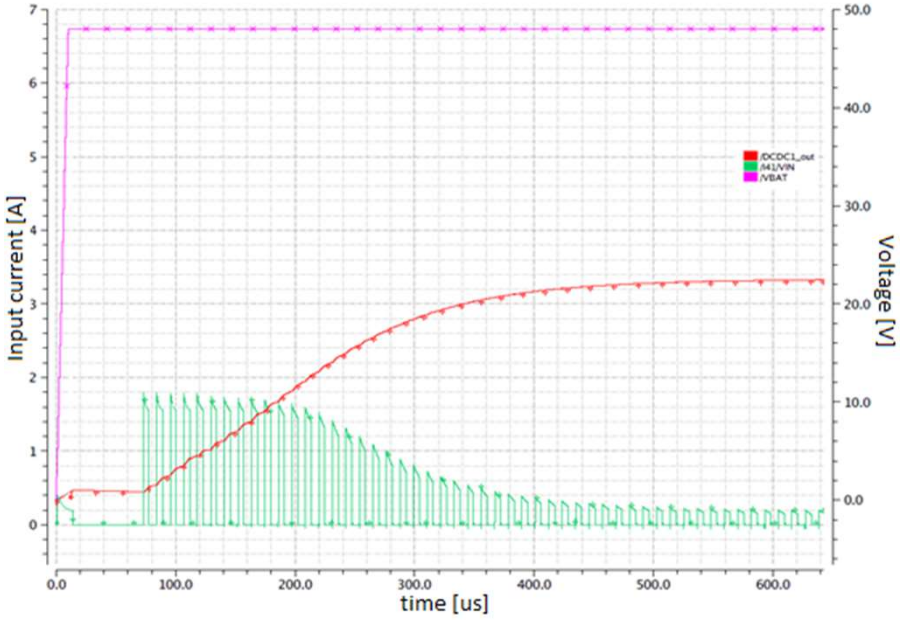
	Set-up		EMI measurement results	
	$V_{battery}$,[V]	I_{load}, [mA]	Freq.peak., [kHz]	Amplitude, [dBV]
This work	8	0-300	180	-84, -74.8, -65.4
	12	0-300	180	-87.2, -77.4, -69.8
	24	0-300	180	-77.8, -77.2, -75.4
	48	0-300	160	-74.4, -76.4, -71.4
	60	0-300	100	-71.4, -63, -57.8
[TI]	30	1600	10	-47.5

Advanced control techniques: Soft-start

Input current without/with soft-start modality (the current peaks, represented from green signal, are reduced by 3 times).

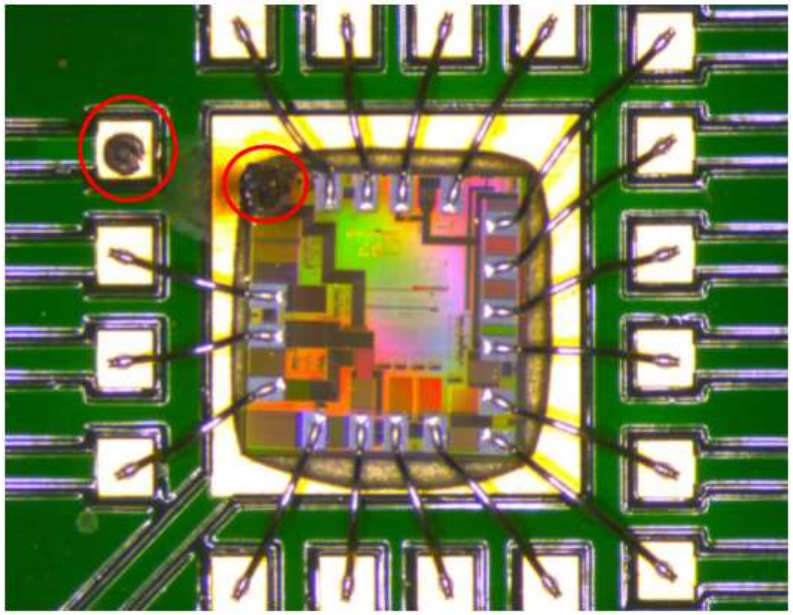
HV-MOS are realized as multiple parallel devices, activated according to a proper sequence when starting to avoid high in-rush currents





Advanced control techniques: Soft-start

Without soft-start chip can be damaged by high current peaks at device start



	Conducted EMI reduction	Radiated EMI reduction	Could be integrated	Low design effort	Low cost
EMI filter	+ + +	-	- -	- -	- -
SKIP control	+ +	+ +	+ + +	+	+ +
Soft-Start technique	+	+	+ + +	-	+

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Outline

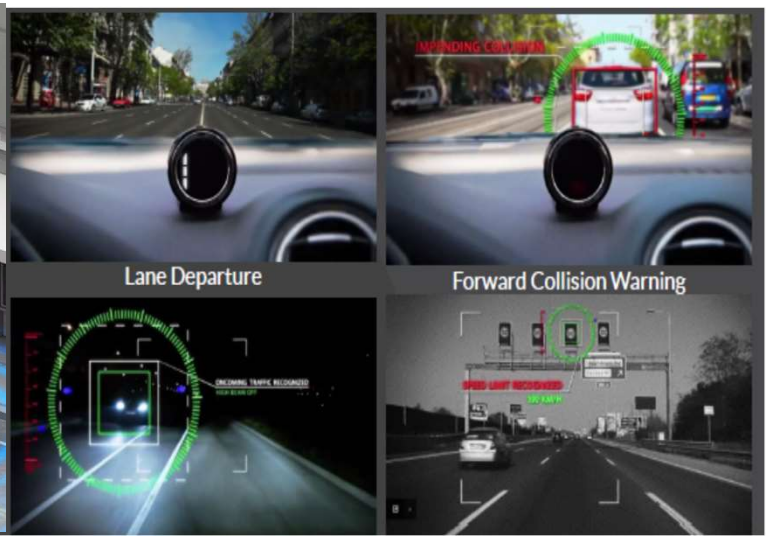
Part I

- Societal, economical and technical challenges of autonomous/connected vehicles and intelligent transport systems (ITS)
- CAS for remote sensing (Radar, Lidar) in smart vehicle & ITS
- Sensing technology & CAS for navigation
- CAS for connected cars: V2X receiver in low-cost CMOS

Part II

- CAS for connected cars: cryptographic HW accelerators
- eHPC (embedded High Performance Computing) needs of autonomous and connected cars
- New computing arithmetic (Posits) for DNN acceleration
- Mixed-signal ICs for smart vehicles
- Conclusions

Conclusions & on-going activities



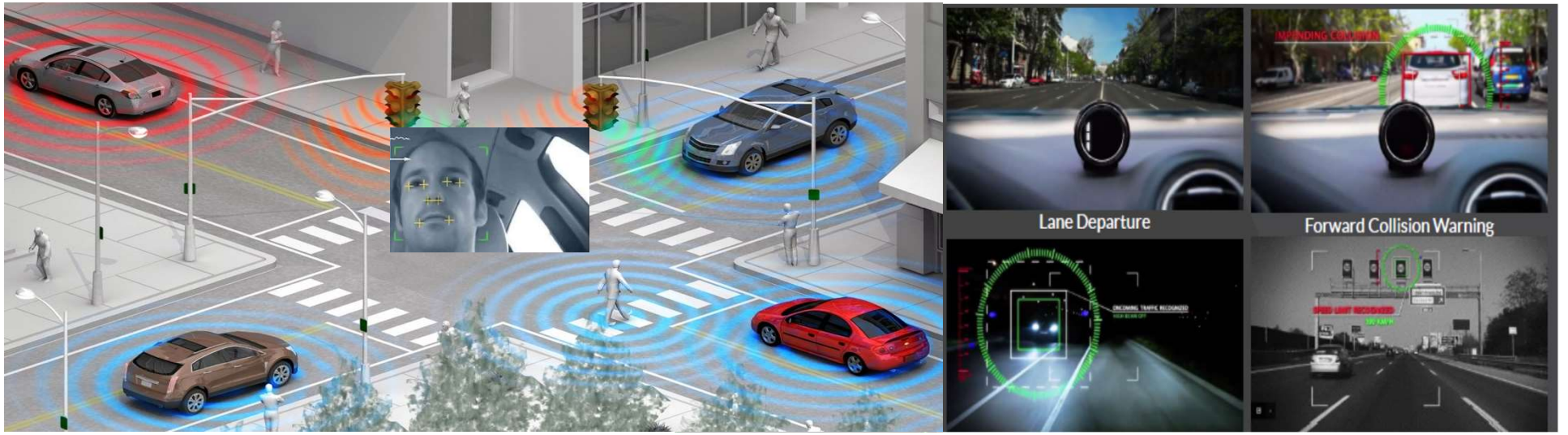
Smart vehicles and ITS are a huge R&D field for I&M

Minimizing bias and random errors in intertial sensors

Fusion of Radar, cameras, Lidar & intertial sensors for ADAS
New fusion algorithms, compact and low-cost radar/lidar, secure in-vehicle networks, on-board MPSoCs in harsh environments, high SIL, HMI & MMI

Sensing technologies for natural Human Machine Interfacing & contactless biometric measurements for fatigue/attention detection

Conclusions & on-going activities



V2X (802.11p) and Cellular-V2X (4GLTE/5G) wireless transceivers
robust and secure links, guaranteed QoS --> integrated security, TSCH/FH, MIMO transceivers, high RX sensitivity, high TX efficiency, beamforming, opportunities at mm-waves, cybersecurity HW accelerators, convergence with 5G (www.5gaa.org)

HW accelerators for ML and DNN for sensor fusion & classification

Innovative acquisition, control and actuations units
for BMS, power converters, distributed sensors/actuators, 3D integration opportunities, EMC/thermal/electrical measurements

Thanks for your attention

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IEEE CASS School “Circuits and Systems for IoT”,
Porto Alegre, Brazil, 5-9 Aug. 2019