

# FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES

THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION'S HORIZON 2020 RESEARCH AND INNOVATION PROGRAMME UNDER GRANT AGREEMENT NO 826647



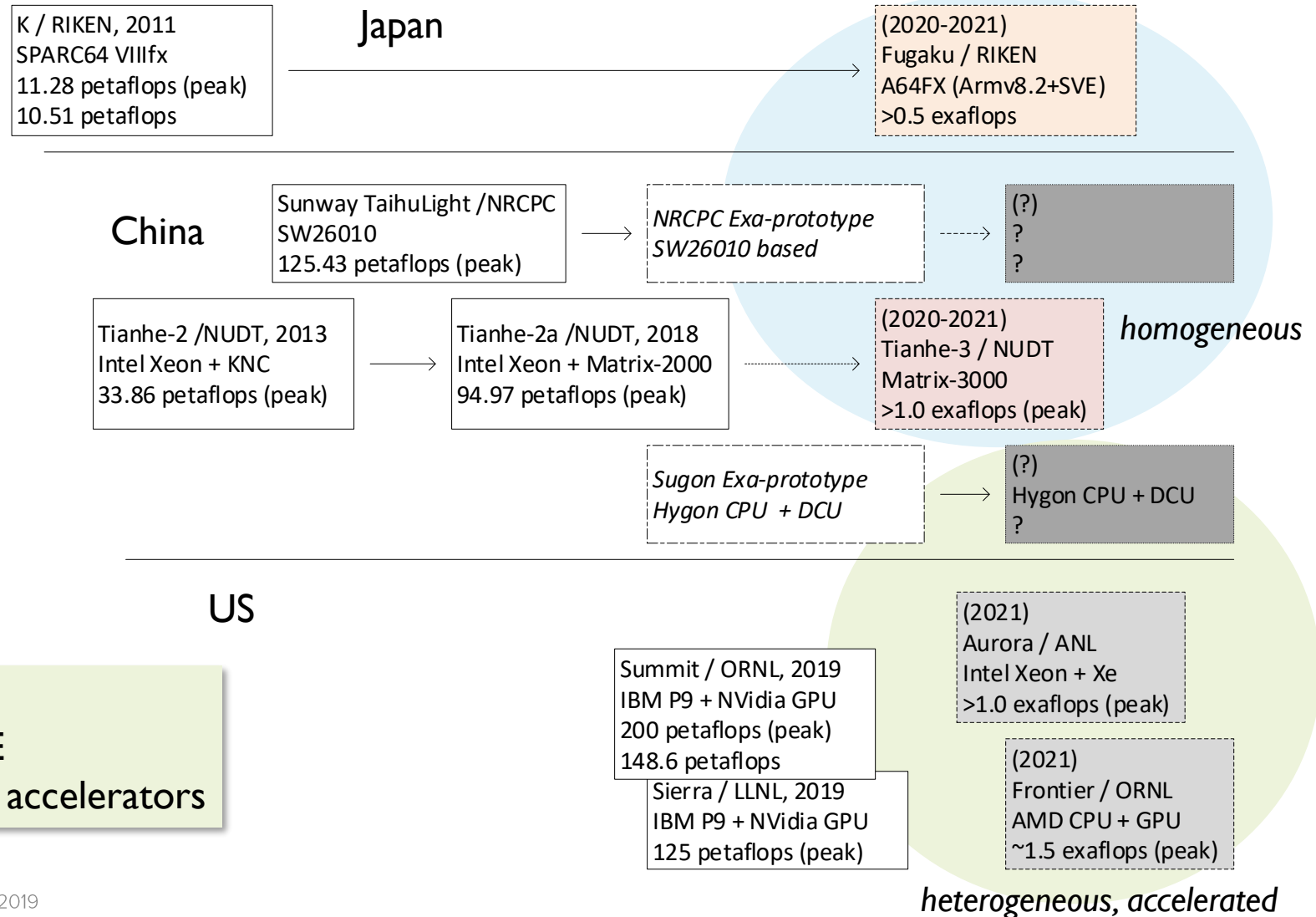


# EPI INTRODUCTION

ANDREA BARTOLINI (WP3 LEADER)

# RACE TO EXASCALE

- CPU architecture choice
  - x86 + accelerator (heterogeneous)
  - Arm/SVE (homogeneous)
  - Others



EPI takes 2-step approach  
 step#1 : homogeneous with Arm core+SVE  
 step#2 : heterogeneous with additional EPI accelerators

# 53<sup>RD</sup> EDITION OF THE TOP500 LIST (JUNE 2019)

- Top#1 today:
  - 0.2 10<sup>18</sup> Flop/s Peak
  - It is 1/5 of Exascale level of performance

## ■ Users:



#1-#2: US



#3-#4: China

## ■ Processor design & technology:

Chip	Design	Manuf.
IBM POWER9		
NVIDIA Volta GV100		
Sunway SW26010		
Intel Xeon E5		

Rank	Site	System
1	DOE/SC/Oak Ridge National Laboratory United States	<b>Summit</b> - IBM Power System AC922, IBM POWER9 22C 3.07GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband IBM
2	DOE/NNSA/LLNL United States	<b>Sierra</b> - IBM Power System S922LC, IBM POWER9 22C 3.1GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband IBM / NVIDIA / Mellanox
3	National Supercomputing Center in Wuxi China	<b>Sunway TaihuLight</b> - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway NRCP
4	National Super Computer Center in Guangzhou China	<b>Tianhe-2A</b> - TH-IVB-FEP Cluster, Intel Xeon E5-2692v2 12C 2.2GHz, TH Express-2, Matrix-2000 NUDT

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How to bring  
back Europe into  
processor race ?

# WHY EUROPE NEEDS ITS OWN PROCESSORS

- Processors now control almost every aspect of our lives
- Security (back doors etc.)
- Possible future restrictions on exports to EU due to increasing protectionism
- A competitive EU supply chain for HPC technologies will create jobs and growth in Europe
- Sovereignty (data, economical, embargo)

**Amazon exec and Super Micro CEO call for retraction of spy chip story**

*'[Tim Cook] is right. Bloomberg story is wrong about Amazon, too.'*



**NSA May Have Backdoors Built Into Intel And AMD Processors**



**The US Cloud Act v The EU's GDPR - Data Privacy & Security**

**A group of researchers showed how a Tesla Model S can be hacked and stolen in seconds using only \$600 worth of equipment**

**A jet sale to Egypt is being blocked by a US regulation, and France is over it**



**Car hacking remains a very real threat as autos become ever more loaded with tech**

Image sources:

<https://www.theverge.com/2018/10/22/18011138/china-spy-chip-amazon-apple-super-micro-ceo-retraction>  
<https://www.businessinsider.in/a-group-of-researchers-showed-how-a-tesla-model-s-can-be-hacked-and-stolen-in-seconds-using-only-600-worth-of-equipment/articleshow/65761310.cms>  
<https://eu.freem.com/story/money/2018/01/13/car-hacking-threat/1028270001/>  
<https://www.eteknix.com/nsa-may-backdoors-built-intel-amd-processors/>  
<https://www.pearsestrust.ie/blog/the-us-cloud-act-v-the-eus-gdpr-data-privacy-security>  
<https://www.defensenews.com/global/europe/2018/08/01/a-jet-sale-to-egypt-is-being-blocked-by-us-regulation-and-france-is-over-it/>

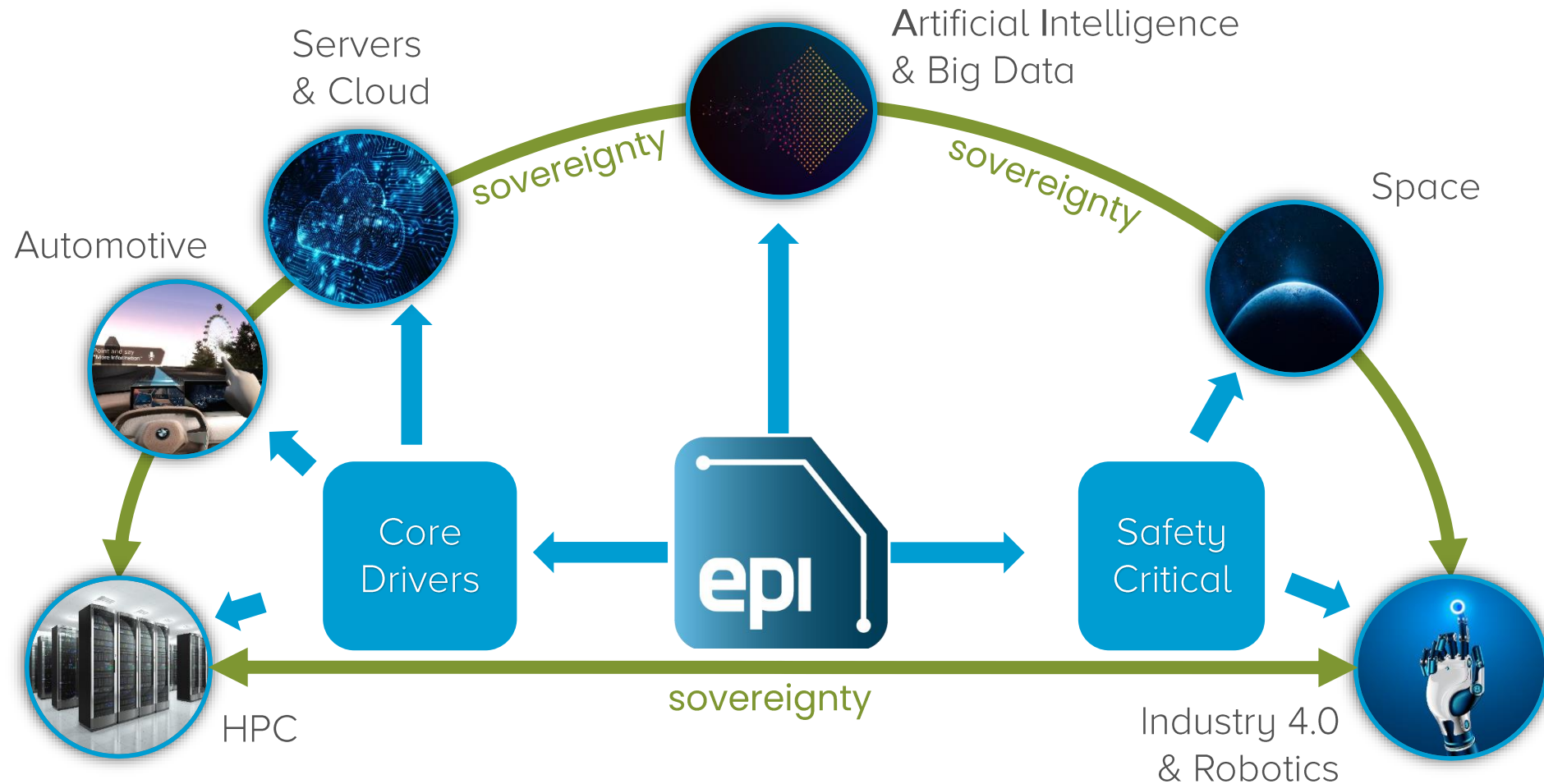
# EUROPEAN PROCESSOR INITIATIVE

- High Performance General Purpose Processor for HPC
- High-performance RISC-V based accelerator
- Computing platform for edge and autonomous cars
- Will also target the AI, Big Data and other markets in order to be economically sustainable

## Overall objective

Develop a complete EU designed high-end microprocessor, protecting our continent from embargos and external data control

# SCALABILITY ALLOWS WIDE MARKET POTENTIAL COVERAGE





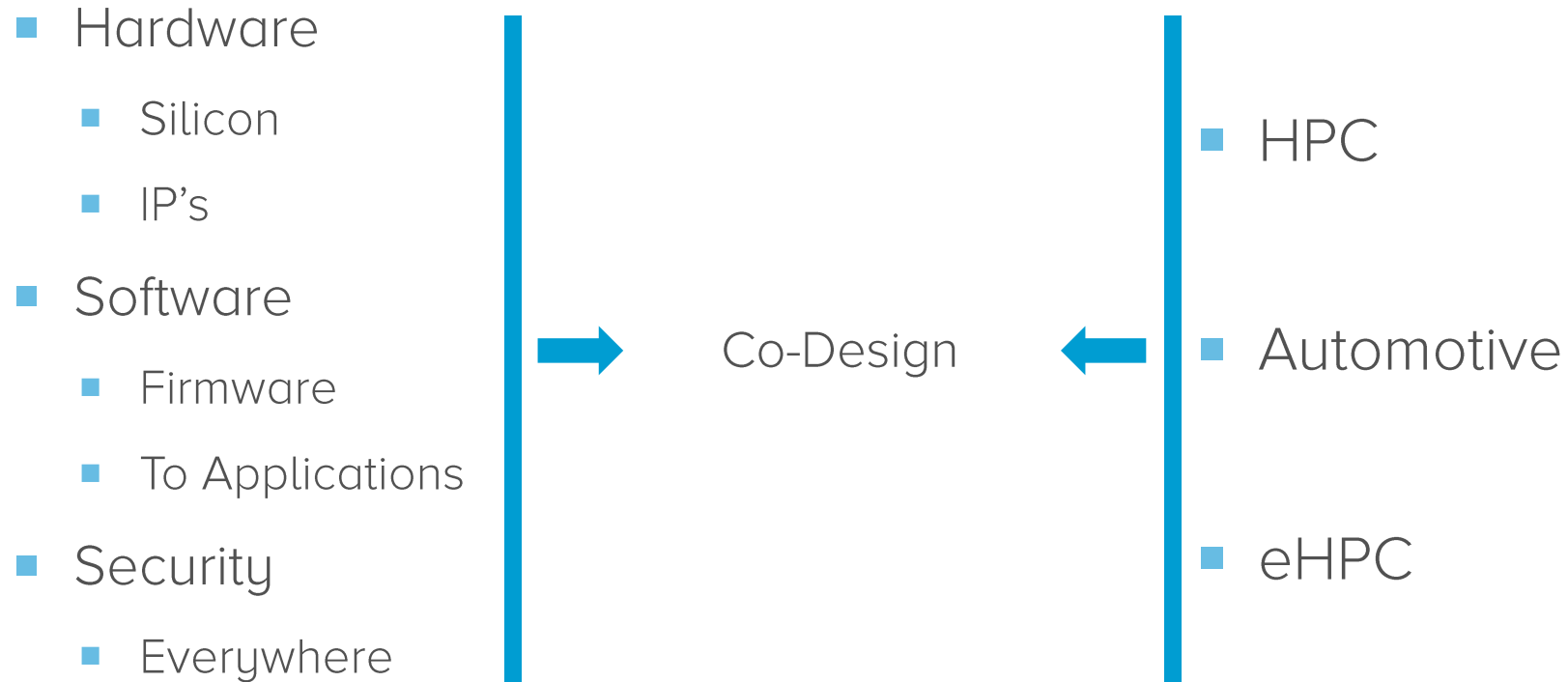
# EPI TODAY

- Official kick off on Dec-2018
- Our Story is known on a WW basis with keynotes and requests from all EU countries, USA, Japan, Singapore and China
- Further Market analysis and business exploration have confirmed 2 compelling interests on top of the high-End processor for HPC and automotive markets
  - EPI End2End Security
  - EPI Common Platform for AI, Crypto and Quantum startups acceleration

# EPI: 27 PARTNERS FROM 10 EU COUNTRIES



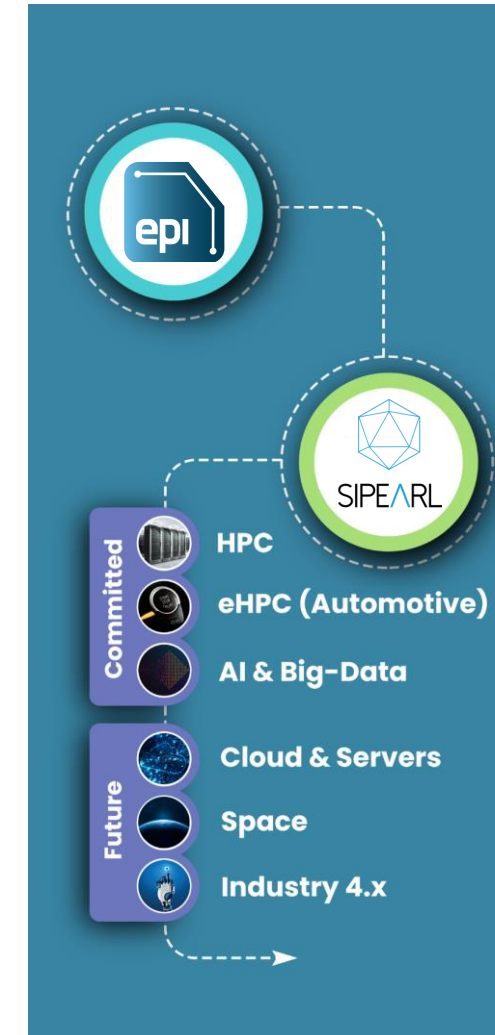
# EPI KEY ELEMENTS



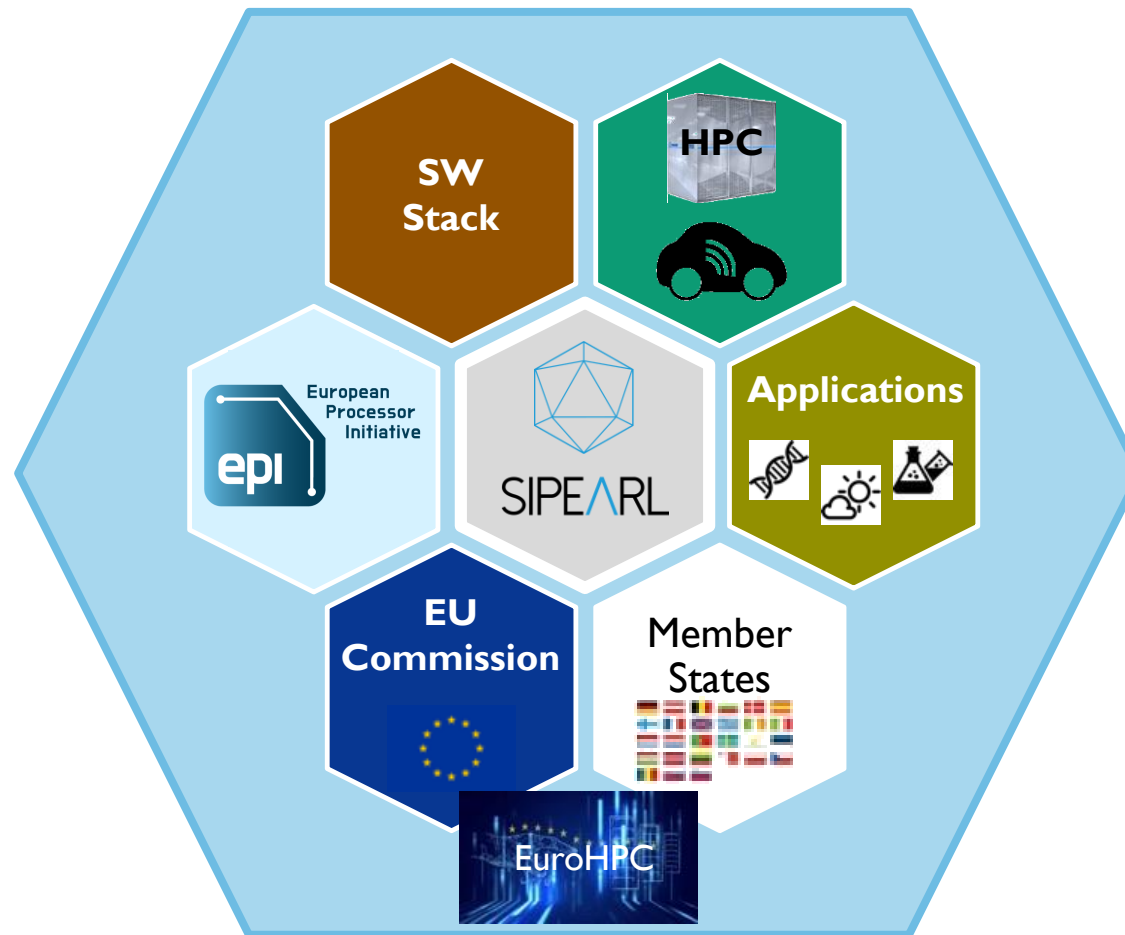
# FROM IPR TO PRODUCTS

## FROM EPI TO SIPEARL

- SIPEARL is
  - Incorporated in EU (France)
  - the industrial and business ‘hand’ of EPI
  - the Fabless company
- licence of IPs from the partners
- develop own IPs around it
- licence the missing components from the market
- Raise in equity the missing budget (~100M€)
- generate revenue from both the HPC, IA, server and eHPC markets
- integrate, market, support & sell the chip
- work on the next generations



# EPI & SIPEARL ARE THE EUROHPC INDUSTRIAL CORNERSTONE



April 2016

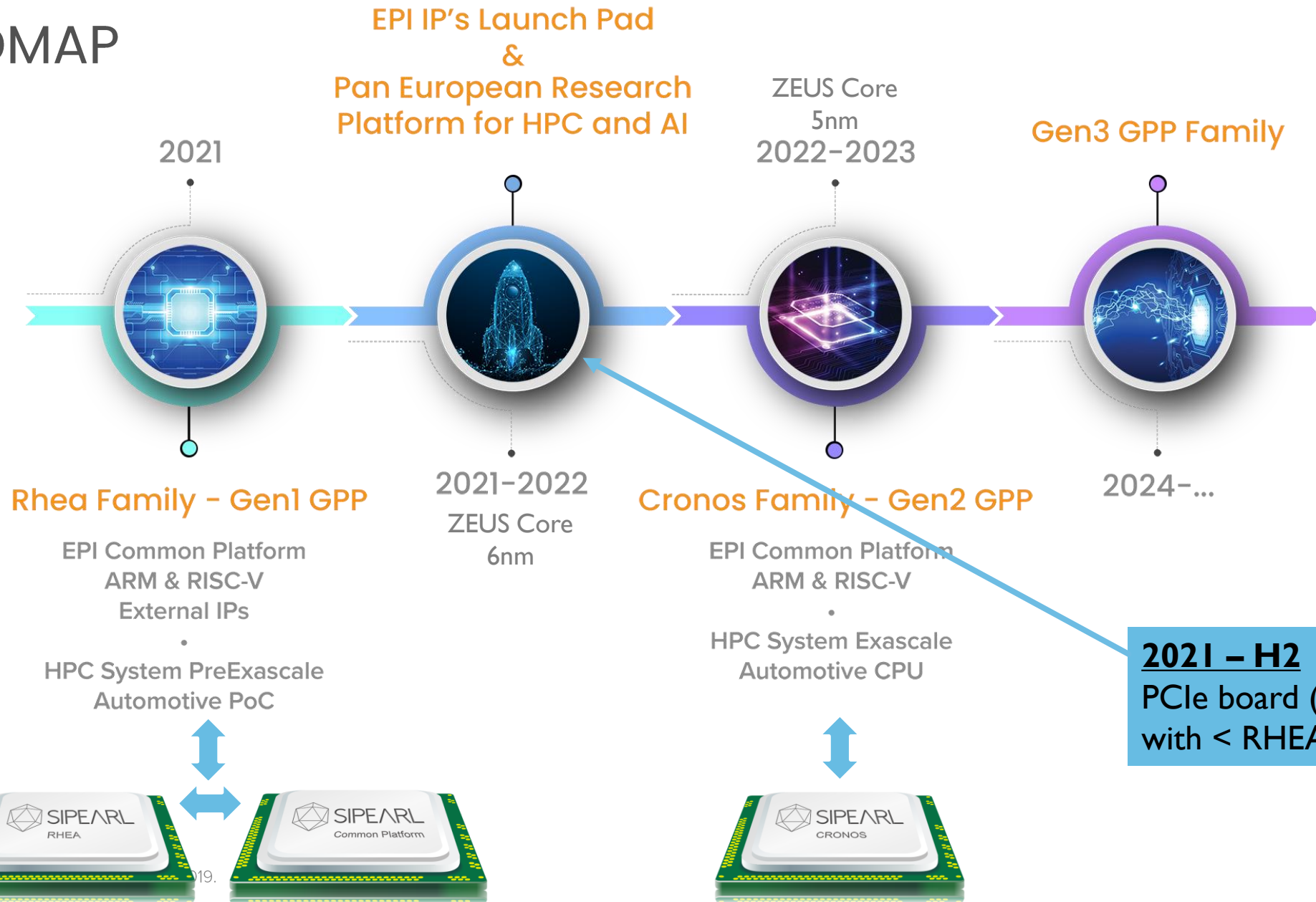


- « foster an HPC ecosystem capable of developing new European technology such as low power HPC chips »
- « ...acquisition of two co-design prototype exascale supercomputers in 2020, at least one based on European technology, which will rank in the Top3 of the world »

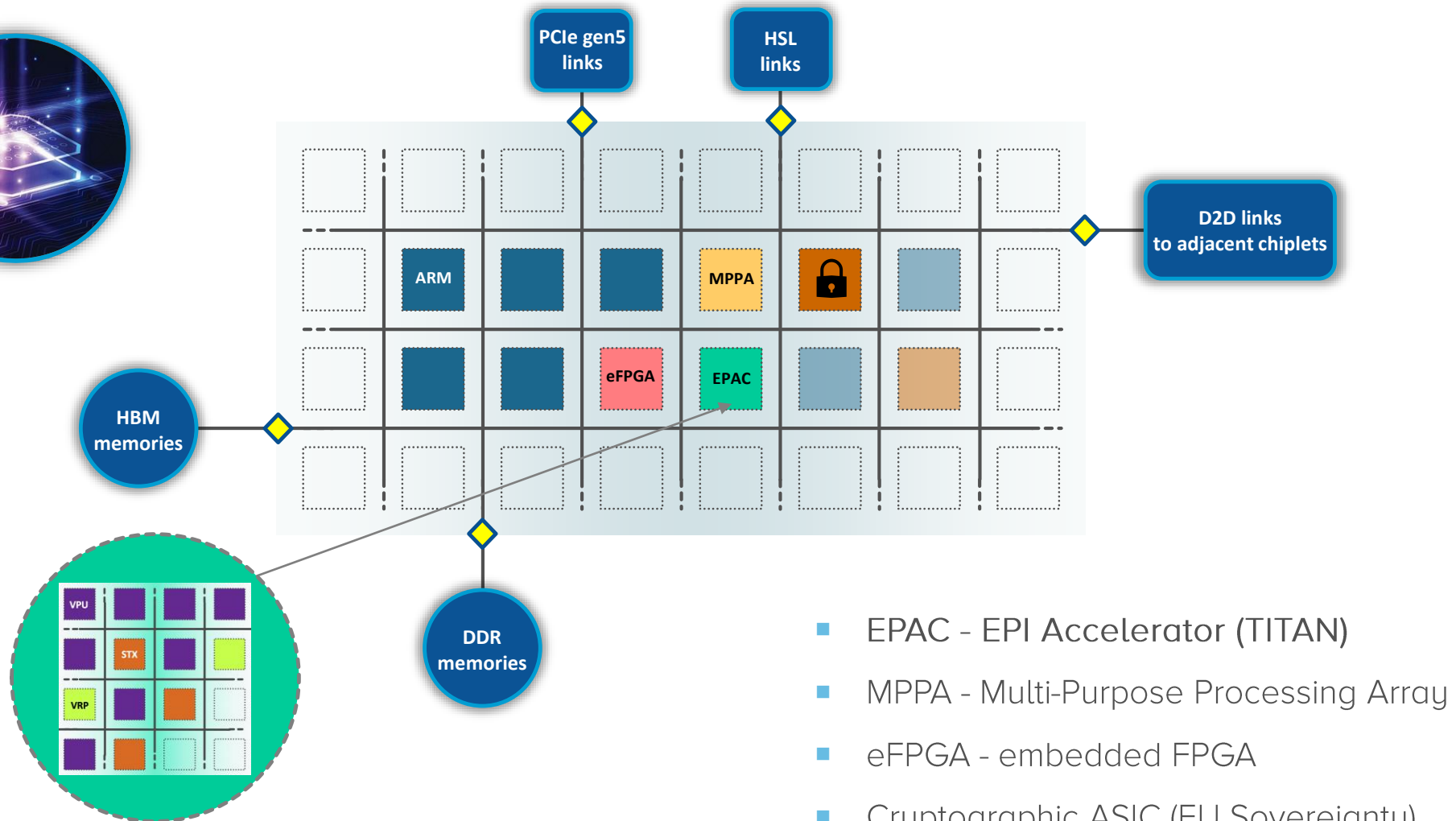
# ROADMAP & TECHNOLOGY



# ROADMAP



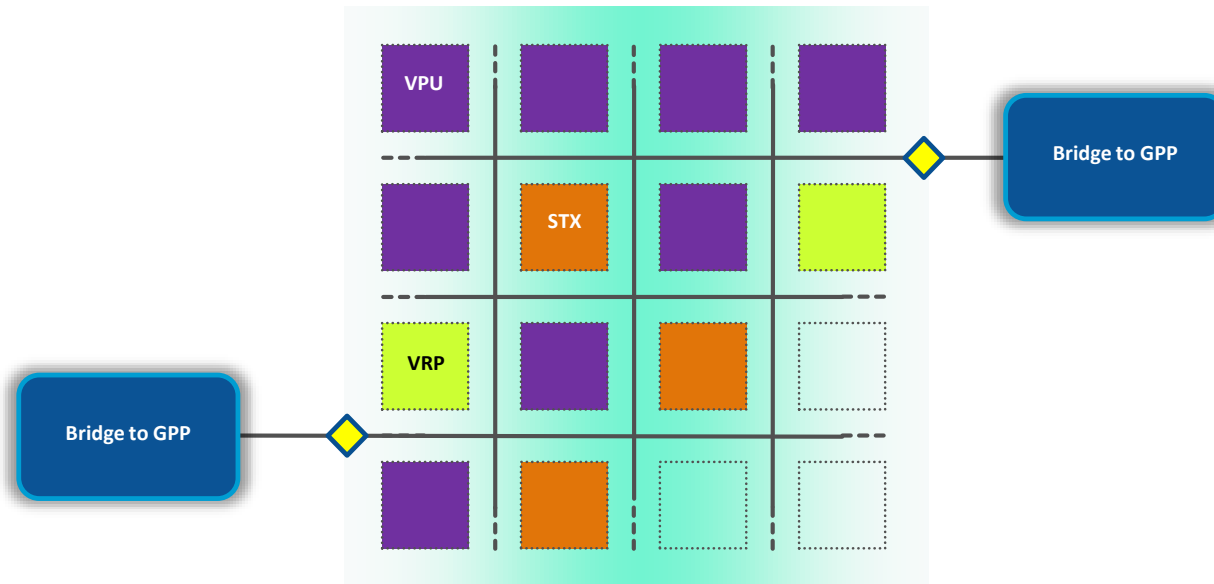
# GPP AND COMMON ARCHITECTURE



- EPAC - EPI Accelerator (TITAN)
- MPPA - Multi-Purpose Processing Array
- eFPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)

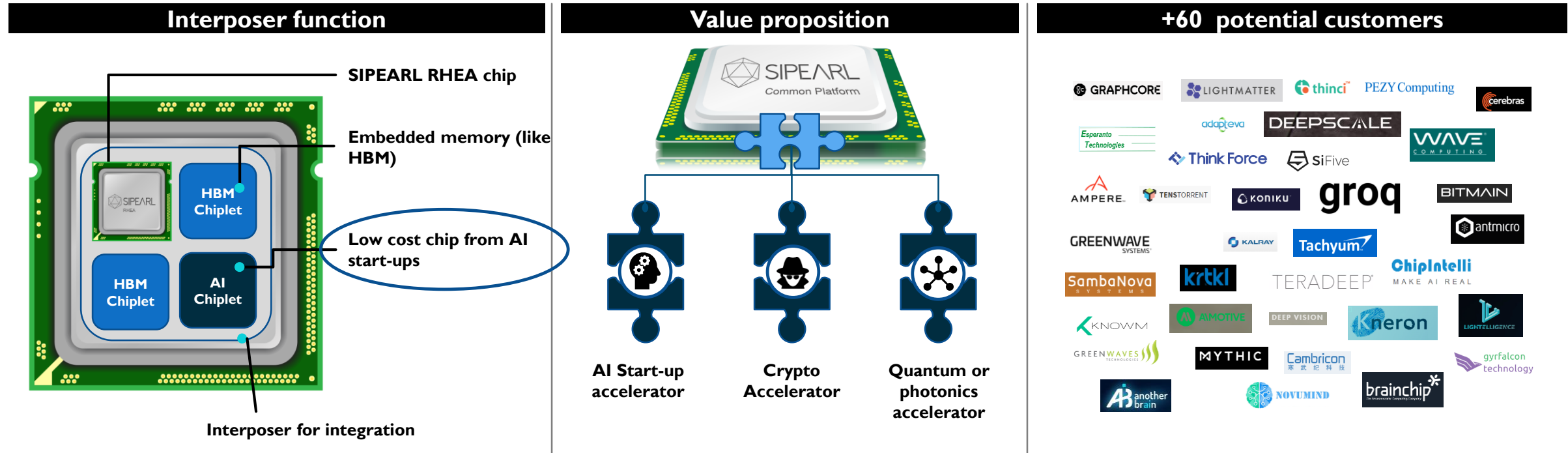


# EPAC – RISC-V ACCELERATOR



- EPAC – TITAN = EPI Accelerator
- VPU – Vector Processing Unit (plan of record)
- STX – Stencil/Tensor accelerator (PoR)

# COMMON PLATFORM VISION: WE ACCELERATE ACCELERATORS



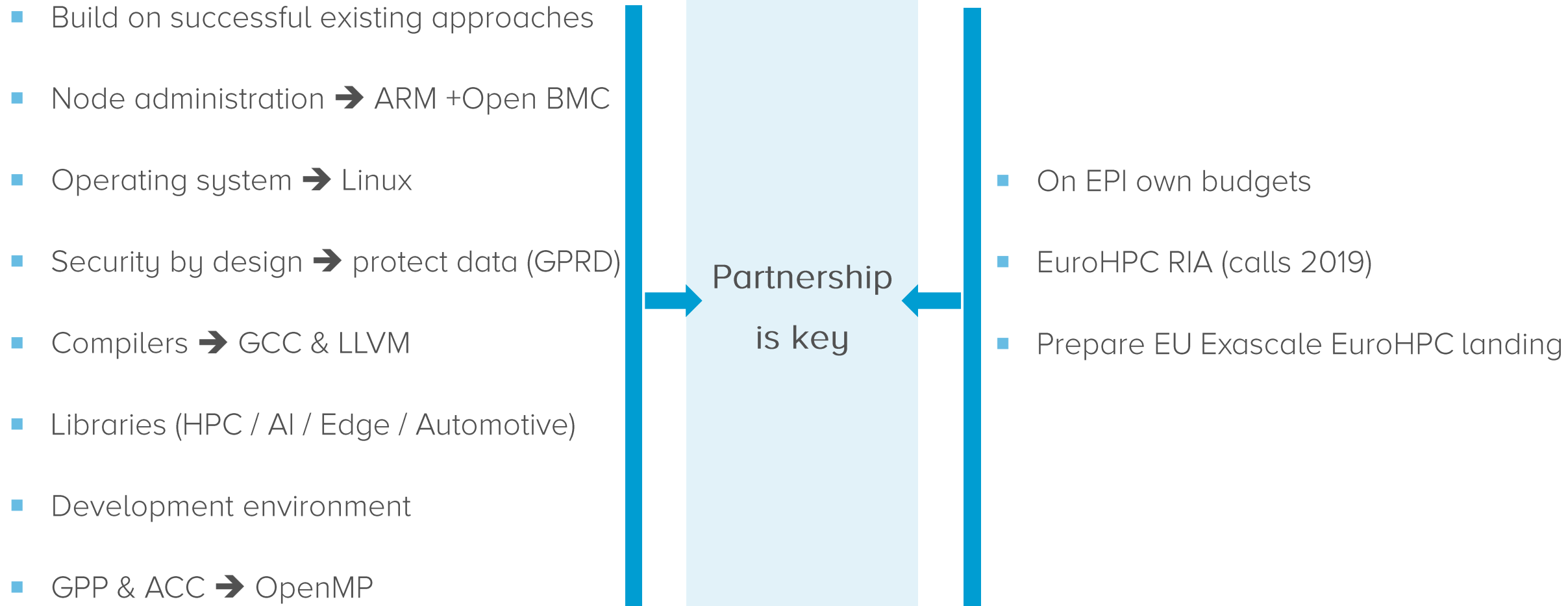
COMMON PLATFORM HAS THE POTENTIAL TO BECOME THE EUROPEAN I/O STANDARD DATA-PROCESSING



# SOFTWARE

## TECHNOLOGY

# HOLISTIC APPROACH



# EPI SOFTWARE AMBITIONS IN HPC

- Complement the already existing software to supply an entire HPC production stack
- **Deployment/administrative side**
  - Securing the node
  - Power managing the node
  - Booting the node
  - (Remote) controlling the node
  - Running a Linux distribution on the node
  - Managing various nodes in a large system
  - Monitoring & accounting various nodes in a large system
- **End-user side**
  - Compiling software for the General Purpose Processor
  - Compiling software for the Accelerators
  - Combining the use of GPP & Accelerators in a software
  - Leveraging standard libraries tuned for the node
  - Running the software on a node
  - Running the software on multiple nodes in a system
- **Automotive (edge-HPC) requirements**
  - Security, power
  - Predictable performance for autonomous driving
    - Multiple inputs, complex models

# ARM WW HPC

CPU manufacturer,  
2 server manufacturers,  
“Astra” system at Sandia,  
upcoming system at Stony Brook



Stony Brook University



Hewlett Packard Enterprise



CRAY



Atos



SIPE/ARL



UNIVERSITY OF LEICESTER



University of BRISTOL



GW4

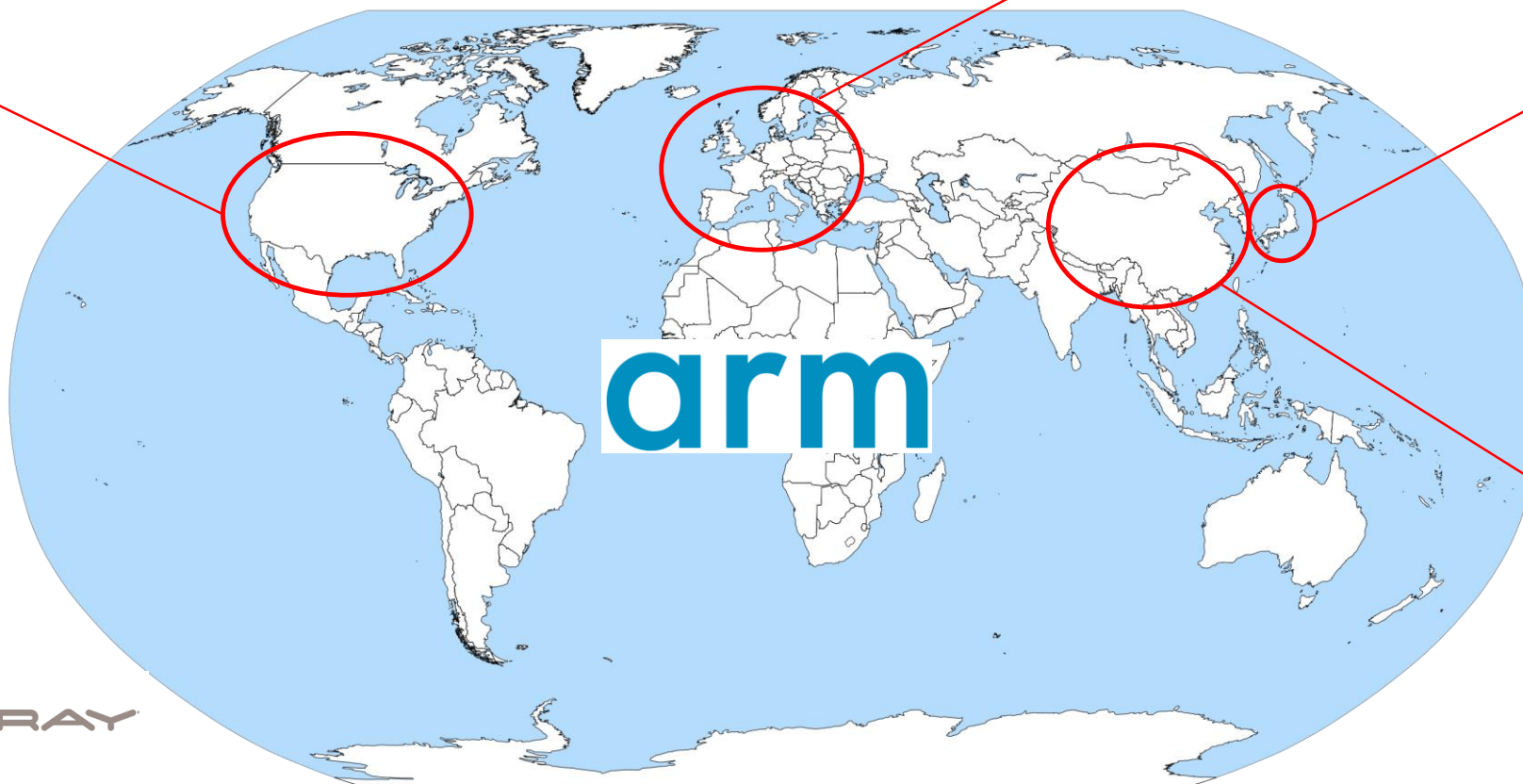
Upcoming CPU manufacturer,  
Server manufacturer,  
system at CEA, UK,  
MontBlanc, EPI



CPU & server manufacturer,  
upcoming “Fugaku” system



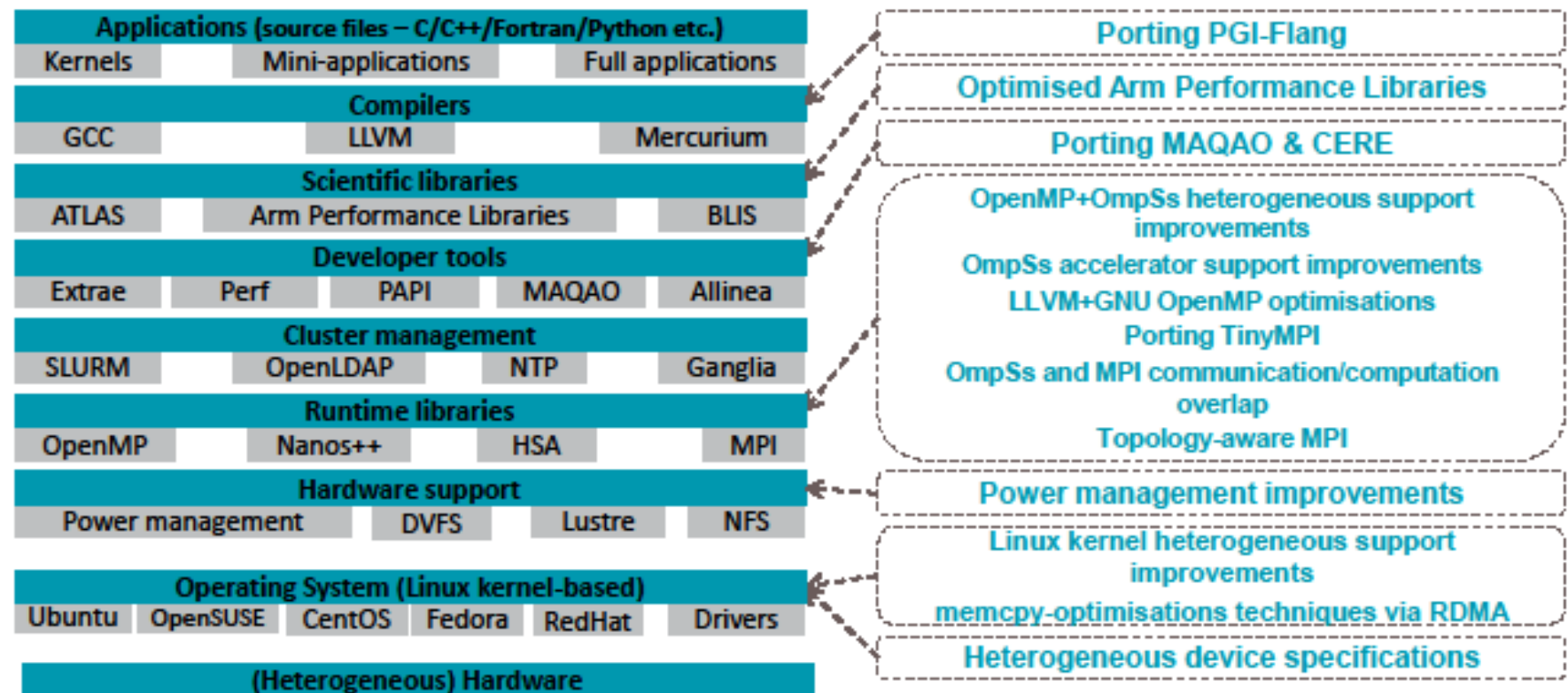
CPU & server manufacturer  
[geopolitical issues regarding the license]



# STANDING ON THE SHOULDERS OF SUCCESSFUL EUROPEAN PROJECTS

- Mont-Blanc 3 helped create and stabilize most of the foundations of a full HPC software stack on Arm

## HPC Arm Software Stack

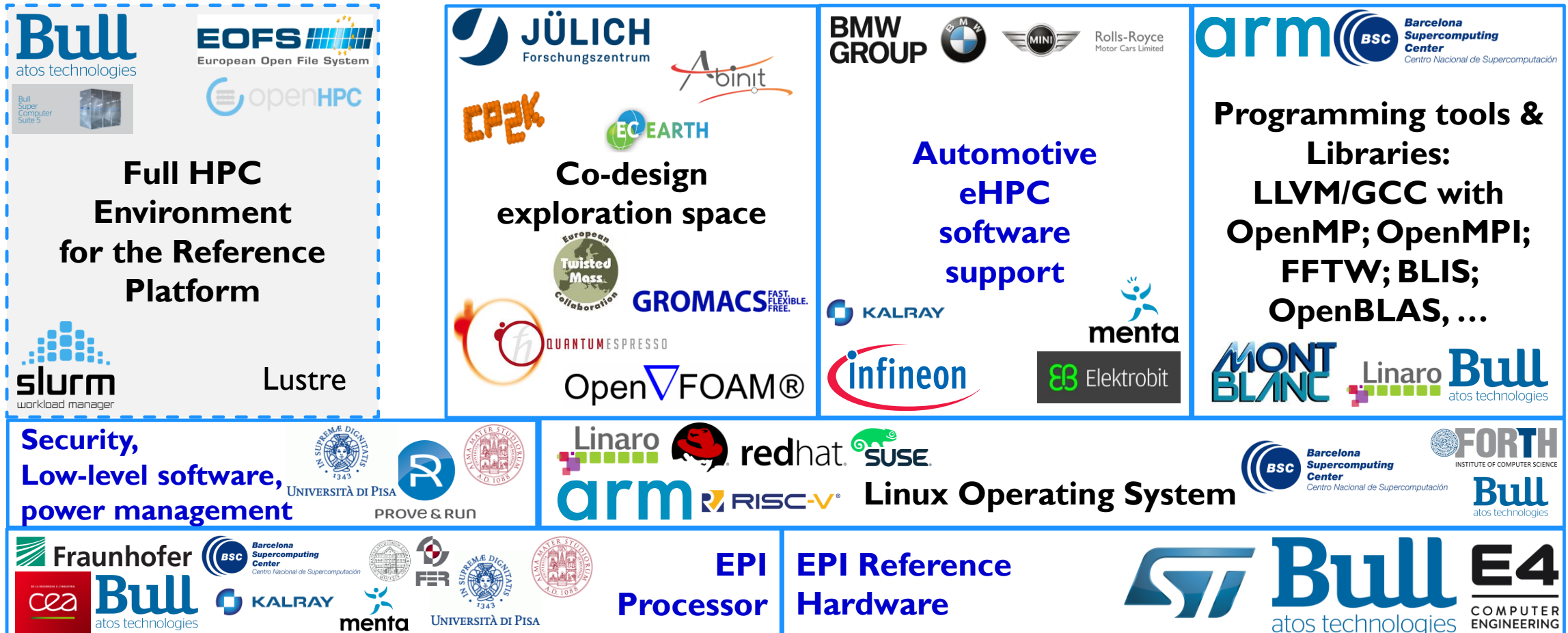


+ Contribution to OpenHPC (from 1.2)



# EPI ECOSYSTEM

(INCLUDING POTENTIAL OUTSIDE PARTNERS)



... and those supporting the ecosystem & EPI, including EPI partners, external partners & OpenSource contributors



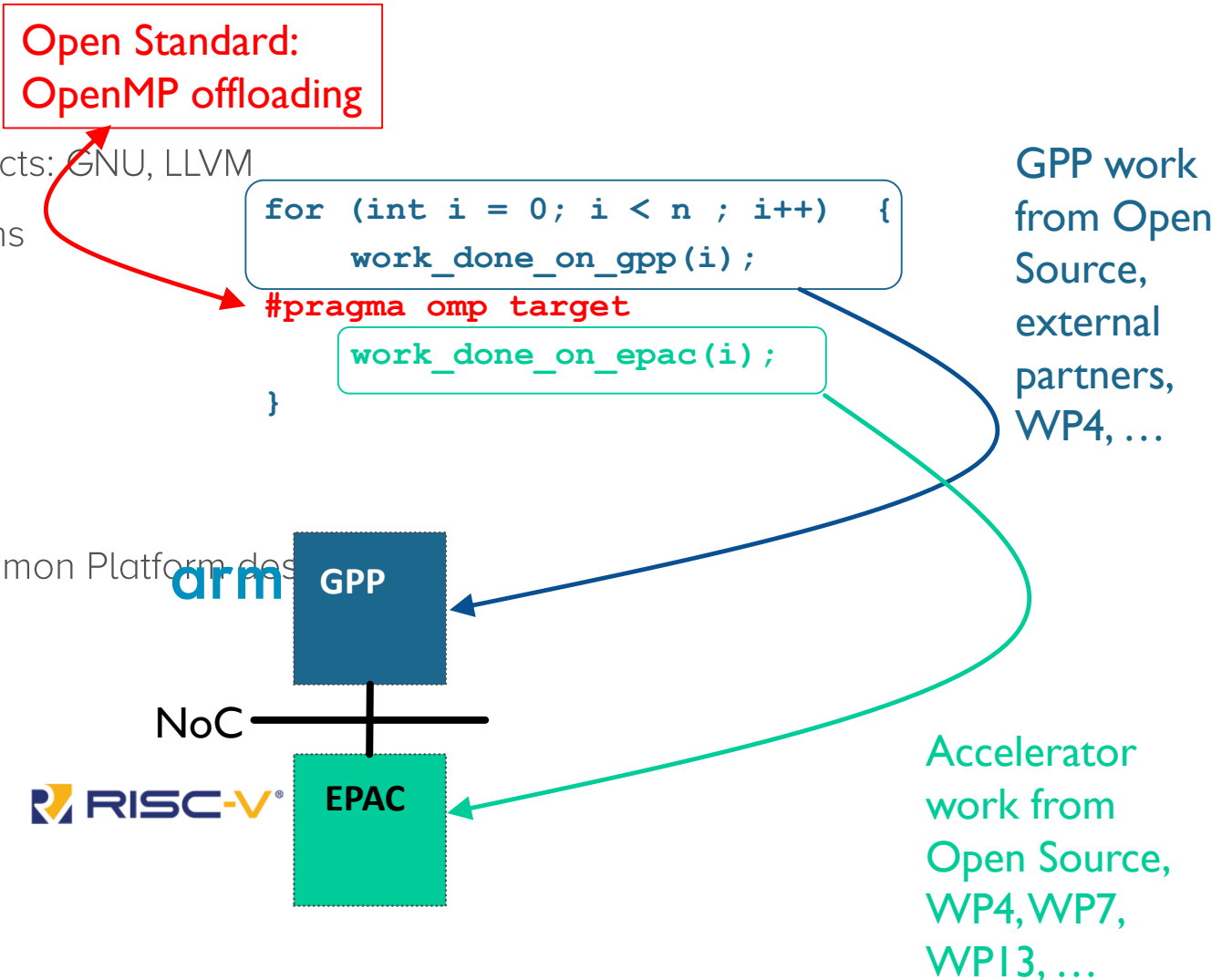
# EXPANDING TO RISC-V



- The RISC-V architecture is used extensively in EPI
  - EPAC accelerator, Power Management, ...
- It is fully open and not reliant on one company for its definition
- The software ecosystem is not yet has developed as the Arm one
  - Mont-Blanc projects were instrumental in maturing the Arm ecosystem
- EPI software work includes work to bring RISC-V closer to the need of a production-ready general-purpose processor
- MPI work on RISC-V & hybrid (WP4)
- OpenMP runtime on RISC-V (WP14, WP7)
  - For offloading & native mode
- Compiler work (WP7, WP14)
  - Including OpenMP SIMD
- Using RISC-V in the industrial world as a full-fledged, linux-capable processor and not just a microcontroller
  - Real-life use to strengthen the software

# END-USER

- Compiling, combining
  - Leveraging work from existing Open Source projects: GNU, LLVM
  - Choosing open standard over proprietary solutions
    - Emphasis on OpenMP in the project
    - OpenVX for automotive in WP20
  - Working with external partners
    - Arm work in LLVM & libraries for the GPP
  - EPI adding missing pieces to fully exploit the Common Platform design
    - Better vectorization in EPAC (WP14)
    - OpenMP offloading (WP4, WP7, WP14, WP20)
    - OpenMP SIMD (WP14 for R5)



# END-USER

- Leveraging, running
  - Tuned libraries to support end-user – optimized FFTs, Linear Algebra, etc. on GPP & EPAC (WP4, WP14)
  - Tuned runtimes for the compiler & the OpenMP support, kernel support (WP4, WP7, WP14)
  - Multi-node support by expanding OpenMPI support for homogeneous & heterogeneous computations (WP4, WP14)
  - Enable PGAS programming model via Global Address Space Programming Interface (GASPI, WP14)
- And also third-party work enabled for EPI, building on the Mont-Blanc work
  - Arm HPC compiler
  - Arm Performance Libraries
  - UVSQ Maqao
  - OpenHPC initiative
  - ...

# SOFTWARE COMPONENTS

- Full boot code for the processor
  - Fully secure boot, power management, UEFI
- Linux kernel support
  - Linux on GPP
  - Linux on generalist accelerator
  - Drivers for built-in hardware
- Compilers for GPP
  - LLVM and GCC
- Compilers for Accelerators
  - LLVM and/or GCC (accelerator-dependent)
  - eFPGA, MPPA-specific toolchains
- Compilers for offload (GPP + accelerator)
  - LLVM and/or GCC (accelerator-dependent)
  - Integrated in the GPP compilers
- Runtimes & drivers for the supported native and offloaded mode
  - OpenMP target
- Libraries for the supported native and offloaded mode
  - MPI GPP, MPI accelerator
  - Numerical libraries GPP, numerical libraries accelerator
- Automotive-specific components
- And OpenSource software components

# CONCLUSION



# EPI NEXT CHALLENGES

## Build on existing IP and w. communities

- Risk minimized by leveraging existing work
  - Open Source, previous projects, external partners
- Future-proofed by favoring open standards & simpler programming models
- Legacy taken into account to widen the potential user-base

## Close the gap between R&I and industrial products

- Have EPI “delivery and product” oriented while fulfilling its needs for Research and Innovation
  - We need to be ready for production end of 2021
- Face a WW class competition
  - We will not be used because we are “engineered” in EU but because we have the best and cost effective solution
- Re-create a real ecosystem for deep node microelectronics:
  - Engineers
  - IP's
  - ...factories...

# WE NEED YOU!

- EPI needs your help
- EPI will be successful through collaborations
- EPI will be successful through partnership
- EPI needs your expertise
- Key areas of collaboration / partnership
  - Development tools
  - Libraries
  - Applications
- DG-CNECT & EUROHPC want to see more collaboration between EPI and RIA calls
- Contact us!



 European Processor Initiative