

FRAMEWORK PARTNERSHIP AGREEMENT IN EUROPEAN LOW-POWER MICROPROCESSOR TECHNOLOGIES

THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION'S HORIZON 2020 RESEARCH AND INNOVATION PROGRAMME UNDER GRANT AGREEMENT NO 826647



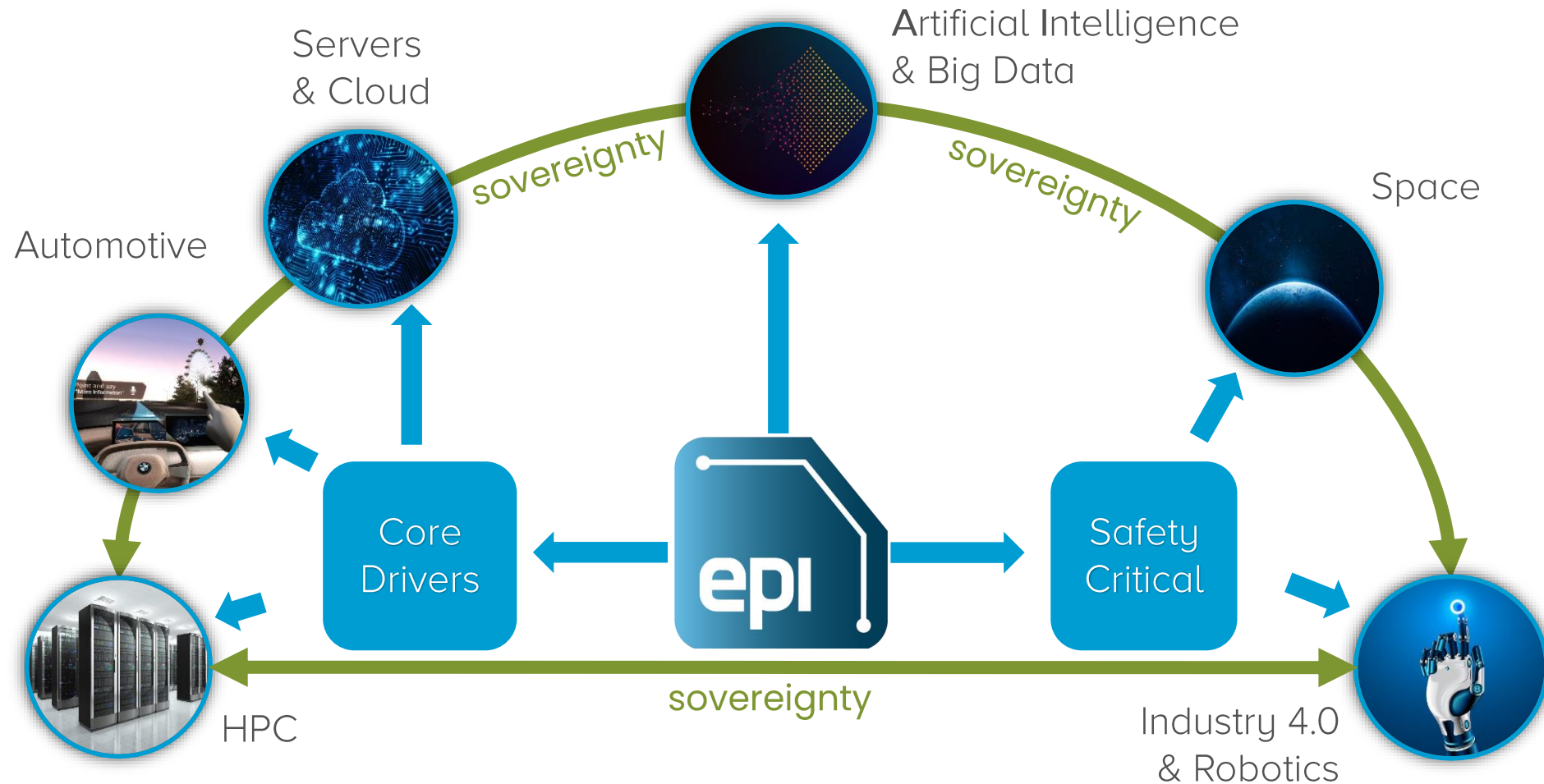
EUROPEAN PROCESSOR INITIATIVE

- High Performance General Purpose Processor for HPC
- High-performance RISC-V based accelerator
- Computing platform for edge and autonomous cars
- Will also target the AI, Big Data and other markets in order to be economically sustainable

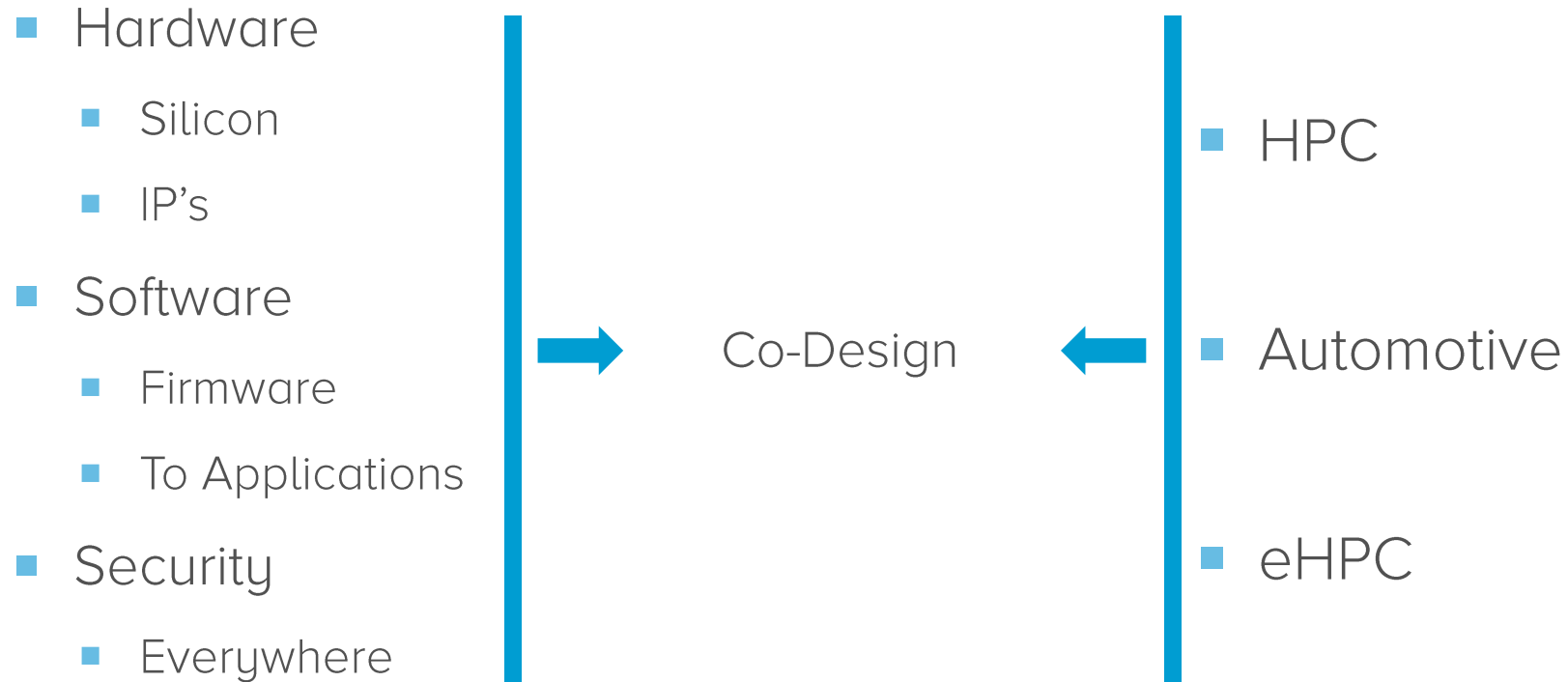
Overall objective

Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments

SCALABILITY ALLOWS WIDE MARKET POTENTIAL COVERAGE

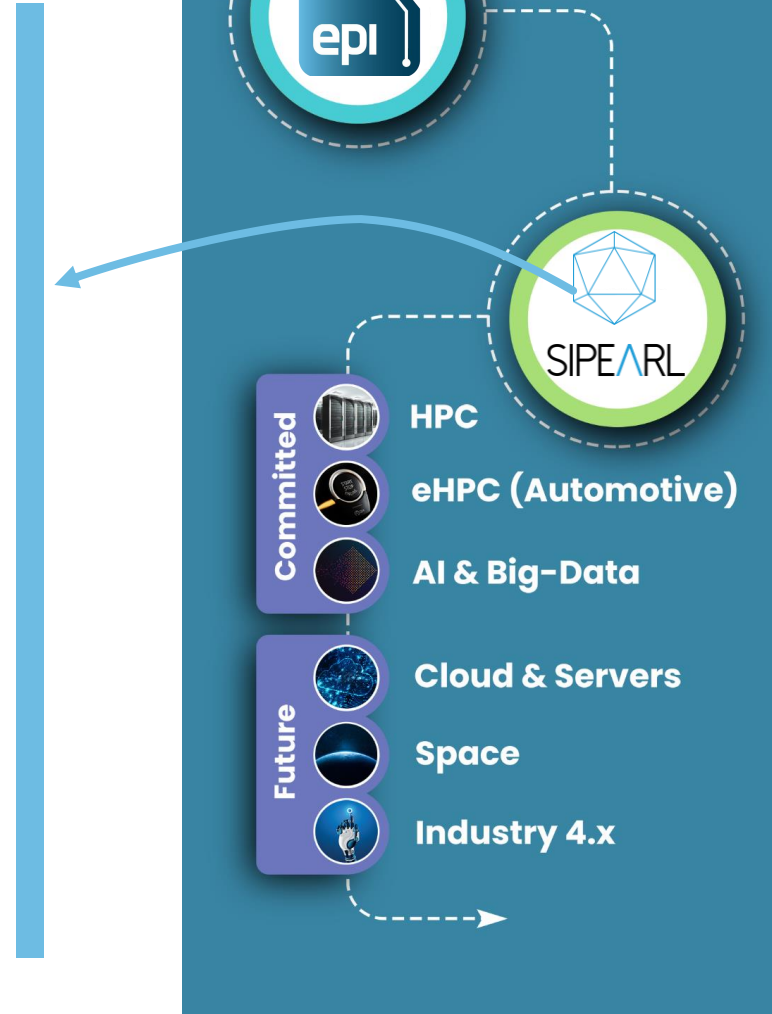


EPI KEY ELEMENTS & GUIDELINES



FROM IPR TO PRODUCTS FROM EPI TO SIPEARL

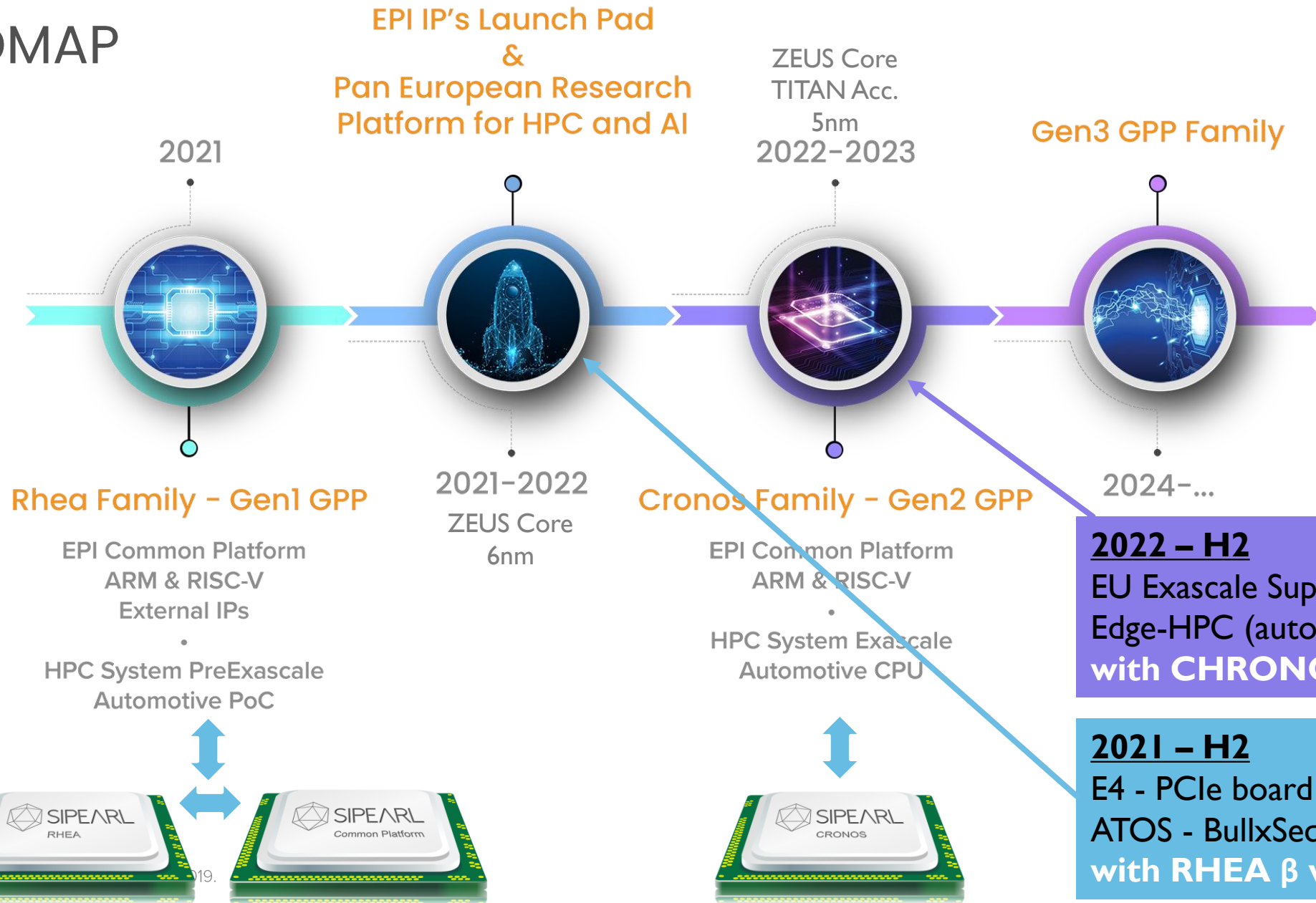
- SIPEARL is
 - Incorporated in EU (France)
 - the industrial and business 'hand' of EPI
 - the Fabless company
- licence of IPs from the partners
- develop own IPs around it
- licence the missing components from the market
- Raise in equity the missing budget (~100M€)
- generate revenue from both the HPC, IA, server and eHPC markets
- integrate, market, support & sell the chip
- work on the next generations



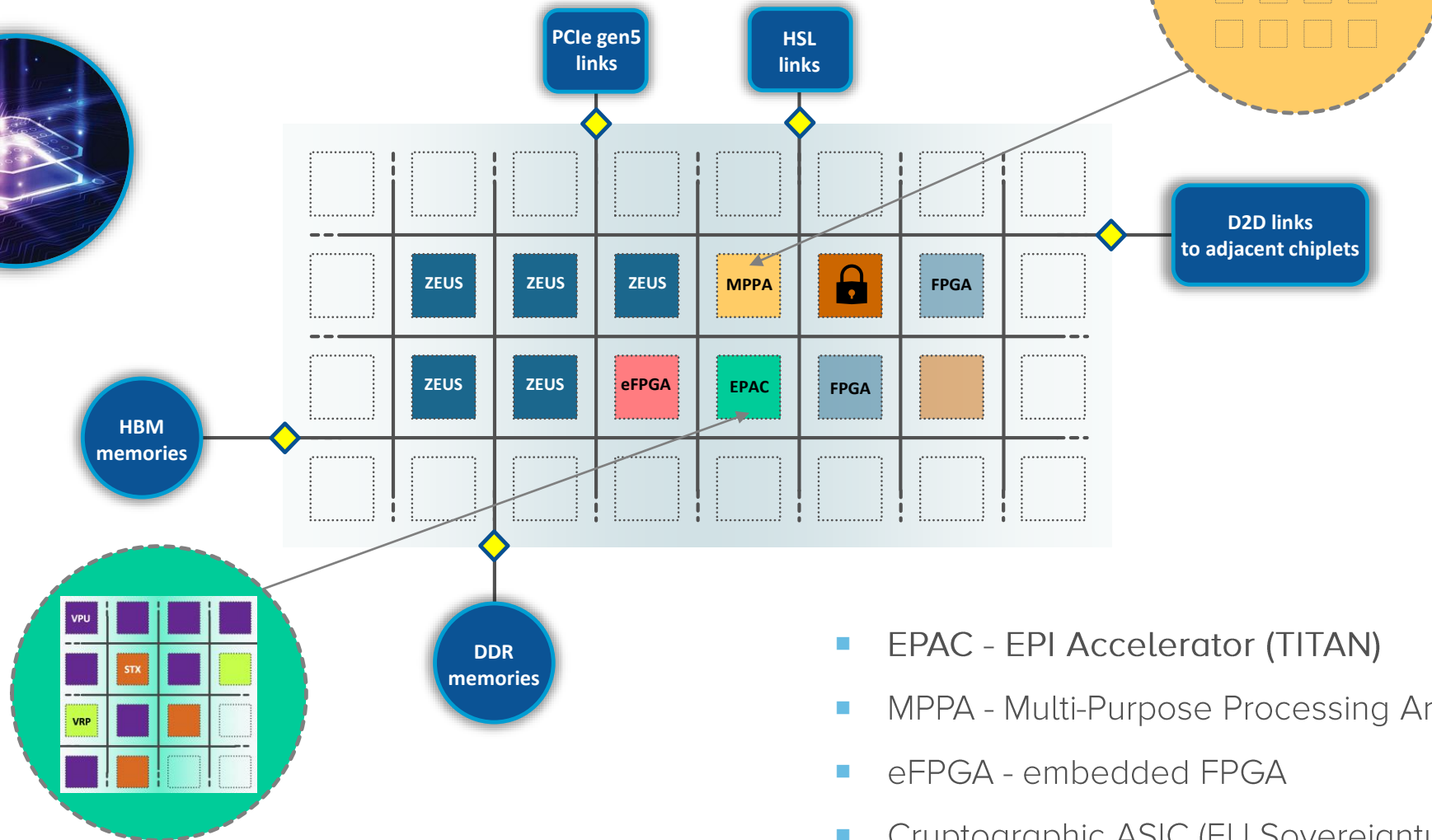
ROADMAP & TECHNOLOGY



ROADMAP

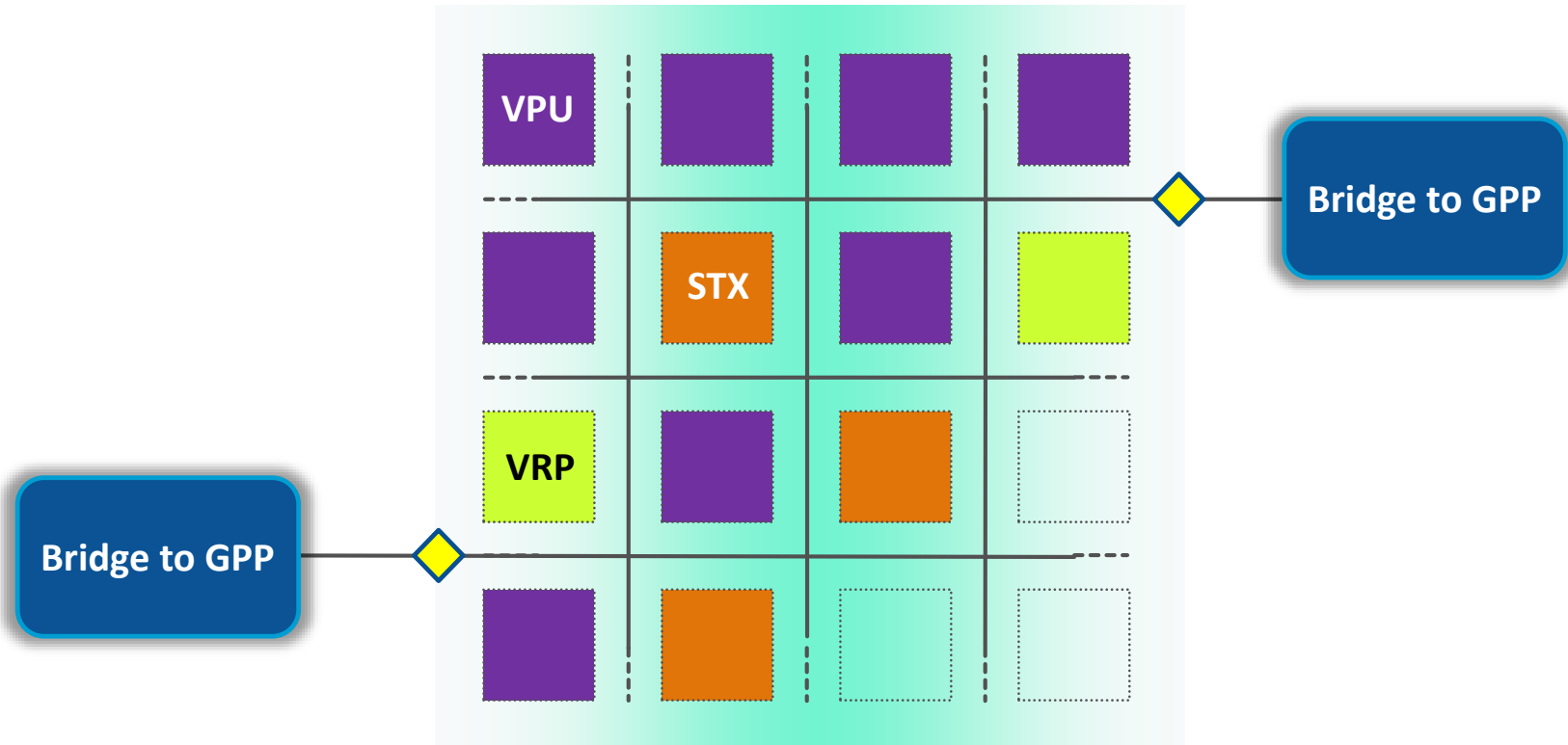


GPP AND COMMON ARCHITECTURE



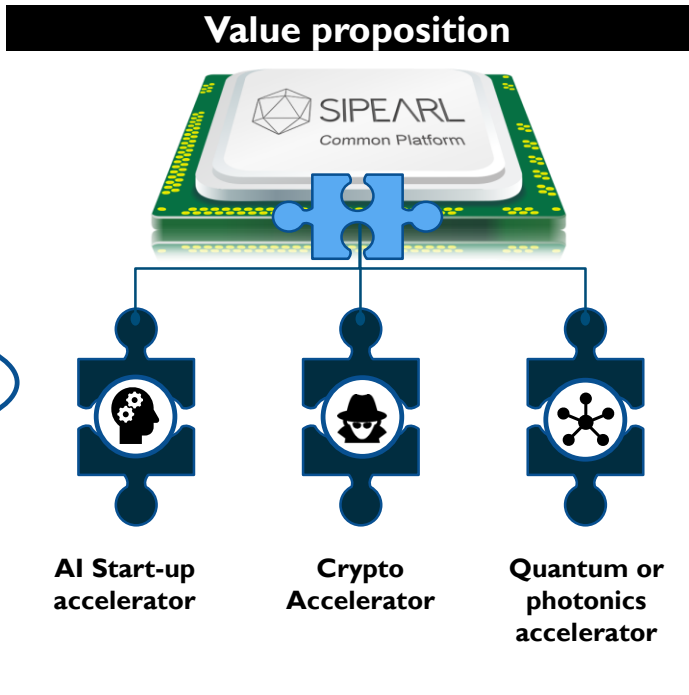
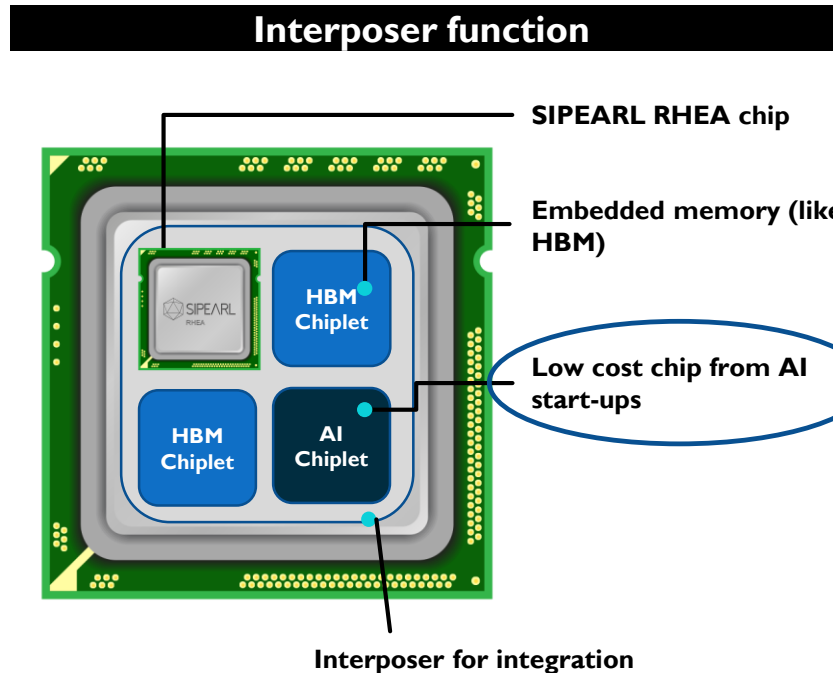
- EPAC - EPI Accelerator (TITAN)
- MPPA - Multi-Purpose Processing Array
- eFPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)

EPAC – RISC-V ACCELERATOR



- EPAC – TITAN = EPI Accelerator
- VPU – Vector Processing Unit
- STX – Stencil/Tensor accelerator

COMMON PLATFORM VISION: WE ACCELERATE ACCELERATORS



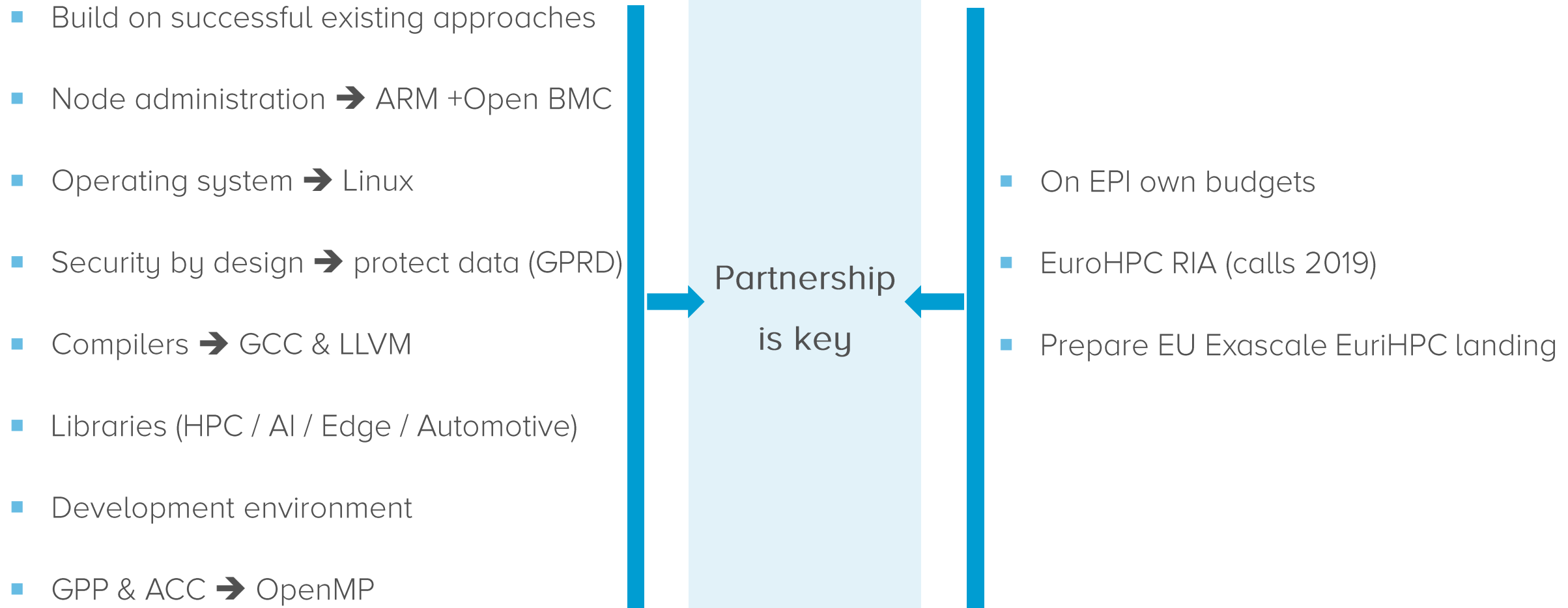
COMMON PLATFORM HAS THE POTENTIAL TO BECOME THE EUROPEAN I/O STANDARD DATA-PROCESSING



SOFTWARE

TECHNOLOGY

HOLISTIC APPROACH



EPI SOFTWARE AMBITIONS IN HPC

- **Complement the already existing software** to supply an entire HPC production stack
- **Deployment/administrative side**
 - Securing the node
 - Power managing the node
 - Booting the node
 - (Remote) controlling the node
 - Running a Linux distribution on the node
 - Managing various nodes in a large system
 - Monitoring & accounting various nodes in a large system
- **End-user side**
 - Compiling software for the General Purpose Processor
 - Compiling software for the Accelerators
 - Combining the use of GPP & Accelerators in a software
 - Leveraging standard libraries tuned for the node
 - Running the software on a node
 - Running the software on multiple nodes in a system
- **Automotive (edge-HPC) requirements**
 - Security, power
 - Predictable performance for autonomous driving
 - Multiple inputs, complex models

ARM WW HPC

CPU manufacturer,
2 server manufacturers,
“Astra” system at Sandia,
upcoming system at Stony Brook



Stony Brook University



Hewlett Packard Enterprise



CRAY



Atos



SIPEARL



UNIVERSITY OF LEICESTER



University of BRISTOL



GW4

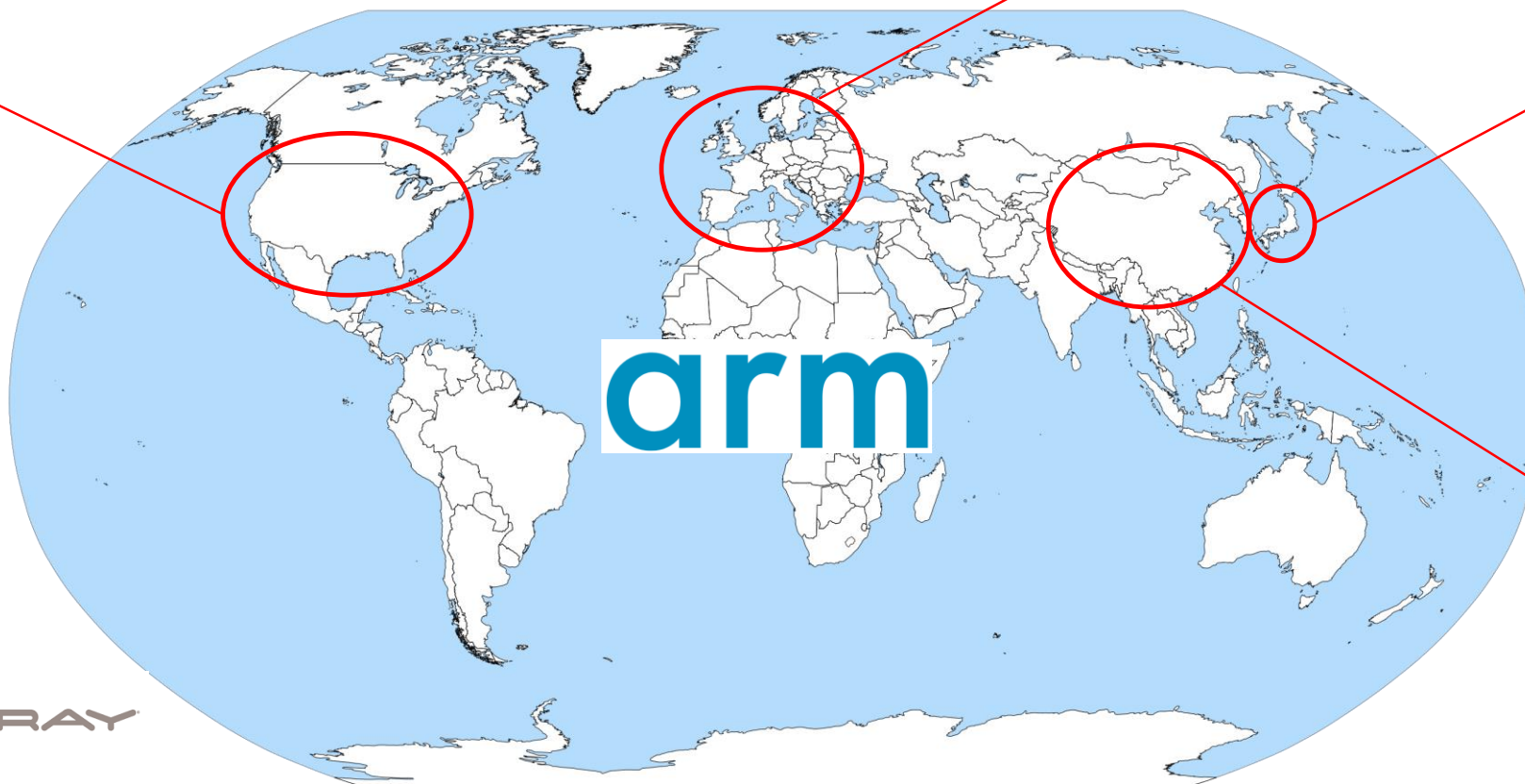
Upcoming CPU manufacturer,
Server manufacturer,
system at CEA, UK,
MontBlanc, EPI



CPU & server manufacturer,
upcoming “Fugaku” system



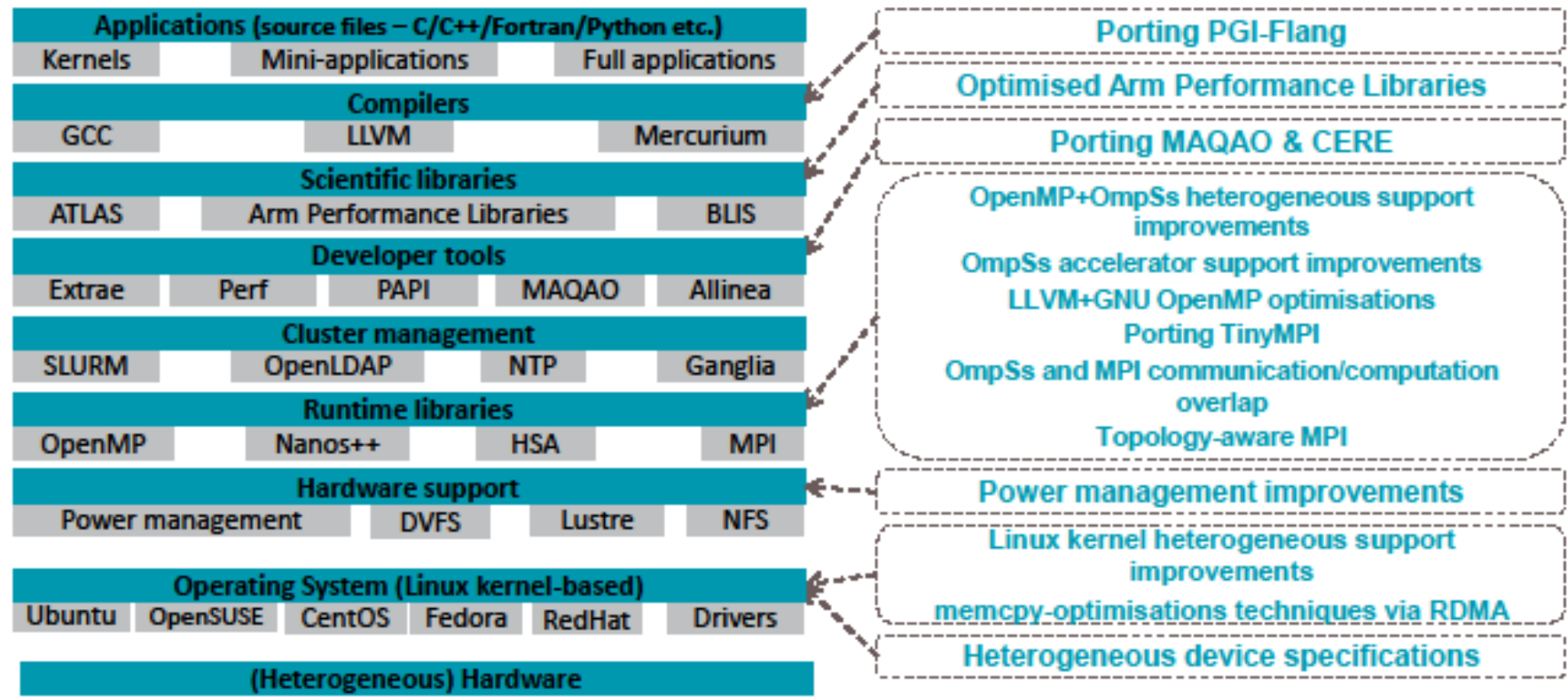
CPU & server manufacturer
[geopolitical issues regarding the license]



STANDING ON THE SHOULDERS OF SUCCESSFUL EUROPEAN PROJECTS

- Mont-Blanc 3 helped create and stabilize most of the foundations of a full HPC software stack on Arm

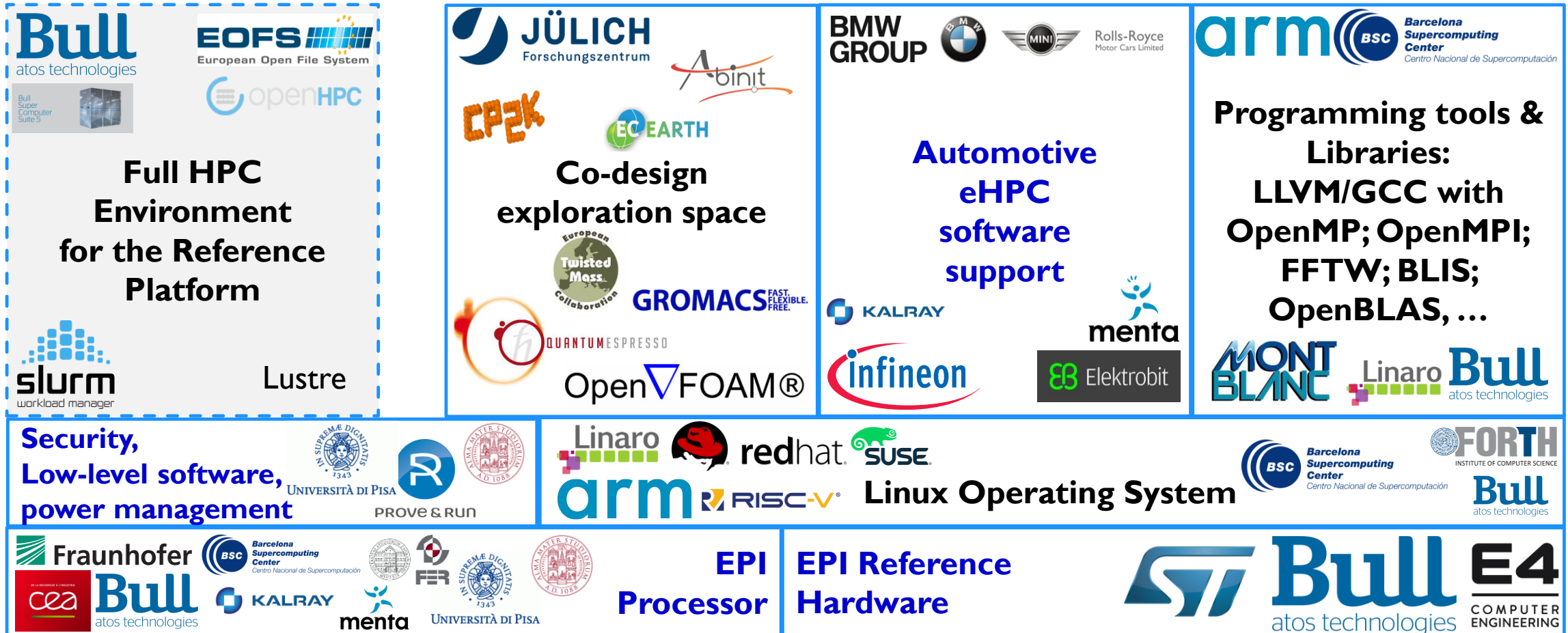
HPC Arm Software Stack



+ Contribution to OpenHPC (from 1.2)

EPI ECOSYSTEM

(INCLUDING POTENTIAL OUTSIDE PARTNERS)



... and those supporting the ecosystem & EPI, including EPI partners, external partners & OpenSource contributors

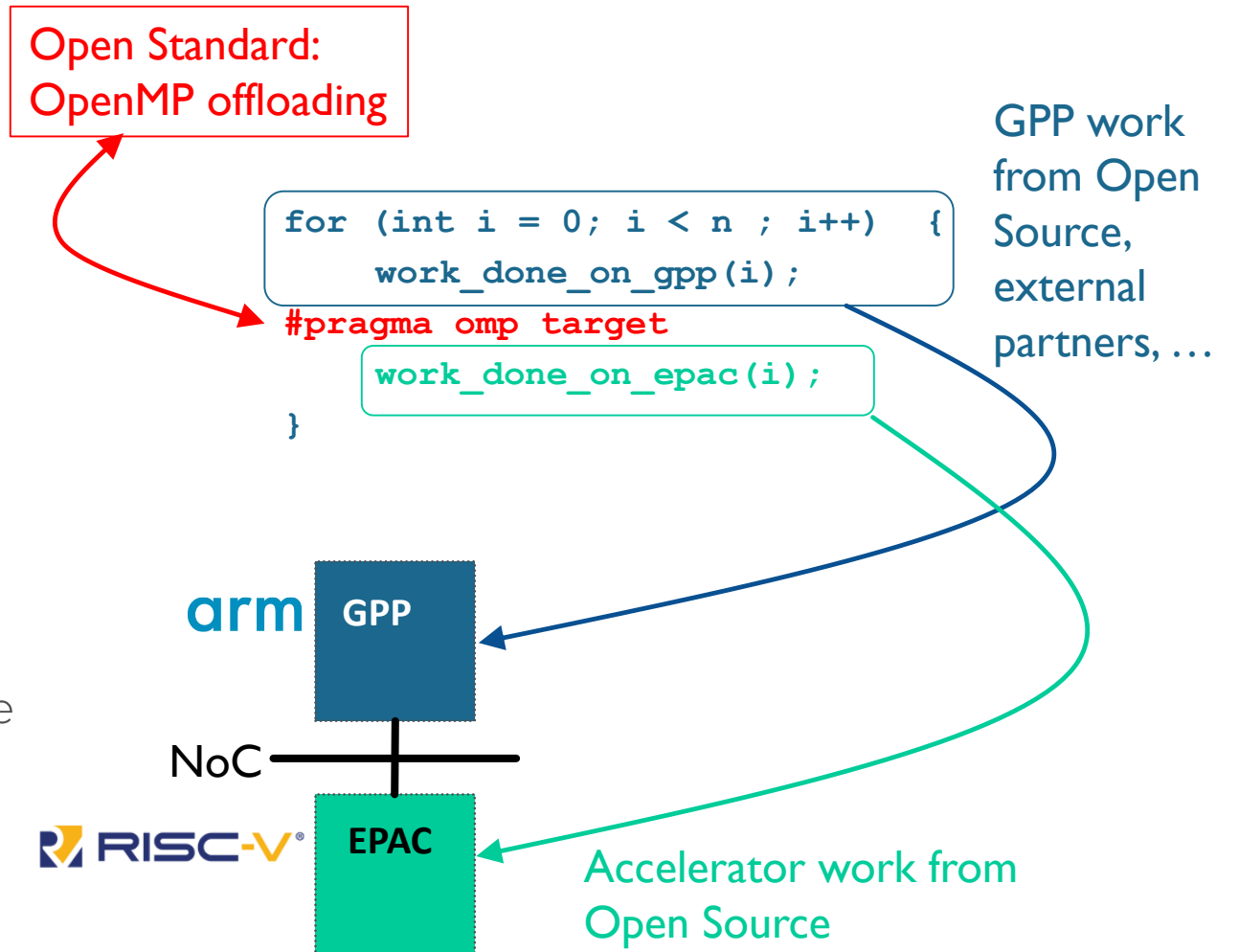
EXPANDING TO RISC-V



- The RISC-V architecture is used extensively in EPI
 - EPAC accelerator, Power Management, ...
- It is fully open and not reliant on one company for its definition
- The software ecosystem is not yet has developed as the Arm one
 - Mont-Blanc projects were instrumental in maturing the Arm ecosystem
- EPI software work includes work to bring RISC-V closer to the need of a production-ready general-purpose processor
- MPI work on RISC-V & hybrid
- OpenMP runtime on RISC-V
 - For offloading & native mode
- Compiler work
 - Including OpenMP SIMD
- Using RISC-V in the industrial world as a full-fledged, linux-capable processor and not just a microcontroller
 - Real-life use to strengthen the software

END-USER : GPP/ACC SEAMLESS USAGE

- Compiling, combining
 - Leveraging work from existing Open Source projects: GNU, LLVM
 - Choosing open standard over proprietary solutions
 - Emphasis on OpenMP in the project
 - OpenVX for automotive
 - Working with external partners
 - Arm work in LLVM & libraries for the GPP
 - EPI adding missing pieces to fully exploit the Common Platform design
 - Better vectorization in EPAC
 - OpenMP offloading
 - OpenMP SIMD for EPAC

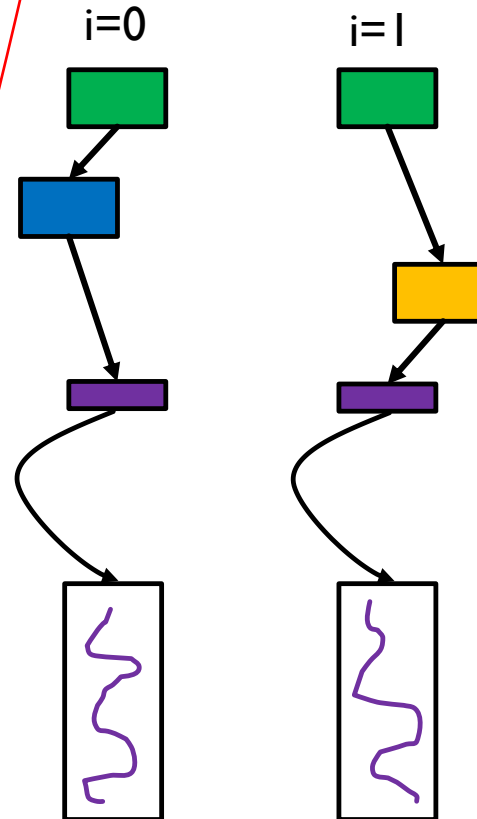


END-USER

```
#pragma omp simd
for (int i = 0 ; i < n ; i++) {
    green_work(i);
    if (cond(i)) {
        blue_work(i);
    } else {
        orange_work(i);
    }
    purple_function(i);
}
```

```
#pragma omp simd declare
void purple_function(int i) {
    (...)
}
```

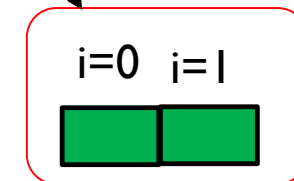
Open Standard:
OpenMP SIMD



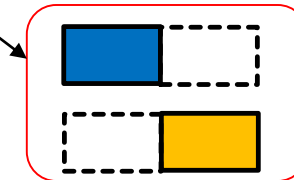
State-of-the-art
(SSE, AVX, ...)

Enabled by
ARM SVE,
RISC-V "V"

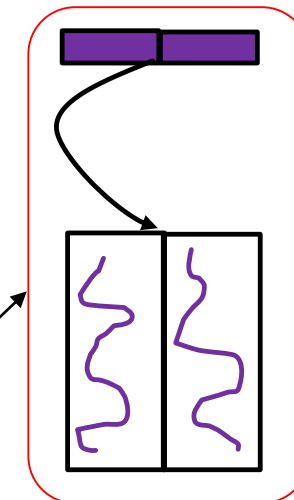
Enabled by
OpenMP
4.x



fully SIMD
vectorized



masked
SIMD



OpenMP
SIMD
"declare"
to generate
vector
function call
&
vector
function body

CONCLUSION



EPI NEXT CHALLENGES

Build on existing IP and w. communities

- Risk minimized by leveraging existing work
 - Open Source, previous projects, external partners
- Future-proofed by favoring open standards & simpler programming models
- Legacy taken into account to widen the potential user-base

Close the gap between R&I and industrial products

- Have EPI “delivery and product” oriented while fulfilling its needs for Research and Innovation
 - We need to be ready for production end of 2021
- Face a WW class competition
 - We will not be used because we are “engineered” in EU but because we have the best and cost effective solution
- Re-create a real ecosystem for deep node microelectronics:
 - Engineers
 - IP's
 - ...factories...

THANK YOU FOR YOUR ATTENTION



European Processor Initiative

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