Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

EPI and beyond: perspectives of a European supercomputing center on open-source hardware and software

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06/2019


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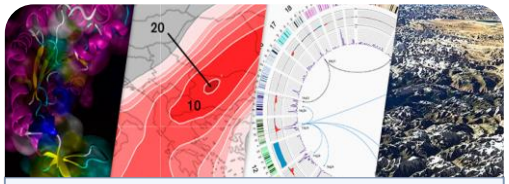
BSC-CNS objectives

Supercomputing services to Spanish and EU researchers



R&D in Computer, Life, Earth and Engineering Sciences

PhD program, Technology Transfer, public engagement

BSC-CNS is a consortium that includes

Spanish Government	60%
Catalan Government	30%
Univ. Politècnica de Catalunya (UPC)	10%

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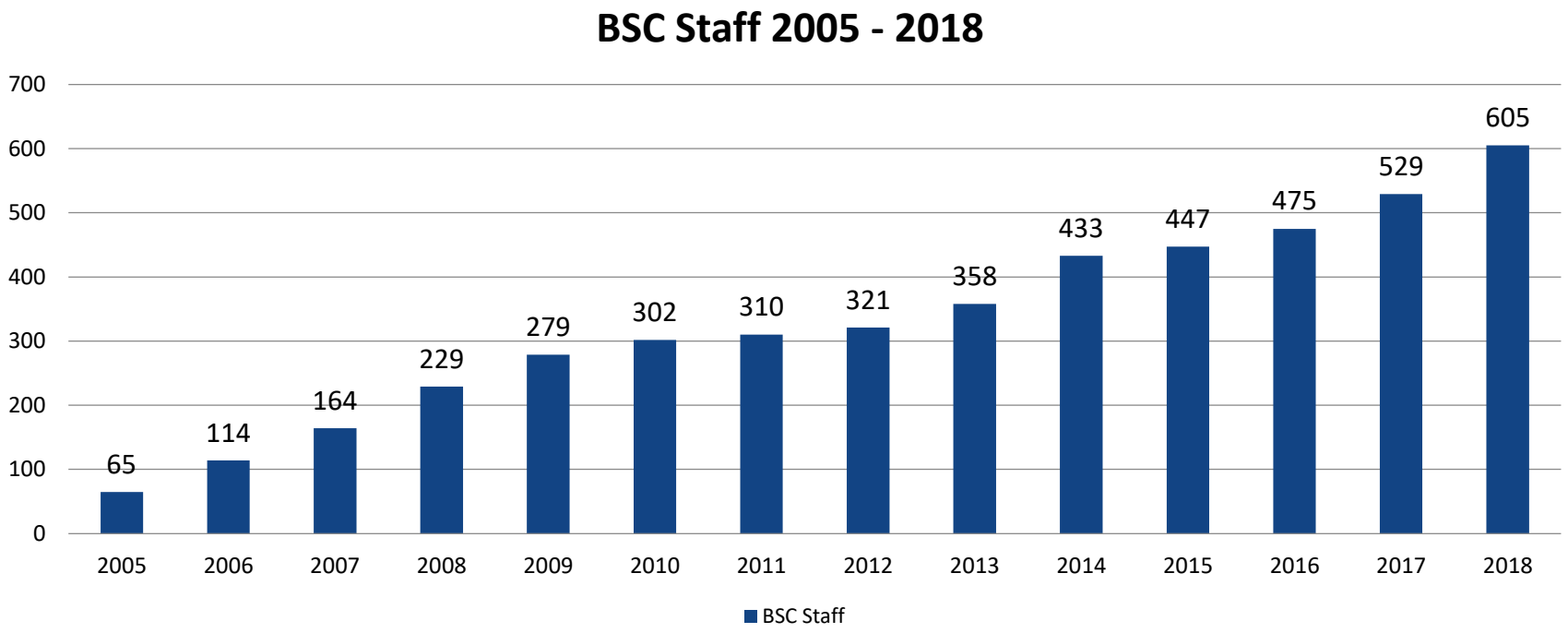
People evolution



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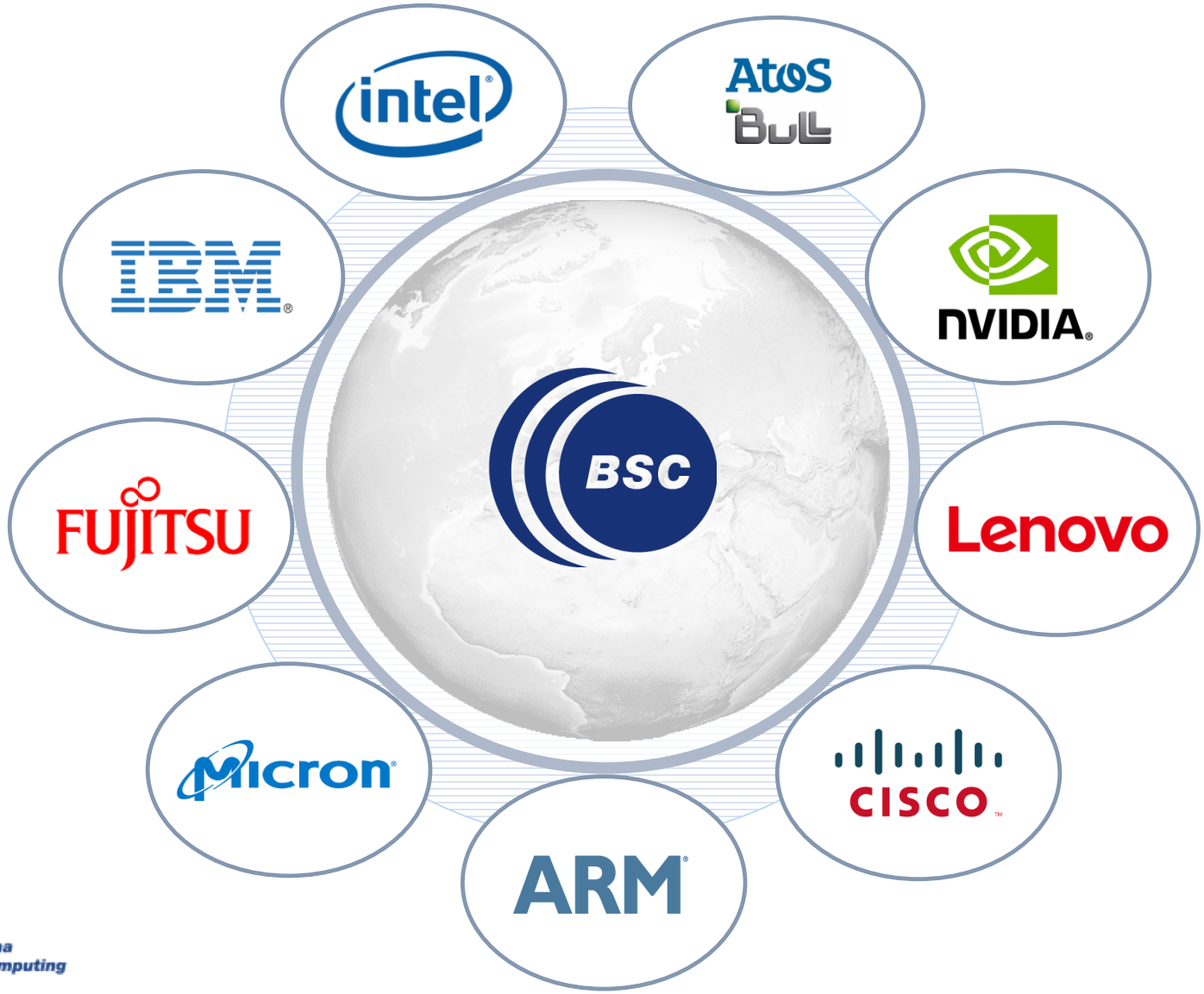
BSC & The Global IT Industry 2018



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European Commission

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Digital Single
supercompute

Luxembou 7 June

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Future MareNostrum 5 Supercomputer at BSC to host Made-in-Europe Technologies

June 10, 2019 by staff | Leave a Comment

Today the Barcelona Supercomputing Center announced plans to host EuroHPC processor technologies within its future Mare Norstrom 5 supercomputer. The EuroHPC Joint Undertaking has chosen BSC to be one of the main centers to host pre-exascale computers co-funded by the European Union.

MareNostrum 5

circa 220 Million Euros budget

Pre-Exascale system

Including new technologies

MareNostrum 1
2004 – 42,3 Tflops
1st Europe / 4th World
New technologies

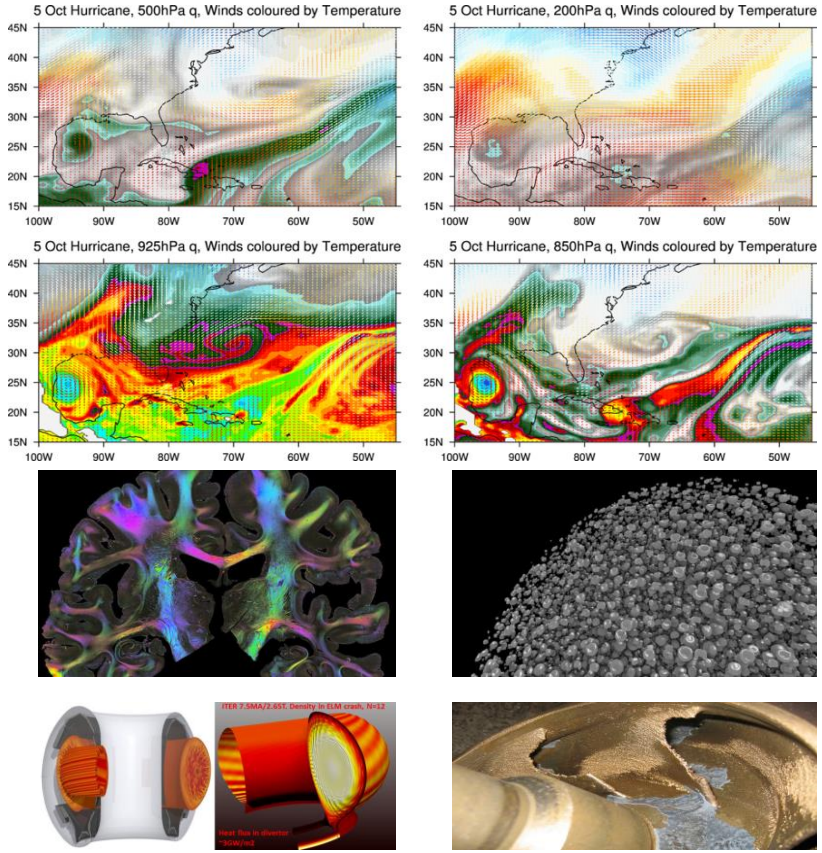
MareNostrum 2
2006 – 94
1st Europe / 5th
New tech

MareNostrum 3
,1 Pflops
ope / 36th World

MareNostrum 4
2017 – 11,1 Pflops
2nd Europe / 13th World
New technologies

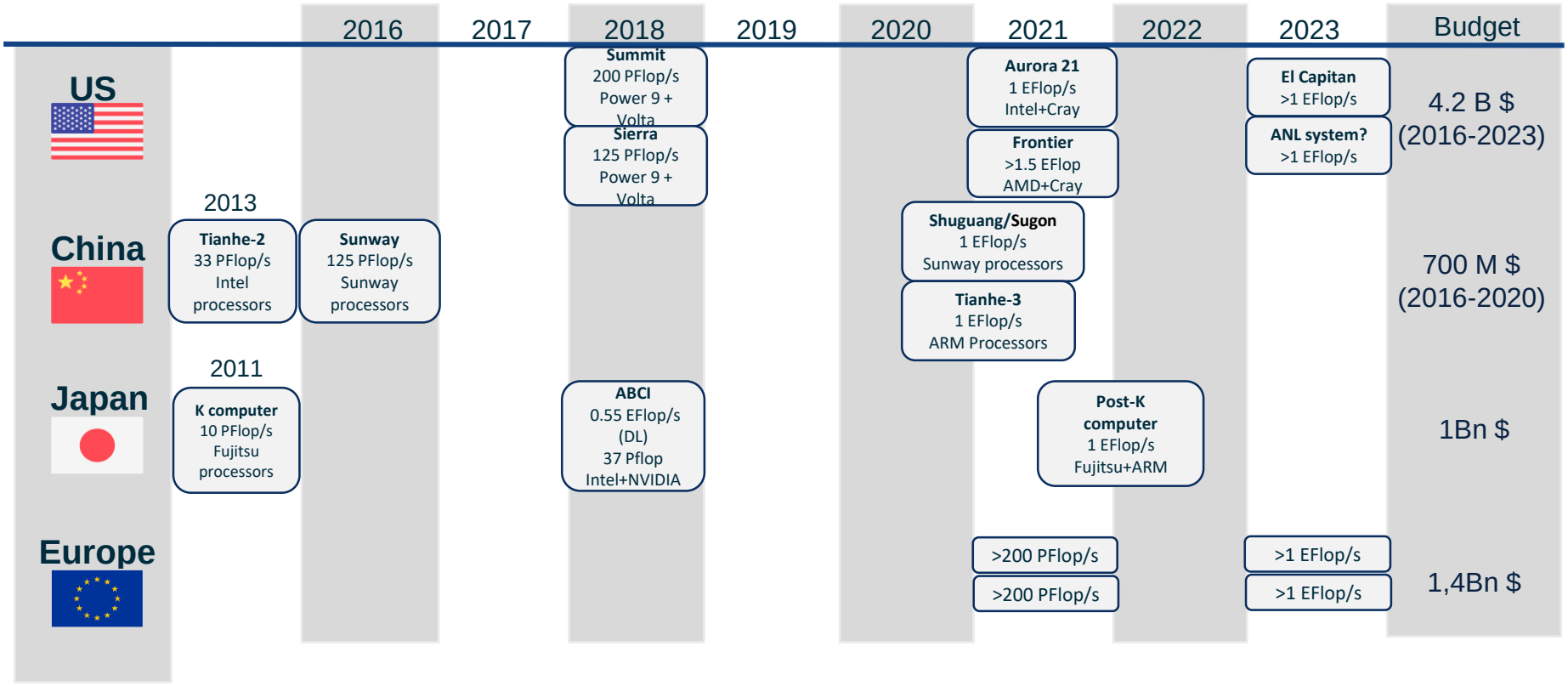
Why is HPC Needed?

- Will save billions by helping us to adapt to climate change
- Will improve human health by enabling personalized medicine
- Will improve fuel efficiency of aircraft & help design better wind turbines
- Will help us to understand how the human brain works



Images courtesy of The PRACE Scientific Steering Committee, "The Scientific Case for Computing in Europe 2018-2026"

The roadmap towards Exascale



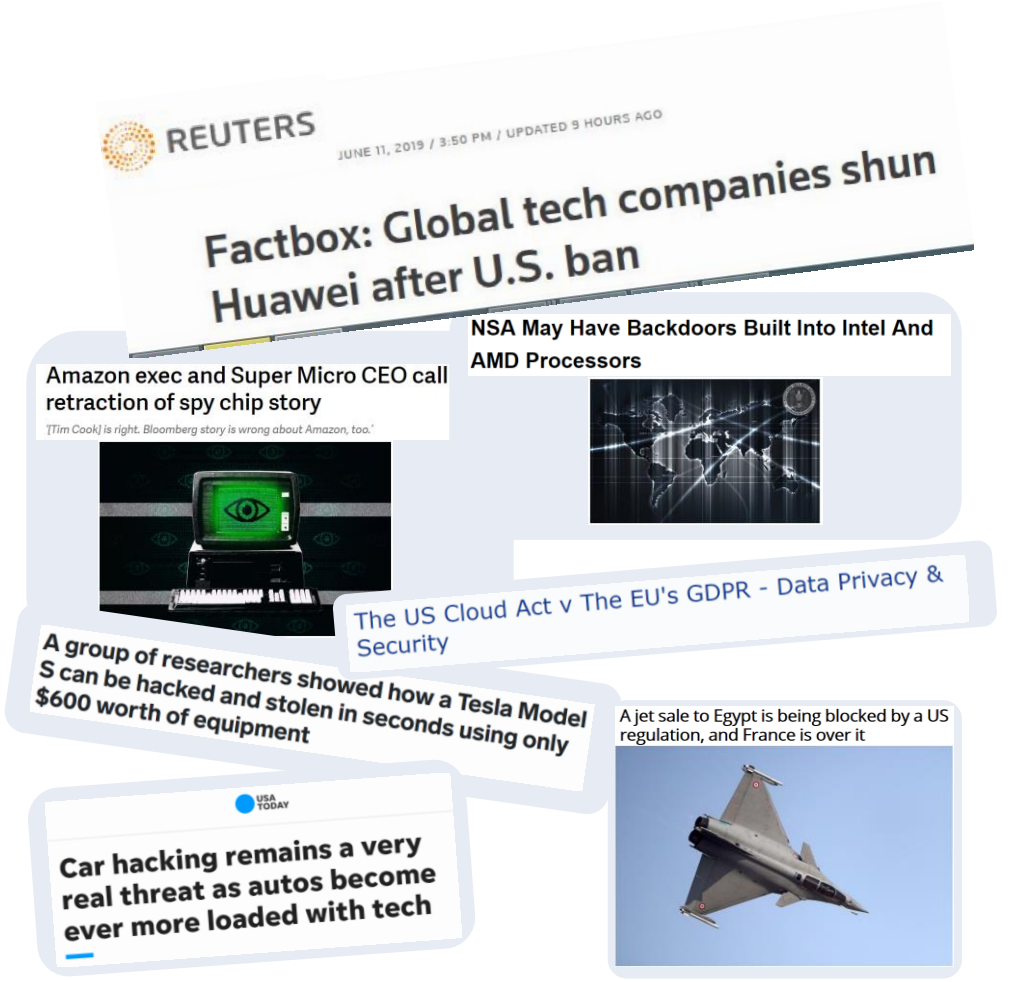
Where Europe needs to be stronger

- Only 1 of the 10 most powerful HPC systems is in the EU
- HPC codes must be upgraded
- Vital HPC hardware elements are missing: **General Purpose Processor** and **Accelerators**

EU needs its own source of as many of the system elements as possible

Why Europe needs its own Processors

- Processors now control almost every aspect of people's lives
- **Security** (back doors etc.)
- Possible **future restrictions on exports to EU** due to **i**ncreasing protectionism
- **A competitive EU supply chain** for HPC technologies will create jobs and growth in Europe



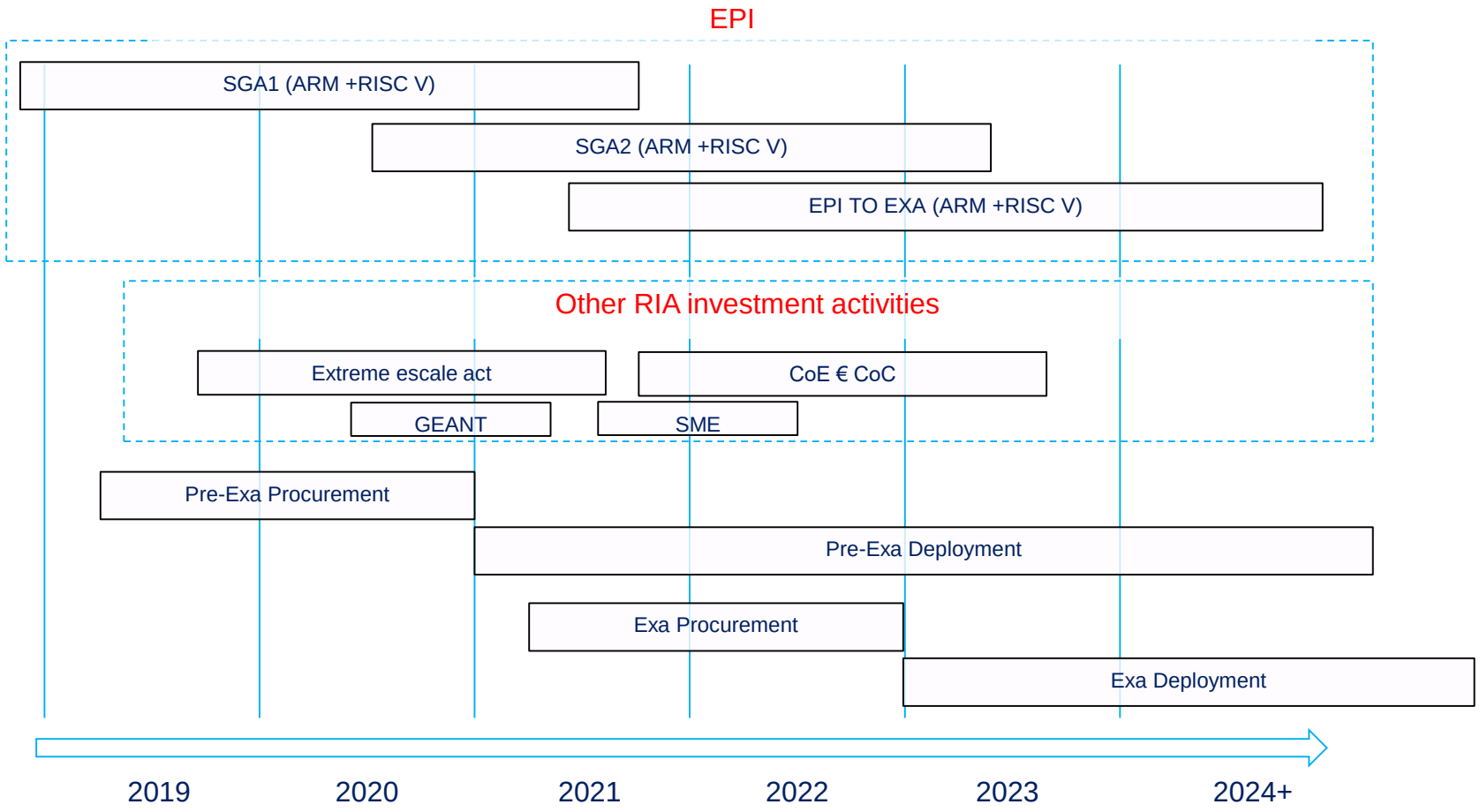
Images courtesy of Reuters.com and European Processor Initiative

The new European framework

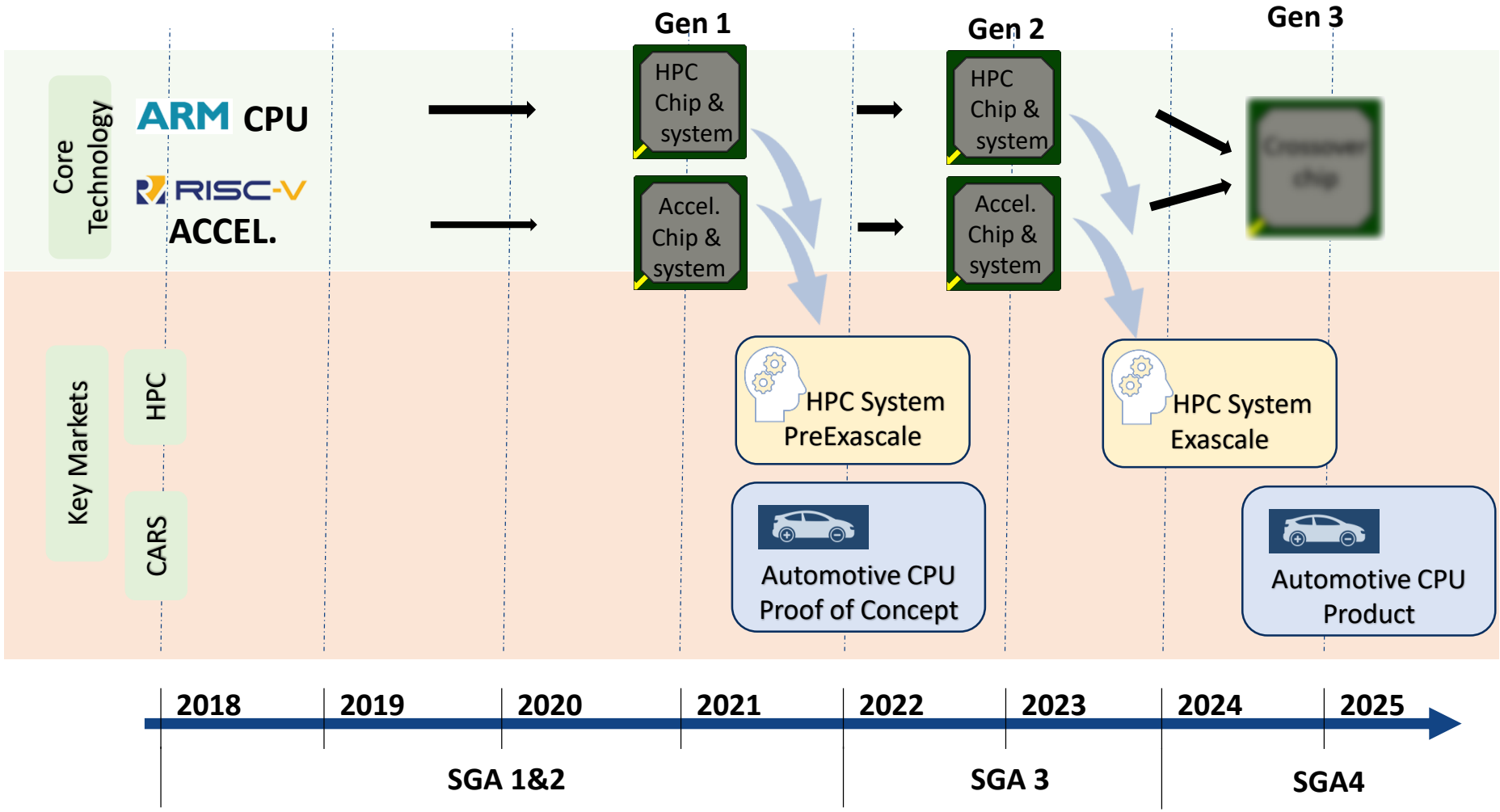
Horizon Europe | The EU's next research and innovation programme (2021 – 2027)

EuroHPC Joint Undertaking

EuroHPC Roadmap

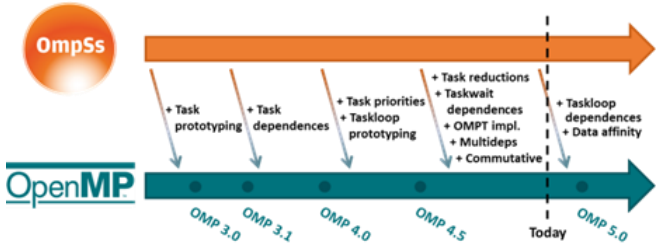


EPI roadmap


Gen 1
Gen 2
Gen 3
Core Technology
ARM CPU
RISC-V
ACCEL.
HPC Chip & system
Accel. Chip & system
HPC Chip & system
Accel. Chip & system
Crossover chip
Key Markets
HPC
CARS
HPC System PreExascale
HPC System Exascale
Automotive CPU Proof of Concept
Automotive CPU Product
2018
2019
2020
2021
2022
2023
2024
2025
SGA 1&2
SGA 3
SGA4

BSC's exascale vision in EPI (and beyond)

- Ensure programmers survive the "exascale" future

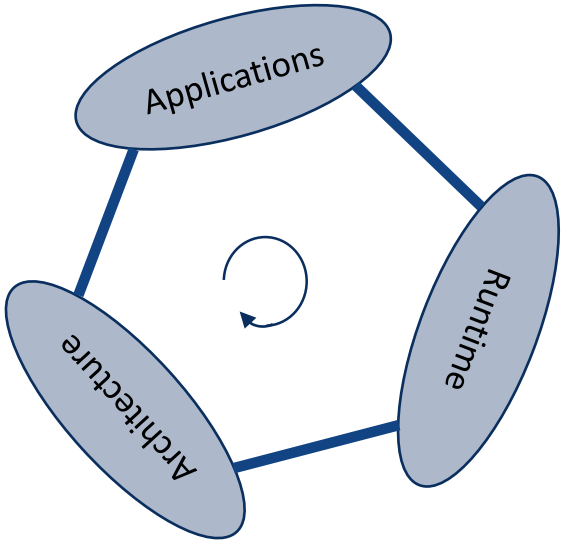


- Can we "move the future" ?

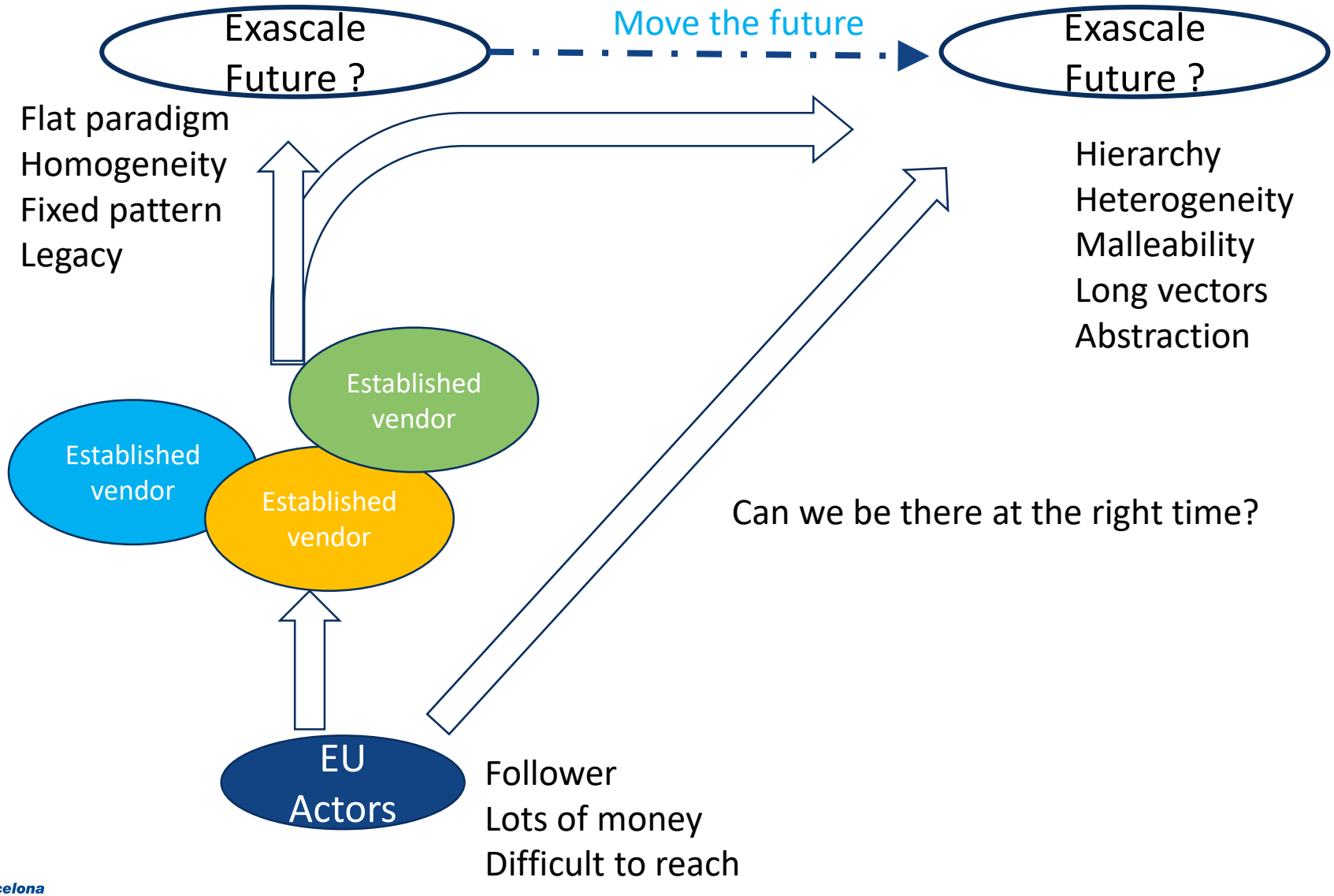
- Maximize take-up → standards

RISC-V

- Co-design
  - Issues addressed in multiple places
  - Runtime aware architectures
  - Runtime provides total abstraction



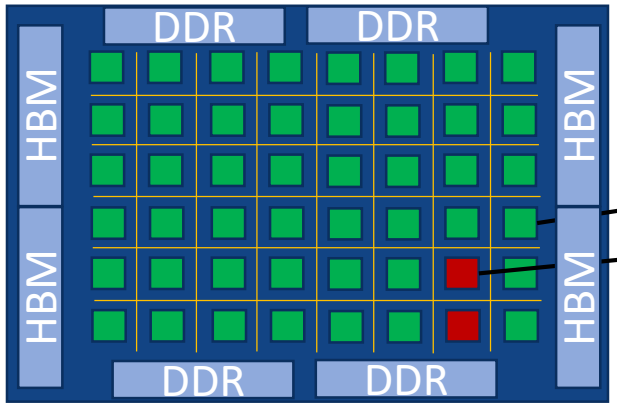
More about the vision



BSC's vision in EPI RISC-V vector processor

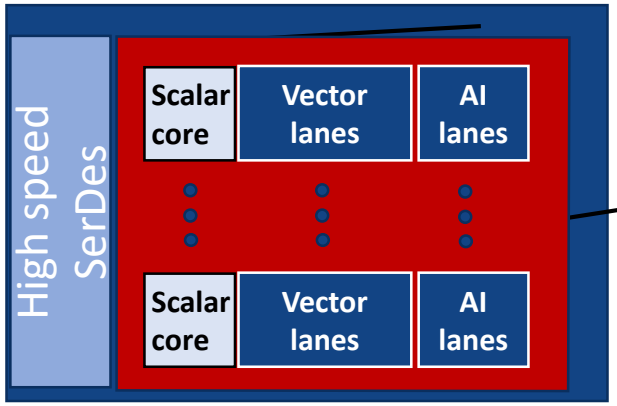
- **Low power**: relatively low voltage , relatively low frequency
- **High throughput devices**
  - **Long Vectors**
    - Optimize memory throughput (High BW, B/F), locality
    - Decoupled architecture
  - **ISA is important:**
  - **"limited" number of control flows**
- **Hierarchical Acceleration**
  - Nested hierarchical parallelism
  - Balanced hierarchy
  - Homogenized heterogeneity
- **MPI+OpenMP paradigm**
  - Throughput oriented programming approach
  - Malleability in application + Dynamic resource (cores, power, BW) management
  - Intelligent runtimes & Runtime Aware Architectures
    - Handle overlap and locality
    - Reduce overhead → hierarchical
    - Architectural support for the runtime

EPI chips



General Purpose Processor (GPP) chip

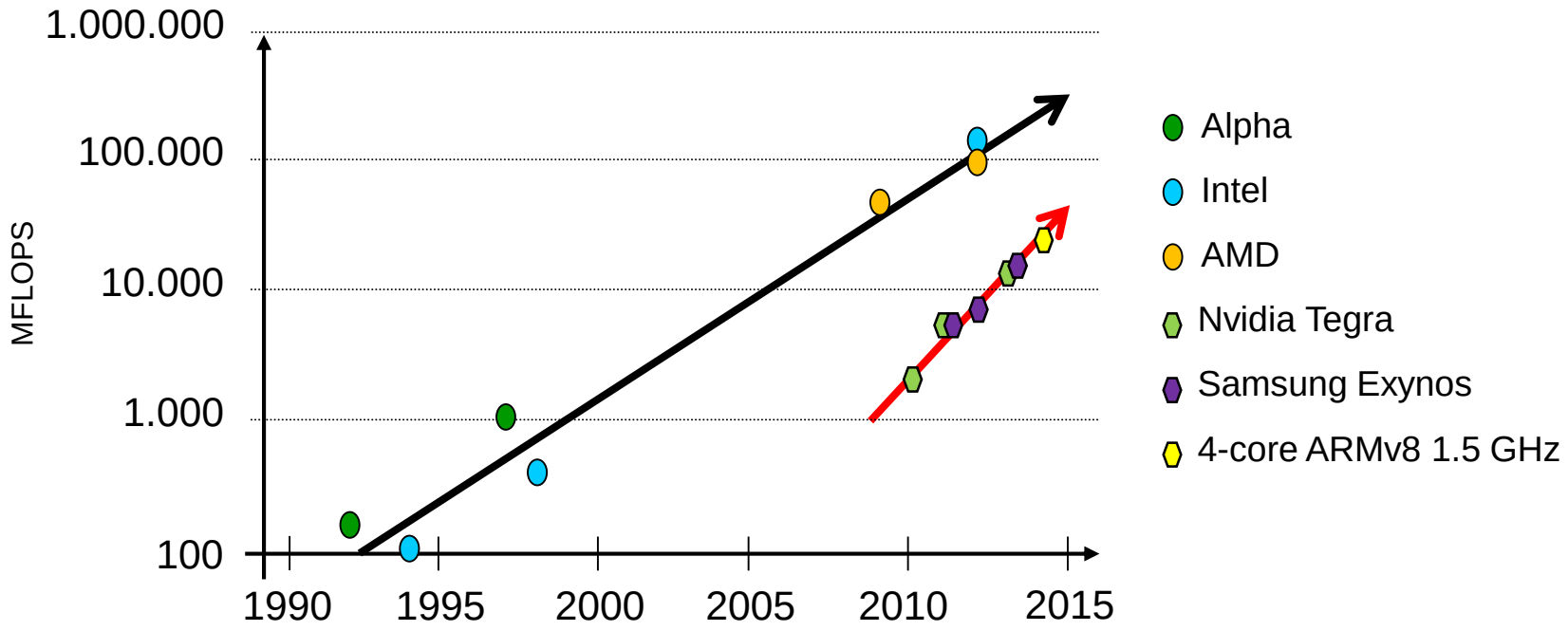
- 7 nm, chip-let technology
- **ARM-SVE** tiles
- **RISC-V** vector+AI accelerator tiles
- L1, L2, L3 cache subsystem + HBM + DDR



RISC-V Accelerator Demonstrator **Test Chip**

- 22 nm FDSOI
- Only one RISC-V accelerator tile
- On-chip L1, L2 + off-chip HBM + DDR PHY
- Targets 128 DP GFLOPS (vector proc.)

The “killer mobile processors”…



- Microprocessors killed the Vector supercomputers
  - They were not faster …
  - … but they were significantly cheaper and greener
- History may be about to repeat itself …
  - Mobile processor are not faster …
  - … but they are significantly cheaper and greener

ARM-based prototypes at BSC

2011
Tibidabo

ARM multicore

2012
KAYLA

ARM + GPU
CUDA on ARM

2013
Pedraforca

ARM + GPU
Inifinband
RDMA

2014
Mont-Blanc

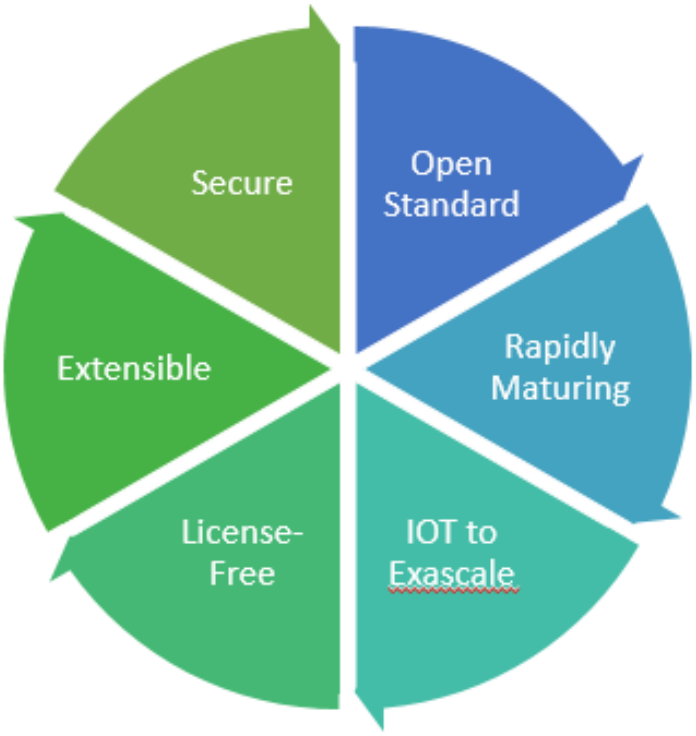
Single chip ARM+GPU
OpenCL on ARM GPU

PRACE PRACE PRACE MONT BLANC

The Open-Source Hardware Opportunity

- In 2015, Mateo Valero said he believed a European Supercomputer based on ARM was possible (Mont-Blanc).
- Even though ARM is no longer European, it can form part of the short-term solution
- The fastest-growing movement in computing at the moment is Open-Source and is called RISC-V
- The future is Open and RISC-V is democratising chip-design

RISC-V



The Open-Source Hardware Opportunity

THE ADVANTAGES….

- RISC-V has no legacy constraints
- RISC-V has (standard and non-standard) extensions
- RISCV extensions facilitate decoupling from hardware (avoid low level accelerator control, e.g. memory mapped)
- RISC-V is contributed by committees of experts doing a great job

THE LIMITATIONS….

- Many people's contributions = many different requirements
- Some features may result less important to some members
- The eco-system issue (but smaller than – for example – in consumer market)
- The political issue question

Special thanks to

- Mateo Valero
- Jesus Labarta
- Eugene Griffiths
- Fabrizio Gagliardi

Thank you for attending

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