Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

Mobiles: on the road to Supercomputers

GoingDigital Community - Mobile World Congress 19

Prof. Mateo Valero

BSC Director

erc

GoingDigital
Rethink economy, business & society.

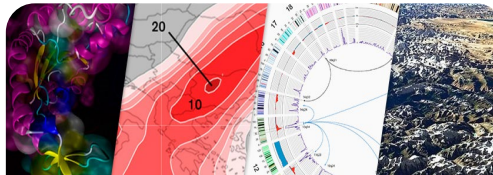A programme of

MOBILE WORLD CAPITAL BARCELONA

Feb 2019

Barcelona Supercomputing Center
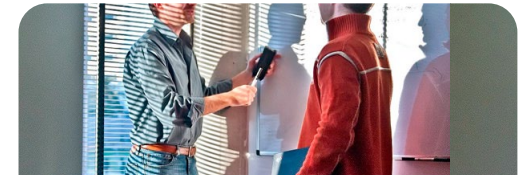# Centro Nacional de Supercomputación

BSC-CNS objectives

Supercomputing services to Spanish and EU researchers

R&D in Computer, Life, Earth and Engineering Sciences

PhD programme, technology transfer, public engagement

BSC-CNS is a consortium that includes

Spanish Government	60%	GOBIERNO DE ESPAÑA / MINISTERIO DE ECONOMÍA Y COMPETITIVIDAD
Catalonian Government	30%	Generalitat de Catalunya Departament d'Empresa i Coneixement
Univ. Politècnica de Catalunya (UPC)	10%	UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

Barcelona Supercomputing Center
Centro Nacional de Supercomputación
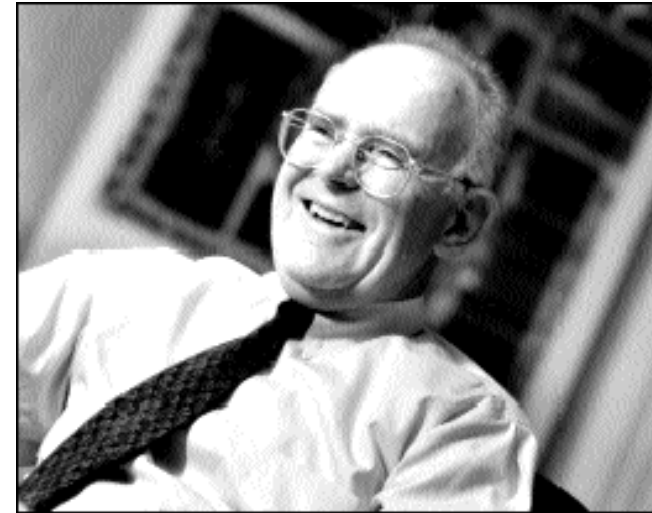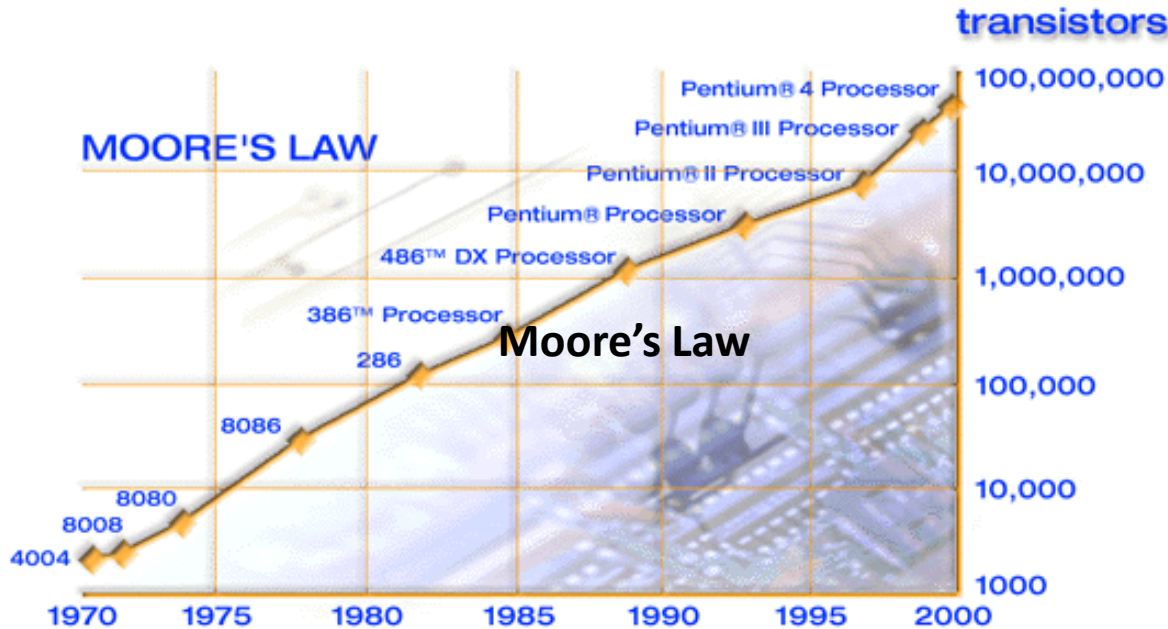
Technological Achievements

- **Transistor (Bell Labs, 1947)**
  - **DEC PDP-1 (1957)**
  - **IBM 7090 (1960)**

- **Integrated circuit (1958)**
  - **IBM System 360 (1965)**
  - **DEC PDP-8 (1965)**

- **Microprocessor (1971)**
  - **Intel 4004**
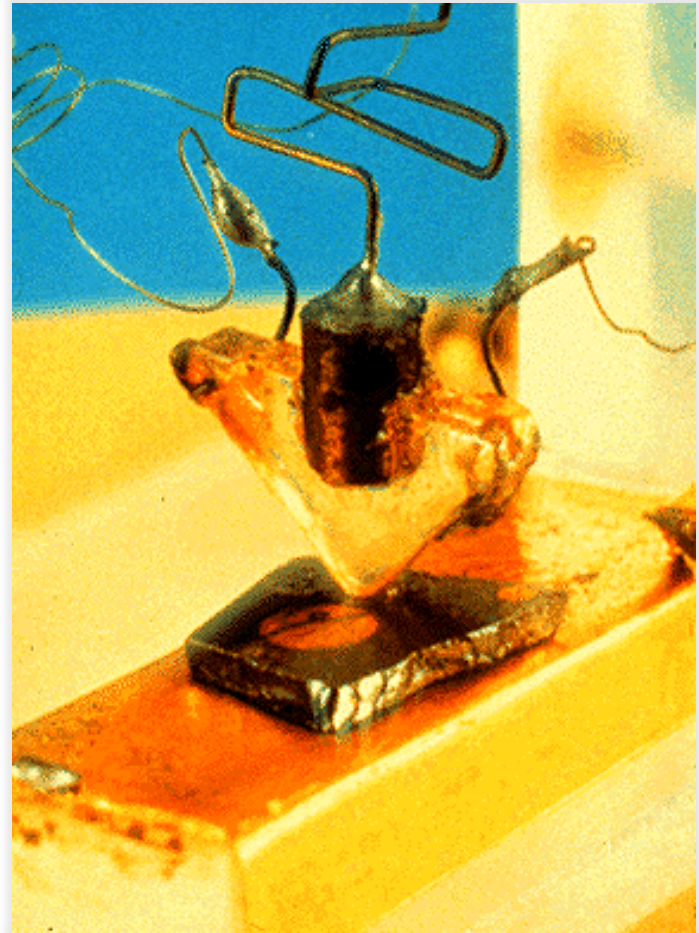
Technology Trends: Microprocessor Capacity

2X transistors/Chip Every 1.5 years

Called "Moore's Law"

Microprocessors have become smaller, denser, and more powerful. Not just processors, bandwidth, storage, etc

Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

ANNOUNCING TESLA V100

GIANT LEAP FOR AI & HPC
VOLTA WITH NEW TENSOR CORE

21B xtors | TSMC 12nm FFN | 815mm^2
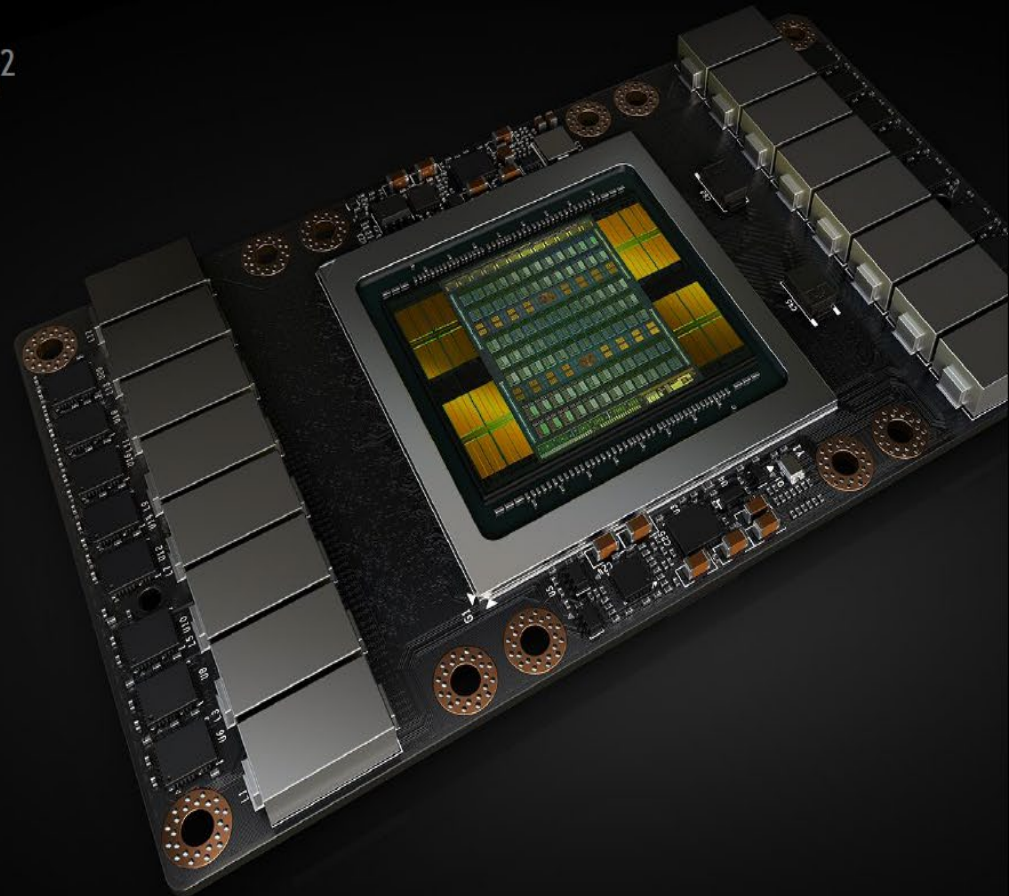
5,120 CUDA cores

7.5 FP64 TFLOPS | 15 FP32 TFLOPS
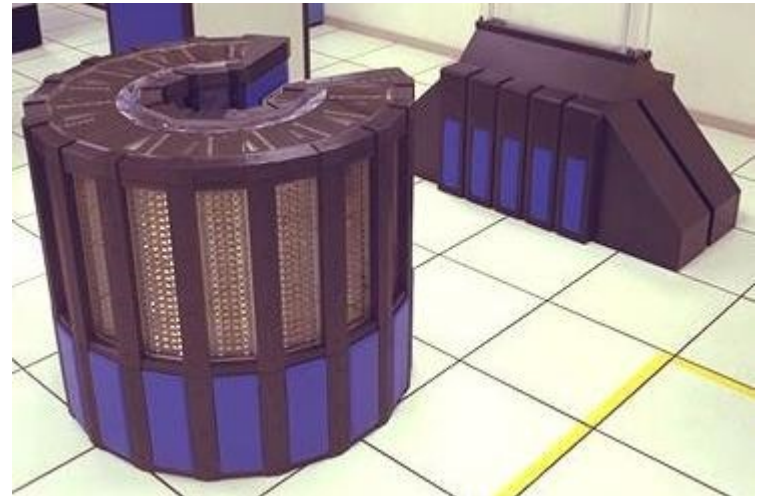
NEW 120 Tensor TFLOPS

20MB SM RF | 16MB Cache

16GB HBM2 @ 900 GB/s
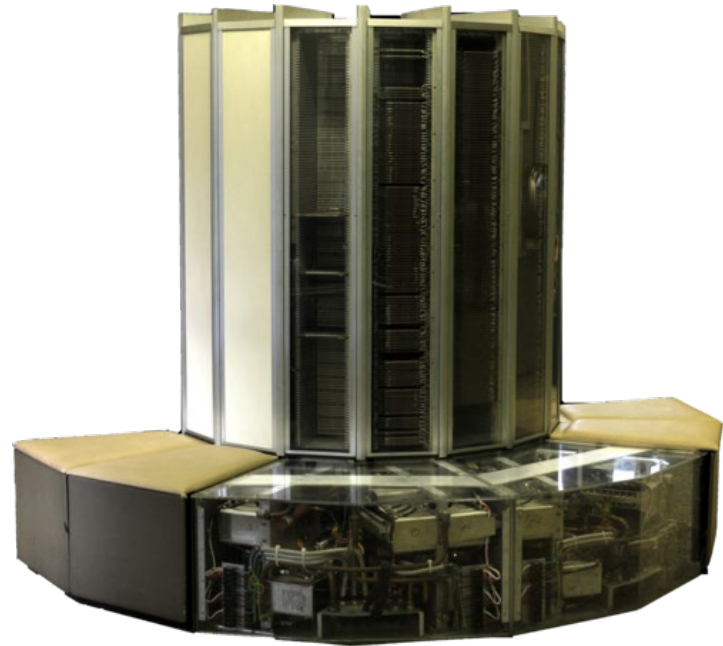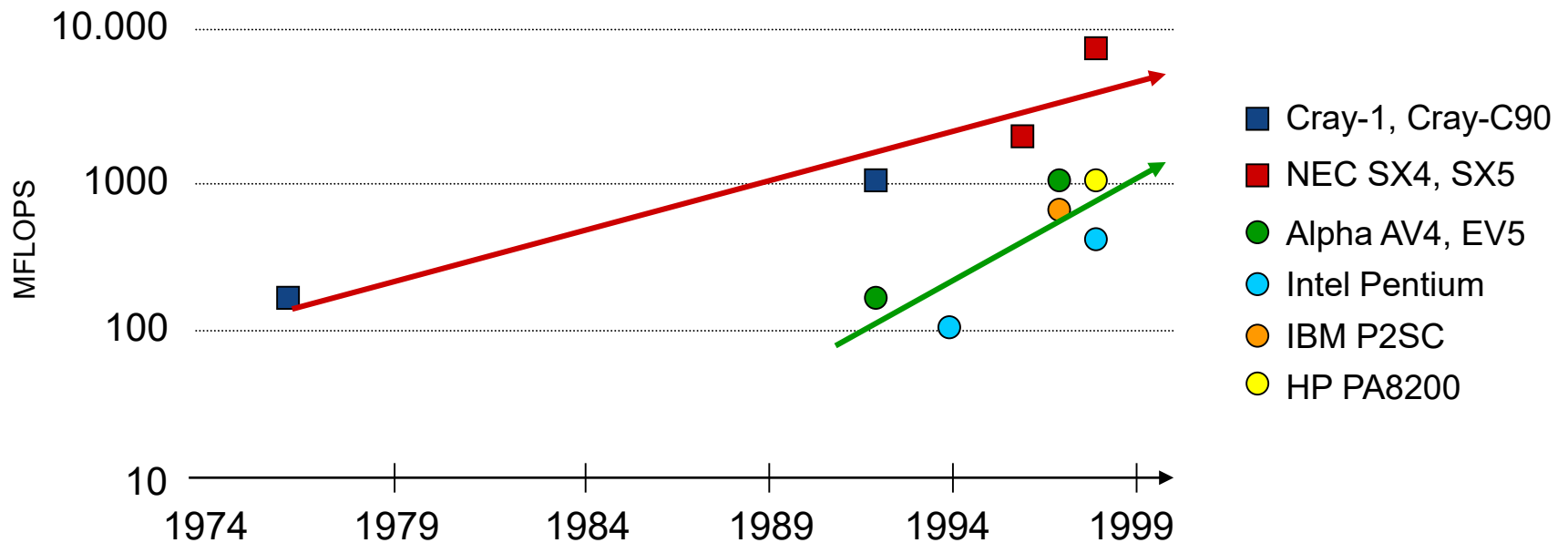
300 GB/s NVLink

In the beginning ... there were only supercomputers

- **Built to order**
  - Very few of them
- **Special purpose hardware**
  - Very expensive

- **Control Data**
- **Cray-1**
  - 1975, 160 MFLOPS
    - 80 units, 5-8 M$
- **Cray X-MP**
  - 1982, 800 MFLOPS
- **Cray-2**
  - 1985, 1.9 GFLOPS
- **Cray Y-MP**
  - 1988, 2.6 GFLOPS

- **...Fortran+ Vectorizing Compilers**

"Killer microprocessors"

- Microprocessors killed the Vector supercomputers
  - They were not faster …
  - … but they were significantly **cheaper** and **greener**
- 10 microprocessors approx. 1 Vector CPU
  - SIMD vs. MIMD programming paradigms

M. Valero. "Vector Architectures: Past, Present and Future". Keynote talk. ICS-11. IEEE-ACM. Melbourne, 1998

Then, commodity took over special purpose

《 ASCI Red, Sandia
  - 1997, 1 Tflops (Linpack),
  - 9298 processors at 200 MHz,
  - 1.2 Terabytes
  - Intel Pentium Pro
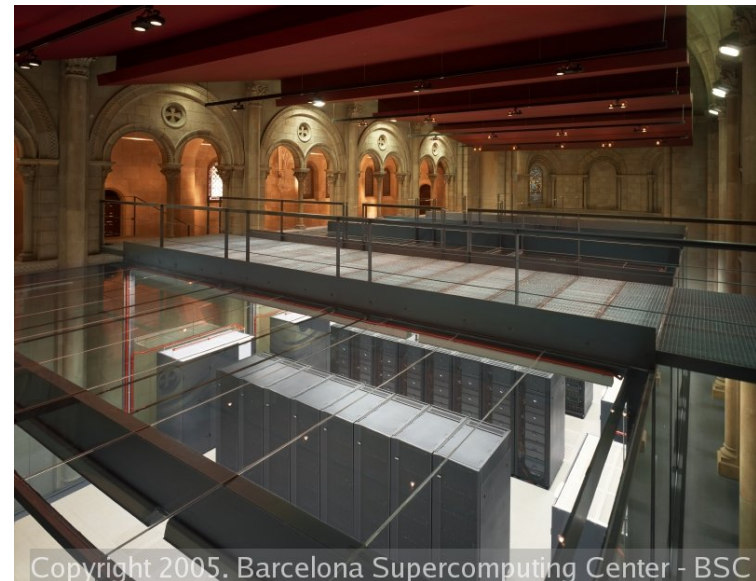   - Upgraded to Pentium II Xeon, 1999, 3.1 Tflops

《 ASCI White, Lawrence Livermore Lab.
  - 2001, 7.3 TFLOPS,
  - 8192 proc. RS6000 at 375 MHz,
  - 6 Terabytes,
  - IBM Power 3
  - (3+3) MWats

Message-Passing Programming Models

Finally, commodity hardware + commodity software

- MareNostrum
  - Nov 2004, #4 Top500
    - 20 Tflops, Linpack
  - IBM PowerPC 970 FX
    - Blade enclosure
  - Myrinet + 1 GbE network
  - SuSe Linux

Copyright 2005. Barcelona Supercomputing Center - BSC

Copyright 2010. Barcelona Supercomputing Center - BSC

Copyright 2005. Barcelona Supercomputing Center - BSC
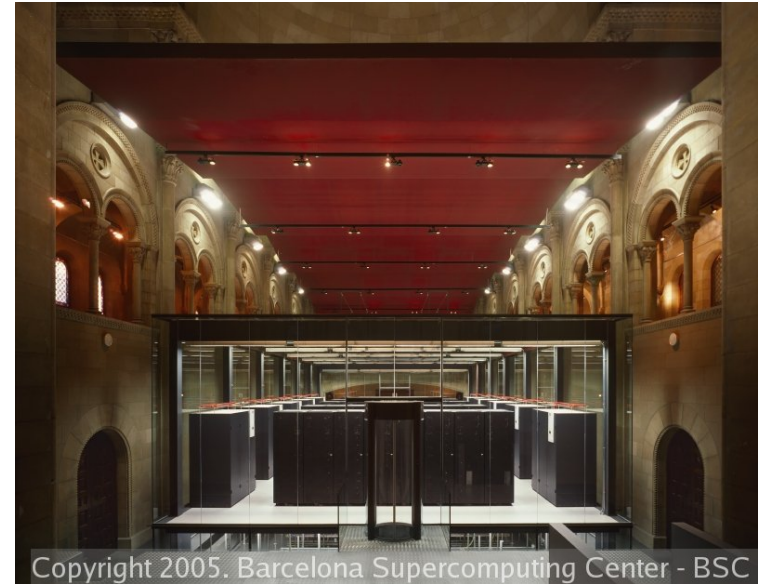
The Killer Mobile processors^{TM}

MFLOPS vs Year chart. Legend:
- Alpha
- Intel
- AMD
- Nvidia Tegra
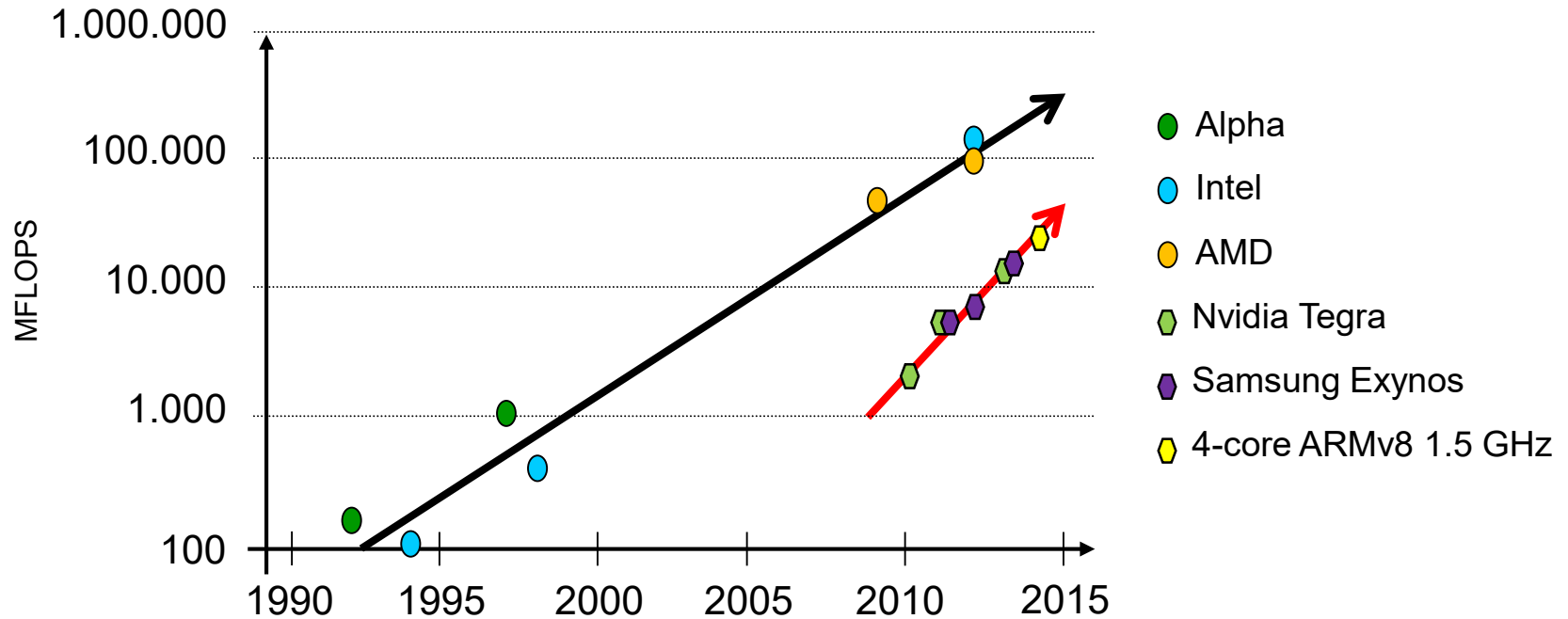- Samsung Exynos
- 4-core ARMv8 1.5 GHz

Y-axis (MFLOPS): 100, 1.000, 10.000, 100.000, 1.000.000
X-axis (Year): 1990, 1995, 2000, 2005, 2010, 2015

« Microprocessors killed the Vector supercomputers

  « They were not faster …

  « … but they were significantly cheaper and greener

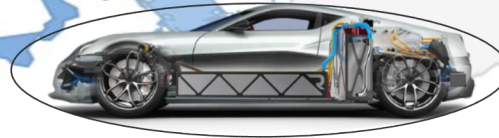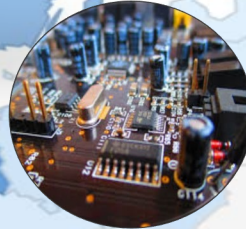« History may be about to repeat itself …

  « Mobile processor are not faster …

  « … but they are significantly cheaper and greener

Network of c.2,000 European R+D experts in advanced computing: **high-performance** and **embedded** architecture and compilation

720 members, 449 affiliated members and **871 affiliated PhD students** from **430** institutions in **46** countries.

hipeac.net

ARM-based prototypes at BSC

2011
Tibidabo

ARM multicore

2012
KAYLA

ARM + GPU
CUDA on ARM

2013
Pedraforca

ARM + GPU
Inifinband
RDMA
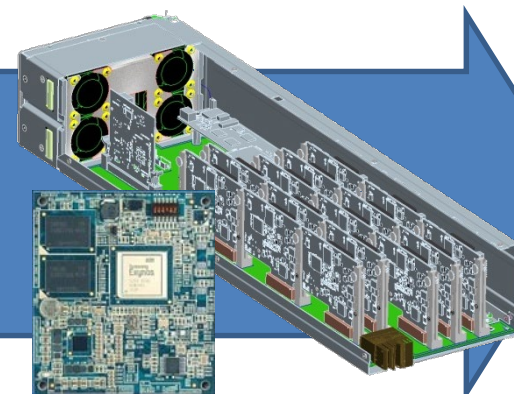
2014
Mont-Blanc

Single chip ARM+GPU
OpenCL on ARM GPU

Tibidabo: The first ARM HPC multicore cluster

Q7 Tegra 2
2 x Cortex-A9 @ 1GHz
2 GFLOPS
5 Watts (?)
0.4 GFLOPS / W

Q7 carrier board
2 x Cortex-A9
2 GFLOPS
1 GbE + 100 MbE
7 Watts
0.3 GFLOPS / W

1U Rackable blade
8 nodes
16 GFLOPS
65 Watts
0.25 GFLOPS / W

2 Racks
32 blade containers
  256 nodes
  512 cores
9x 48-port 1GbE switch

512 GFLOPS
3.4 Kwatt
0.15 GFLOPS / W

« Proof of concept
  – It is possible to deploy a cluster of smartphone processors

« Enable software stack development

BSC **Barcelona Supercomputing Center**
Centro Nacional de Supercomputación

Mont-Blanc HPC Stack for ARM

Industrial applications
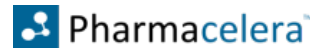
Applications

System software

Hardware

Press Impacts

BullSequana compute blade: X1310 Marvell ThunderX2™ (ARMv8) processor

▶ **Atos and ARMv8**
- – Atos is the industrial pivot of MontBlanc3
- – ARM is one of the Atos strategic directions for the next years
- – Europe is leading in ARM development
- – Montblanc project is proceeding as expected

▶ **BullSequana X1310 blade**
- – Up to 288 nodes in one BullSequana X1000 and up to 96 nodes in one BullSequana XH2000 with:
- – 3 compute nodes with 2 Marvell ThunderX2 (ARMv8) processors
- – Up to 1024 GB of Memory per node – DDR4 @2666 MT/s (w/64GB DIMMs)
- – High-speed Ethernet, InfiniBand EDR, HDR or HDR100 on the mezzanine interconnect
- – Up to 192 cores per blade
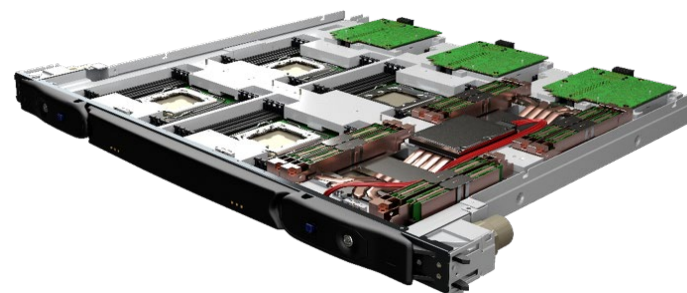
311 TFops

92 BullSequana X1310 blades, three compute nodes per blade, dual Marvell ThunderX2 processors of 32 cores @ 2.2 GHz, based on the Armv8-A instruction set, with 256 GB per node and Infiniband® EDR interconnect.

ARM processor – a credible alternative to X86 processor clusters

Atos

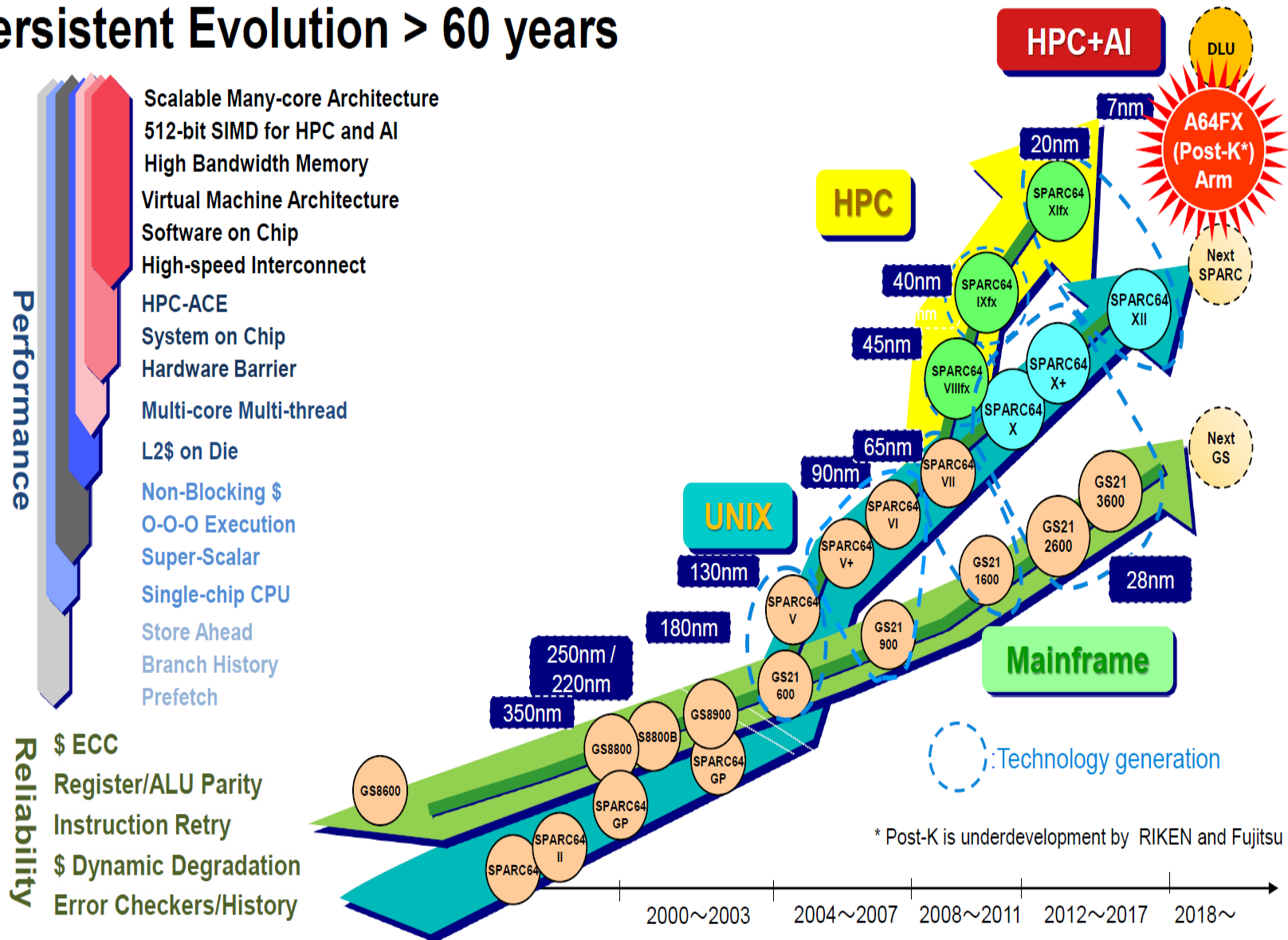# Fujitsu Processor Development

FUJITSU

Persistent Evolution > 60 years

Scalable Many-core Architecture
512-bit SIMD for HPC and AI
High Bandwidth Memory
Virtual Machine Architecture
Software on Chip
High-speed Interconnect
HPC-ACE
System on Chip
Hardware Barrier
Multi-core Multi-thread
L2$ on Die
Non-Blocking $
O-O-O Execution
Super-Scalar
Single-chip CPU
Store Ahead
Branch History
Prefetch

Performance

Reliability

$ ECC
Register/ALU Parity
Instruction Retry
$ Dynamic Degradation
Error Checkers/History

HPC+AI
DLU
7nm
20nm
HPC
SPARC64 XIfx
A64FX (Post-K*) Arm
Next SPARC
40nm
SPARC64 IXfx
SPARC64 XII
45nm
SPARC64 VIIIfx
SPARC64 X+
SPARC64 X
65nm
SPARC64 VII
Next GS
90nm
SPARC64 VI
GS21 3600
UNIX
SPARC64 V+
GS21 2600
130nm
SPARC64 V
GS21 1600
180nm
GS21 900
28nm
250nm / 220nm
GS21 600
Mainframe
350nm
GS8900
SPARC64 GP
GS8800
S8800B
SPARC64 GP
: Technology generation
GS8600
SPARC64 GP
SPARC64 II
SPARC64

* Post-K is underdevelopment by RIKEN and Fujitsu

2000~2003   2004~2007   2008~2011   2012~2017   2018~

3

USA

Sandia Labs:

- HPE, Astra Supercomputer
- 2592 nodes, 28 core dual
- 2.3 petaflops/peak, 1.529, Linpack)
- # 203, Top500 (Nov. 2018)
- #36, HPCG (Nov. 2018)

Others: (smaller systems)

- Nercs Labs: Cray, 1080 cores
- Argonne Labs: HPE, Comanche system

Why Europe needs its own Processors

- Processors now control almost every aspect of our lives

- **Security** (back doors etc.)

- Possible **future restrictions on exports to EU** due to **i**ncreasing protectionism

- **A competitive EU supply chain** for HPC technologies will create jobs and growth in Europe

NSA May Have Backdoors Built Into Intel And AMD Processors

Amazon exec and Super Micro CEO call retraction of spy chip story

'[Tim Cook] is right. Bloomberg story is wrong about Amazon, too.'

The US Cloud Act v The EU's GDPR - Data Privacy & Security

A group of researchers showed how a Tesla Model S can be hacked and stolen in seconds using only $600 worth of equipment

A jet sale to Egypt is being blocked by a US regulation, and France is over it

USA TODAY

Car hacking remains a very real threat as autos become ever more loaded with tech

Images courtesy of European Processor Initiative

HPC is a global competition

"The country with the strongest computing capability will host the world's next scientific breakthroughs".

US House Science, Space and Technology Committee Chairman
Lamar Smith (R-TX)

"Our goal is for Europe to become one of the top 3 world leaders in high-performance computing by 2020".

European Commission President
Jean-Claude Juncker (27 October 2015)

"Europe can develop an exascale machine with ARM technology. Maybe we need an ⊚ **AIRBUS** *consortium for HPC and Big Data".*

Seymour Cray Award Ceremony Nov. 2015
Mateo Valero

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

BSC and the EC

Final plenary panel at ICT - Innovate, Connect, Transform conference, 22 October 2015 Lisbon, Portugal.
the transformational impact of excellent science in research and innovation

""Europe needs to develop an entire domestic exascale stack from the processor all the way to the system and application software",
Mateo Valero, Director of Barcelona Supercomputing Center

Director of Barcelona Supercomputing Center, Mateo Valero, makes a pledge for developing a strong HPC ecosystem.

Published on 12/04/2016

Europe has the competence and skills to engage in the global competition towards Exascale Supercomputing. To fully benefit from the opportunities of the digital single market, Europe must strengthen the fundamental research on which digital transformation is based and build a stronger European High Performance Computing (HPC) ecosystem.

In a guest blog post on Commissioner Günther Oettinger's website Mateo Valero stresses the need for Europe to join the race towards Exascale supercomputing. According to him, there is an open window of opportunity for the High Performance Computing (HPC) development that would stimulate scientific breakthroughs and have tremendous impact on society and industry.

Share

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EuroHPC & EPI (European Processor Initiative)

- High Performance General Purpose Processor for HPC

- High-performance RISC-V based accelerator

- Computing platform for autonomous cars

- Will also target the AI, Big Data and other markets in order to be economically sustainable
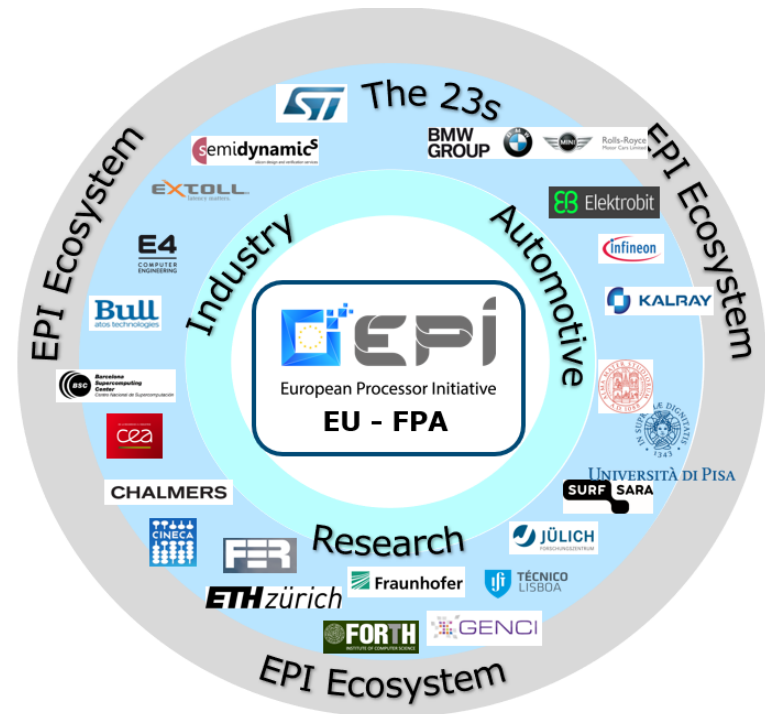
Images courtesy of European Processor Initiative

The Open-Source Hardware Opportunity

- In 2015 I said I believed a European Supercomputer based on ARM was possible (Mont-Blanc).

- Even though ARM is no longer European, it can form part of the short-term solution

- The fastest-growing movement in computing at the moment is Open-Source and is called RISC-V

- The future is Open and RISC-V is democratising chip-design

EuroHPC opens a window of opportunity to create the Airbus/Galileo of HPC
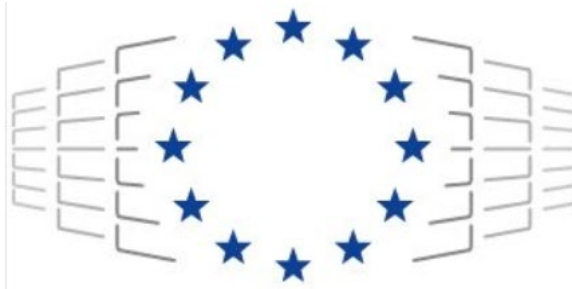
Mare Nostrum RISC-V inauguration 202X

MN-RISC-V

www.bsc.es

Thank you !!!

For further information please contact
mateo.valero@bsc.es